

Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE
Available

PRODUCT SUMMARY		
V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	1.1
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	2.7	
Q_{gd} (nC)	7.8	
Configuration	Single	

FEATURES

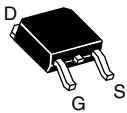
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR224, SiHFR224)
- Straight Lead (IRFU224, SiHFU224)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

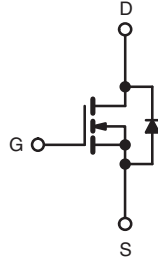
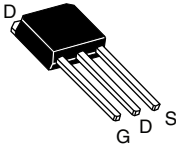
Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

DPAK
(TO-252)



IPAK
(TO-251)



N-Channel MOSFET

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR224-GE3	SiHFR224TR-GE3	SiHFR224TRL-GE3	SiHFU224-GE3
Lead (Pb)-free	IRFR224PbF	IRFR224TRPbF ^a	IRFR224TRLPbF ^a	IRFU224PbF
	SiHFR224-E3	SiHFR224T-E3 ^a	SiHFR224TL-E3 ^a	SiHFU224-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	V_{GS} at 10 V $T_C = 25$ °C	3.8
		$T_C = 100$ °C	2.4
Pulsed Drain Current ^a	I_{DM}	15	A
Linear Derating Factor		0.33	W/°C
Linear Derating Factor (PCB Mount) ^e		0.020	
Single Pulse Avalanche Energy ^b	E_{AS}	130	mJ
Repetitive Avalanche Current ^a	I_{AR}	3.8	A
Repetitive Avalanche Energy ^a	E_{AR}	4.2	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	42
		$T_A = 25$ °C	2.5
Peak Diode Recovery dV/dt ^c	dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s	260	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$ V; starting $T_J = 25$ °C, $L = 14$ mH, $R_g = 25$ Ω , $I_{AS} = 3.8$ A (see fig. 12).
- $I_{SD} \leq 3.8$ A, $di/dt \leq 90$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R _{thJA}	-	50	°C/W
Maximum Junction-to-Ambient	R _{thJA}	-	110	
Maximum Junction-to-Case	R _{thJC}	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		250	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.36	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 250 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.3 A ^b	-	-	1.1	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.3 A ^b		1.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^c		-	260	-	pF
Output Capacitance	C _{oss}			-	77	-	
Reverse Transfer Capacitance	C _{rss}			-	15	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.4 A, V _{DS} = 200 V, see fig. 6 and 13 ^{b, c}	-	-	14	nC
Gate-Source Charge	Q _{gs}			-	-	2.7	
Gate-Drain Charge	Q _{gd}			-	-	7.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 125 V, I _D = 4.4 A, R _G = 18 Ω, R _D = 28 Ω, see fig. 10 ^{b, c}		-	7.0	-	ns
Rise Time	t _r			-	13	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	12	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.8	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	15	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 3.8 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.4 A, dI/dt = 100 A/μs ^b		-	200	400	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.93	1.9	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

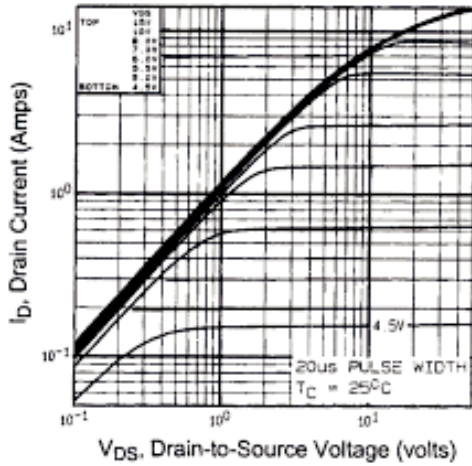


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

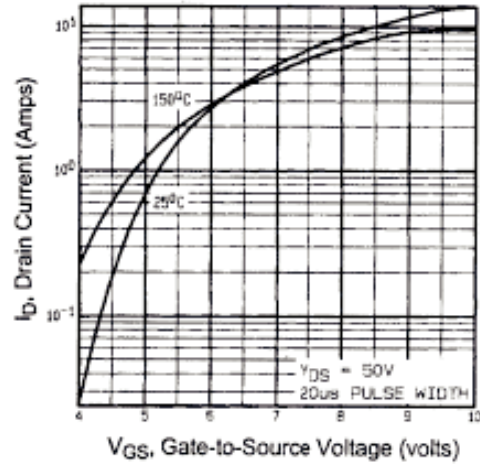


Fig. 3 - Typical Transfer Characteristics

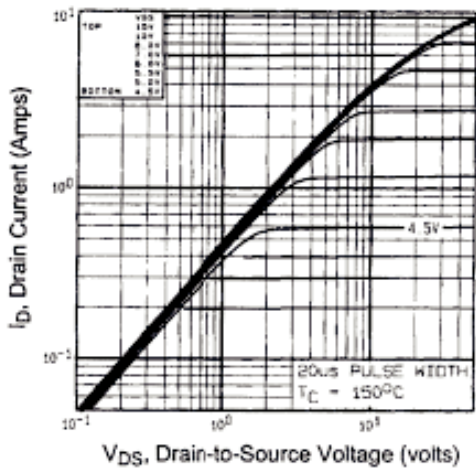


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

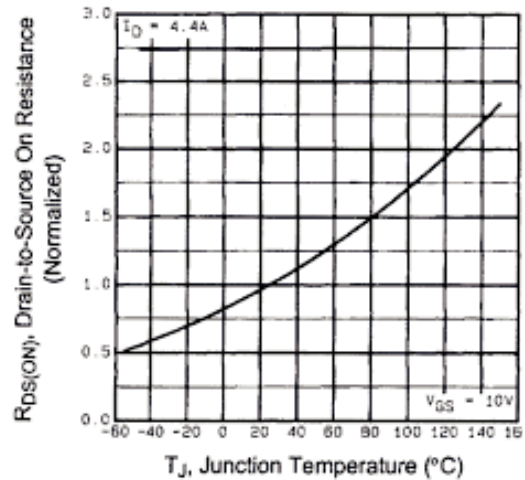


Fig. 4 - Normalized On-Resistance vs. Temperature

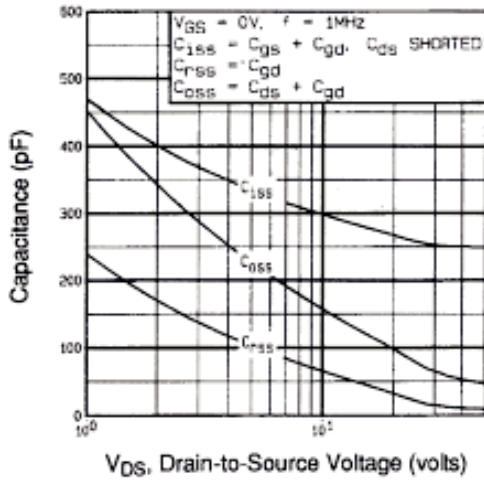


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

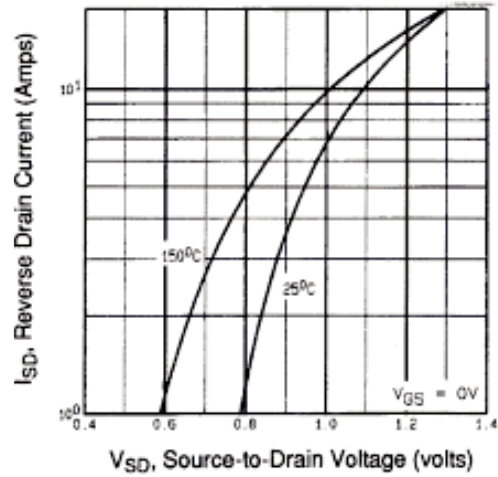


Fig. 7 - Typical Source-Drain Diode Forward Voltage

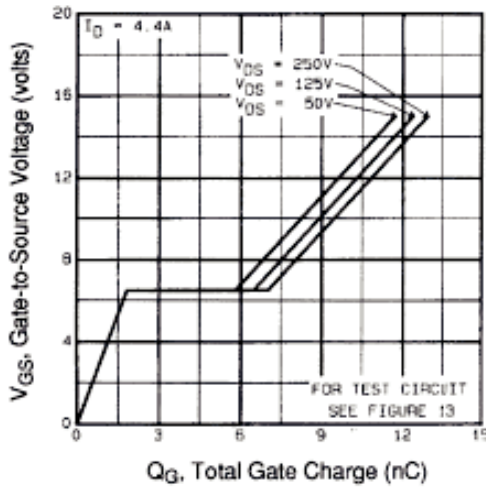


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

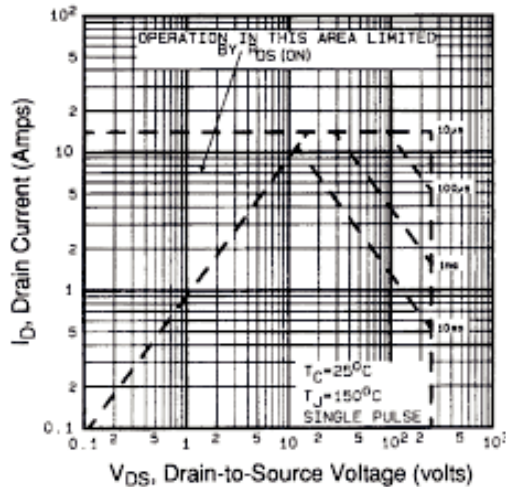


Fig. 8 - Maximum Safe Operating Area

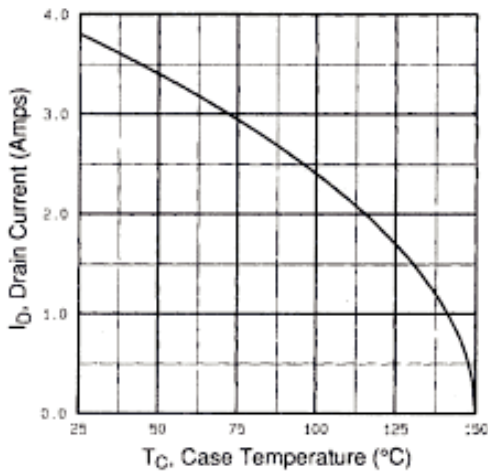


Fig. 9 - Maximum Drain Current vs. Case Temperature

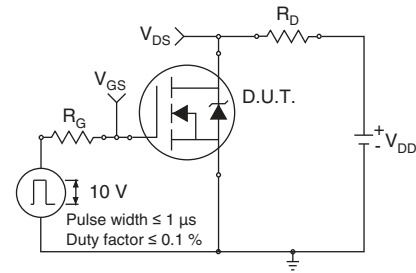


Fig. 10a - Switching Time Test Circuit

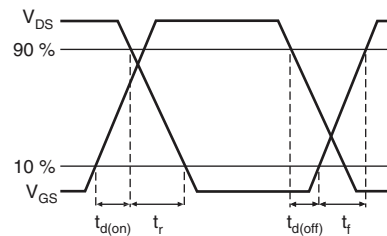


Fig. 10b - Switching Time Waveforms

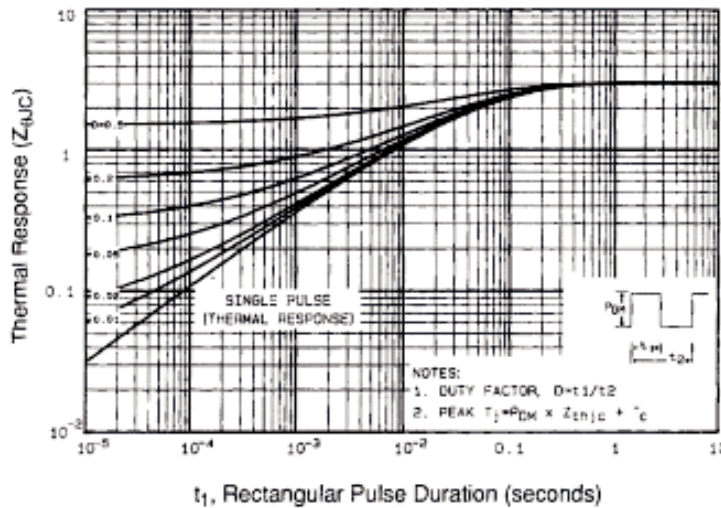


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

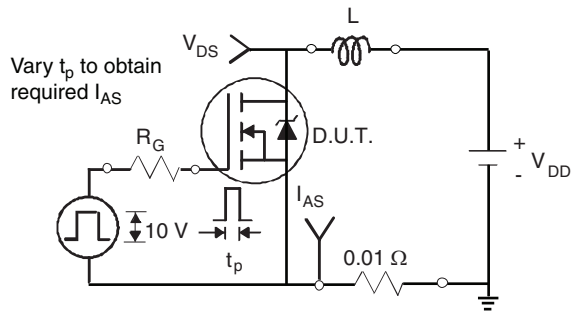


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

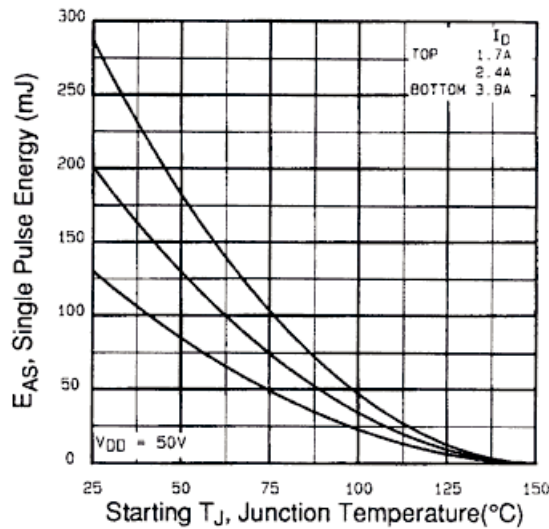


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

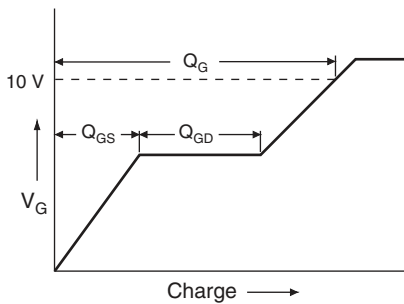


Fig. 13a - Basic Gate Charge Waveform

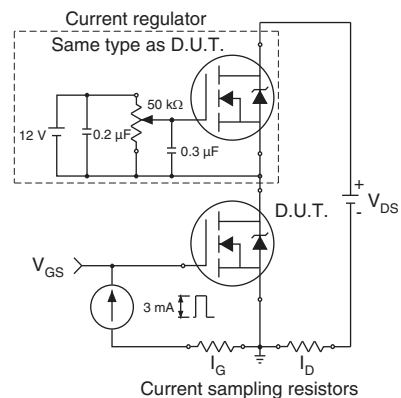


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08
 DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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