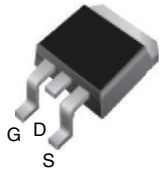
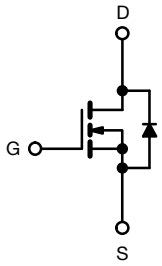
## Power MOSFET

D²PAK (TO-263)




N-Channel MOSFET

### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Logic-level gate drive
- $R_{DS(on)}$ specified at $V_{GS}$ = 4 V and 5 V
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

HALOGEN FREE Available

**Note**

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 60 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 5.0 V | 0.028 |
| $Q_g$ (Max.) (nC) | 66 | |
| $Q_{gs}$ (nC) | 12 | |
| $Q_{gd}$ (nC) | 43 | |
| Configuration | Single | |

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

| ORDERING INFORMATION | | |
|---|---|---|
| Package | D²PAK (TO-263) | D²PAK (TO-263) |
| Lead (Pb)-free and Halogen-free | SiHLZ44S-GE3 | SiHLZ44STRR-GE3[a] |
| Lead (Pb)-free | IRLZ44SPbF | IRLZ44STRRPbF[a] |

**Note**

a. See device orientation

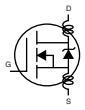
| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 10 | |
| Continuous Drain Current[f] | $V_{GS}$ at 5.0 V | $T_C$ = 25 °C | $I_D$ | 50 | A |
| Continuous Drain Current | | $T_C$ = 100 °C | | 36 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 200 | |
| Linear Derating Factor | | | | 1.0 | W/°C |
| Linear Derating Factor (PCB Mount)[e] | | | | 0.025 | |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 400 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 150 | W |
| Maximum Power Dissipation (PCB Mount)[e] | $T_A$ = 25 °C | | | 3.7 | |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 175 | °C |
| Soldering Recommendations (Peak Temperature)[d] | For 10 s | | | 300[d] | |

**Notes**

b. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
c. $V_{DD}$ = 25 V, starting $T_J$ = 25 °C, L = 179 μH, $R_g$ = 25 Ω, $I_{AS}$ = 51 A (see fig. 12)
d. $I_{SD} \leq$ 51 A, dI/dt ≤ 250 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C
e. 1.6 mm from case
f. When mounted on 1" square PCB (FR-4 or G-10 material)
g. Current limited by the package, (die current = 51 A)

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount)[a] | $R_{thJA}$ | - | 40 | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 1.0 | |

**Note**
a. When mounted on 1" square PCB (FR-4 or G-10 material)

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = 250 µA | | 60 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.070 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 1.0 | - | 2.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 10 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | - | - | 25 | µA |
| | | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V, $T_J$ = 150 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 5.0 V | $I_D$ = 31 A[b] | - | - | 0.028 | Ω |
| | | $V_{GS}$ = 4.0 V | $I_D$ = 25 A[b] | - | - | 0.039 | |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 25 V, $I_D$ = 31 A[b] | | 23 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 3300 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 1200 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 200 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 5.0 V | $I_D$ = 51 A, $V_{DS}$ = 48 V, see fig. 6 and 13[b] | - | - | 66 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 12 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 43 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $I_D$ = 51 A, $R_g$ = 4.6 Ω, $R_D$ = 0.56 Ω, see fig. 10[b] | | - | 17 | - | ns |
| Rise Time | $t_r$ | | | - | 230 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 42 | - | |
| Fall Time | $t_f$ | | | - | 110 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 50[c] | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 200 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 51 A, $V_{GS}$ = 0 V[b] | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 51 A, dI/dt = 100 A/µs[b] | | - | 130 | 180 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 0.84 | 1.3 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %
c. Current limited by the package, (Die Current = 51 A)

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

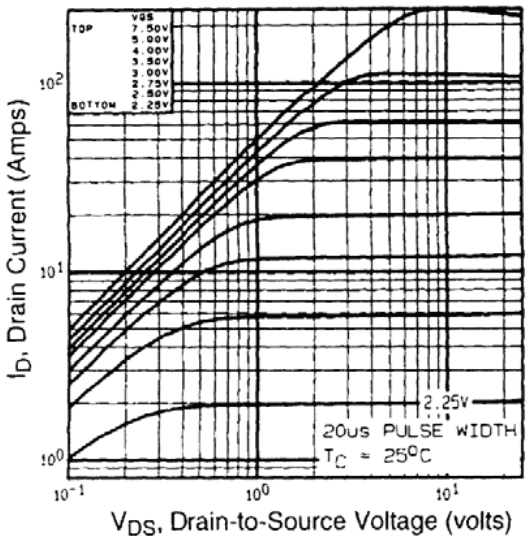



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

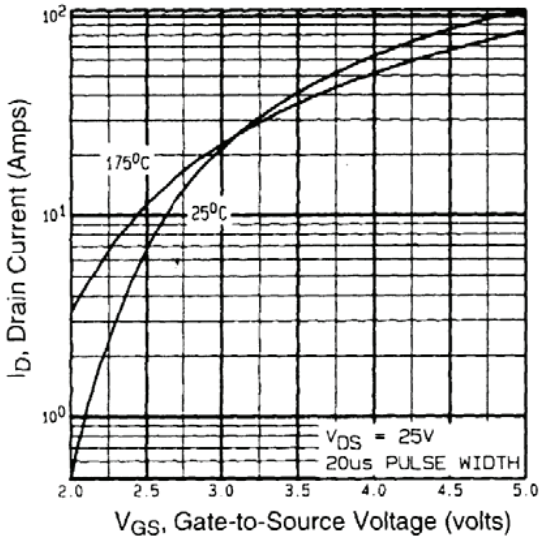



**Fig. 2 - Typical Transfer Characteristics**

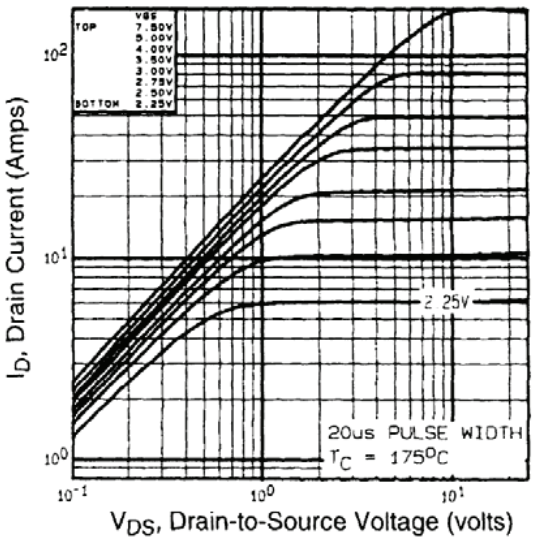



**Fig. 1 - Typical Output Characteristics, $T_C$ = 150 °C**

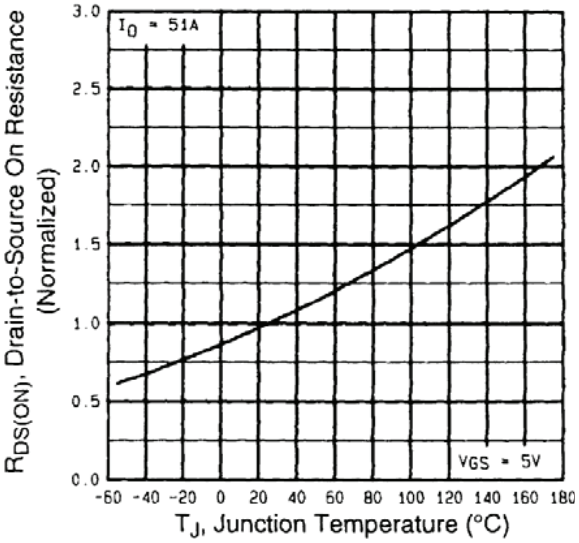



**Fig. 3 - Normalized On-Resistance vs. Temperature**

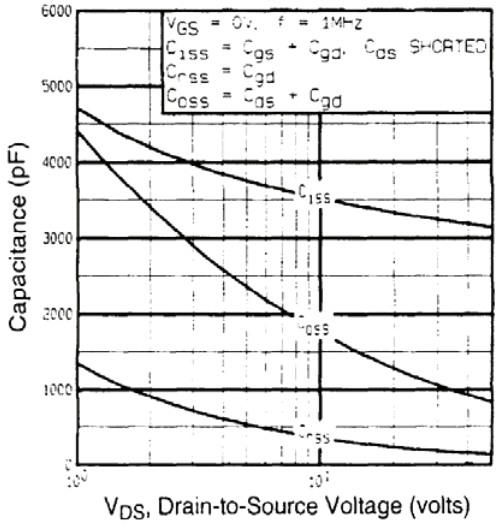



**Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage**

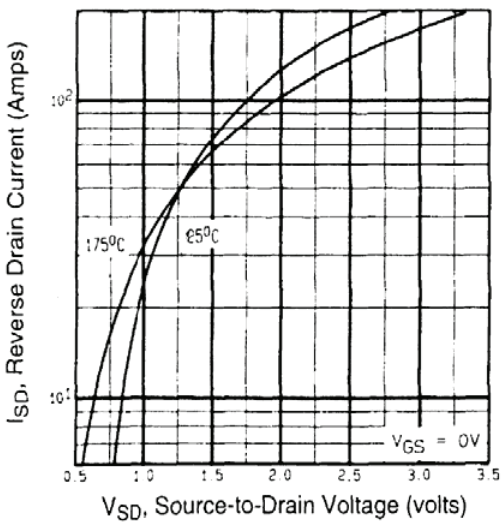



**Fig. 6 - Typical Source-Drain Diode Forward Voltage**

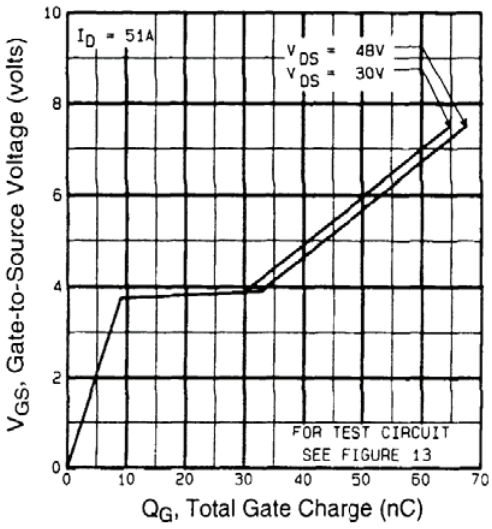



**Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage**

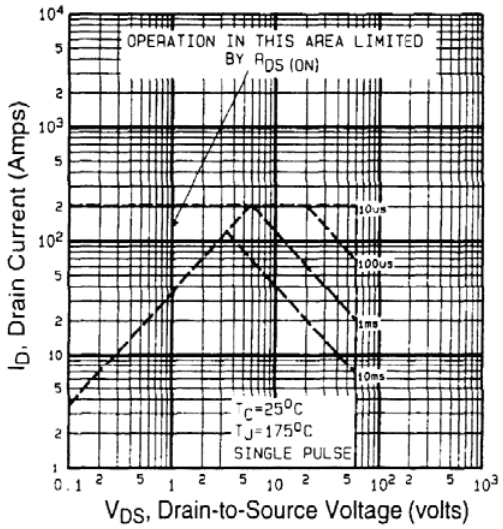



**Fig. 7 - Maximum Safe Operating Area**

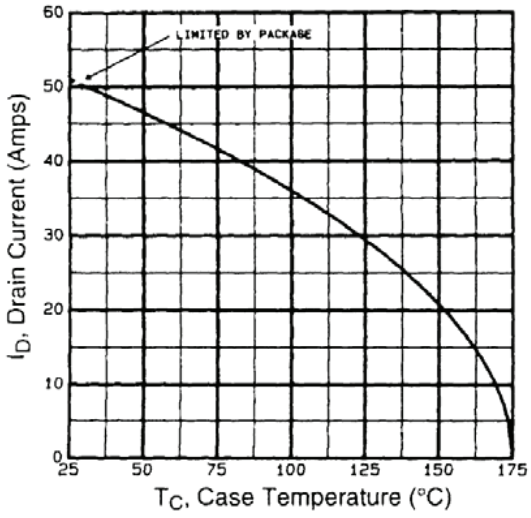



**Fig. 8 - Maximum Drain Current vs. Case Temperature**

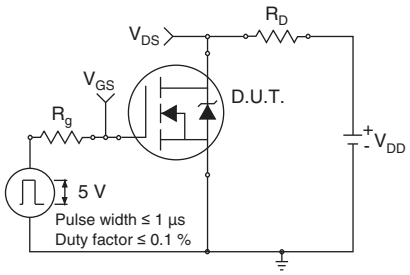



**Fig. 10a - Switching Time Test Circuit**

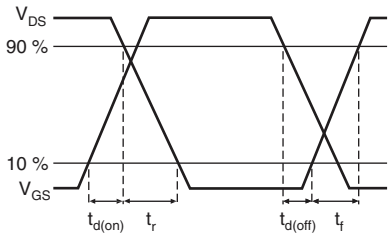



**Fig. 10b - Switching Time Waveforms**

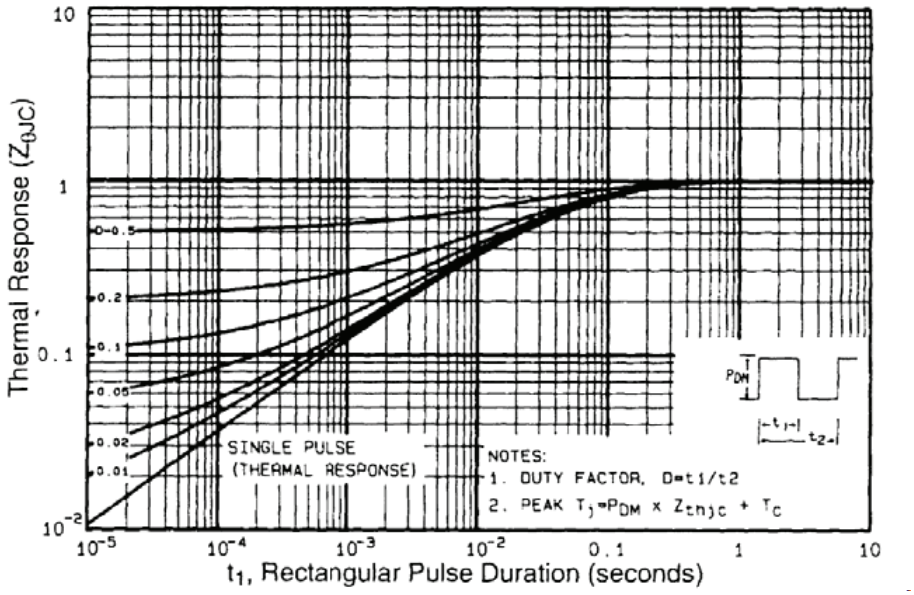



**Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

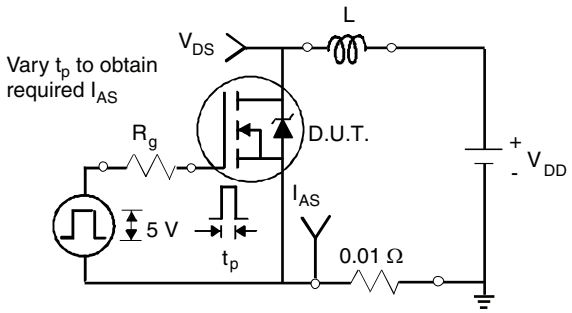



**Fig. 12a - Unclamped Inductive Test Circuit**

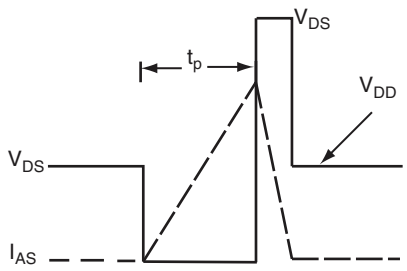



**Fig. 12b - Unclamped Inductive Waveforms**

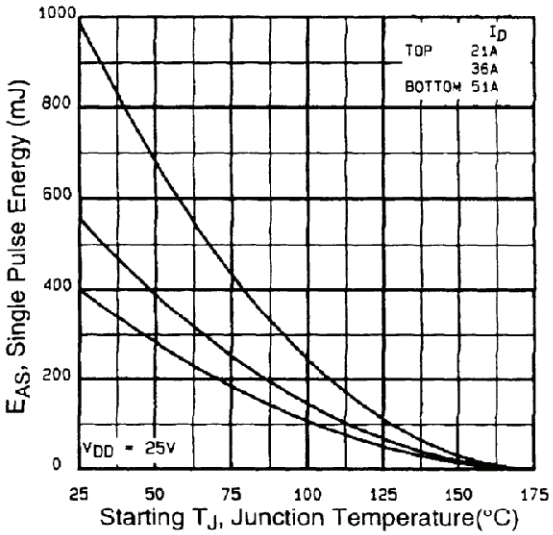



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

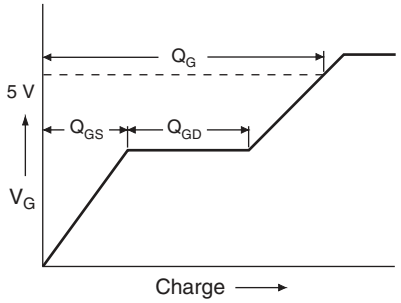



**Fig. 13a - Basic Gate Charge Waveform**

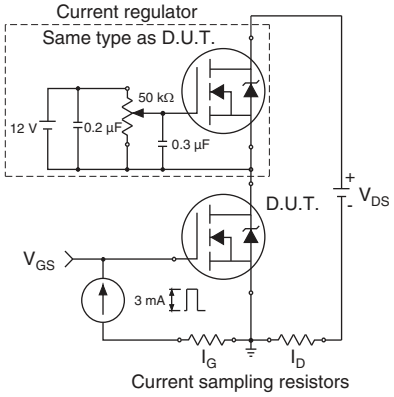
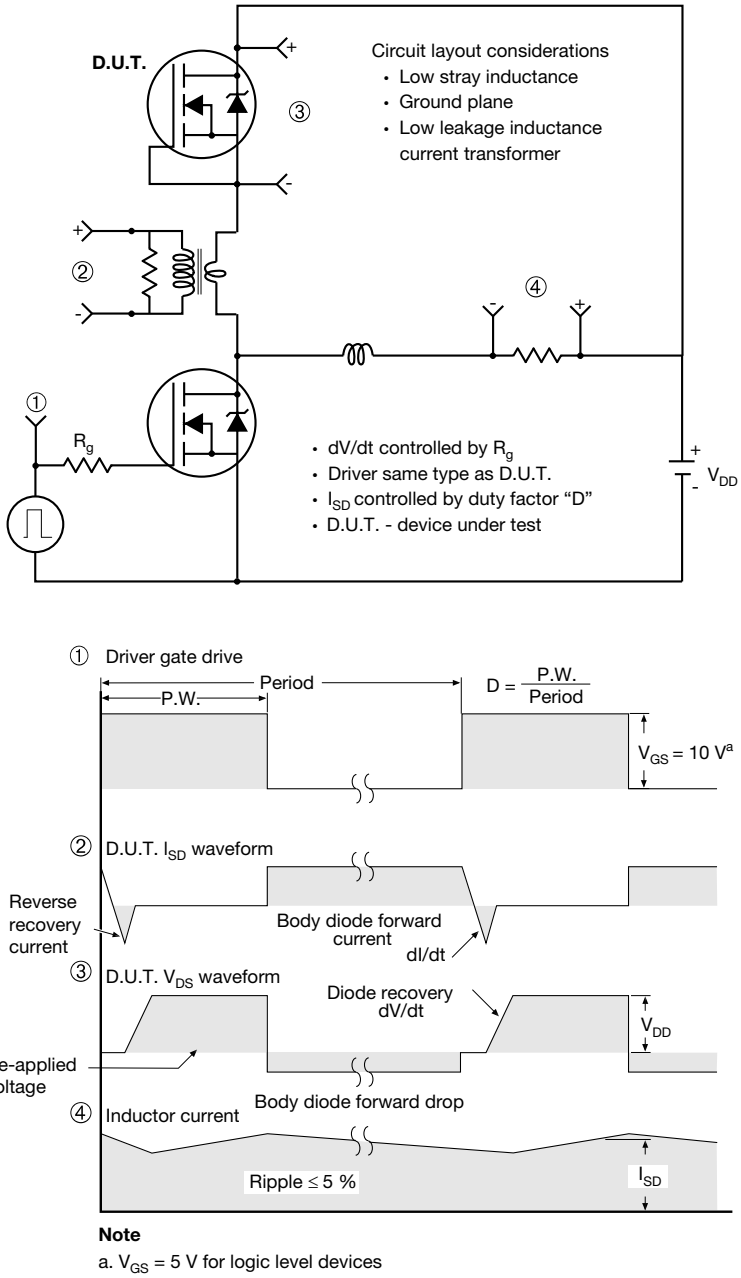



**Fig. 13b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**

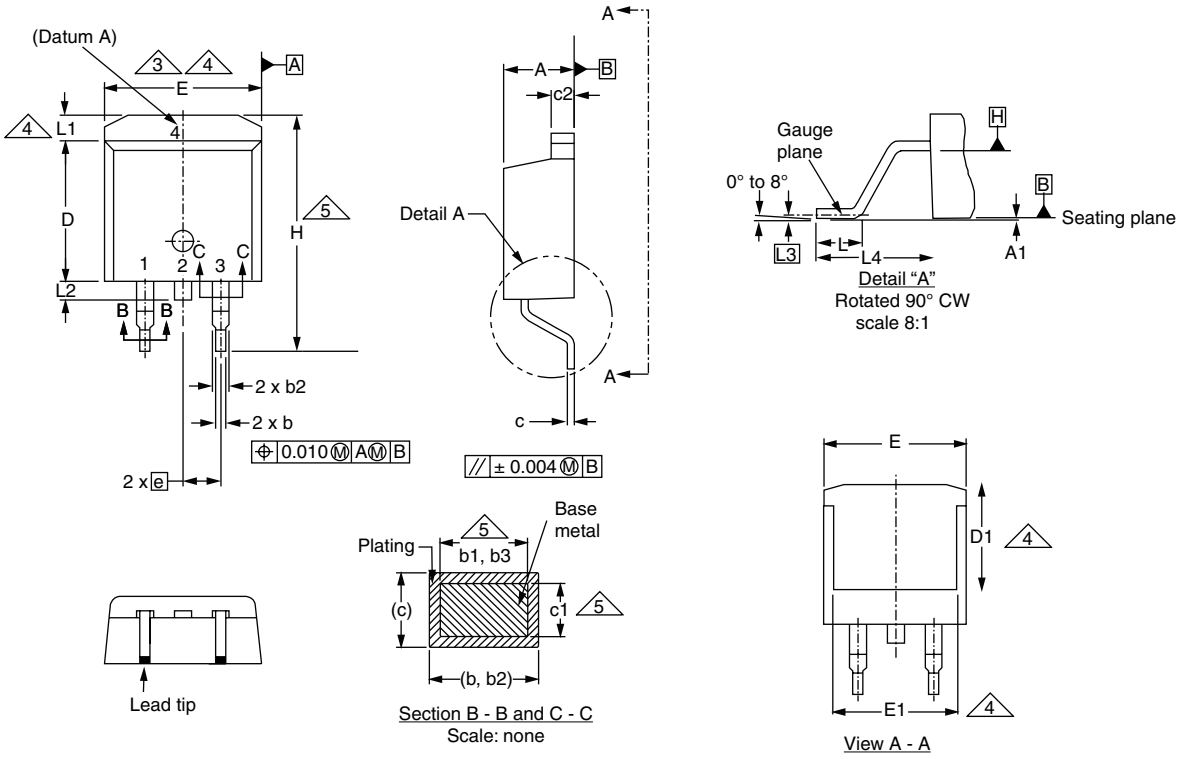



**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 10 - For N-Channel**

## TO-263AB (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

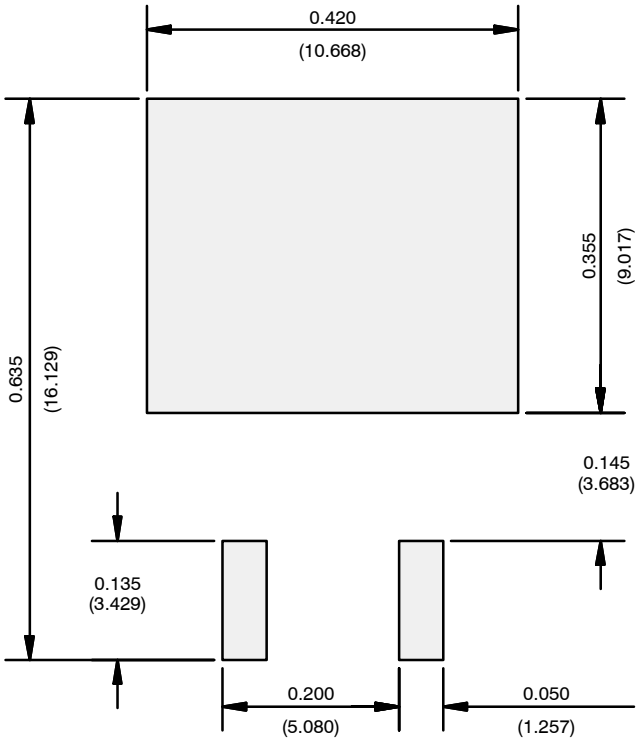
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

## RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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