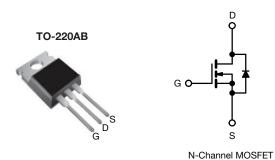
Vishay Siliconix

RoHS COMPLIANT

HALOGEN

FREE

# **E Series Power MOSFET**



PRODUCT SUMMARY					
$V_{DS}$ (V) at $T_J$ max.	550				
R <sub>DS(on)</sub> max. at 25 °C (Ω)	$V_{GS} = 10 \text{ V}$	0.145			
Q <sub>g</sub> (Max.) (nC)	86				
Q <sub>gs</sub> (nC)	14				
Q <sub>gd</sub> (nC)	25				
Configuration	Single				

### **FEATURES**

- Low figure-of-merit (FOM): Ron x Qg
- Low input capacitance (C<sub>iss</sub>)
- · Reduced switching and conduction losses
- Low gate charge (Qq)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>



- Hard switched topologies
- Power factor correction power supplies (PFC)
- Switch mode power supplies (SMPS)
- Computing
  - PC silver box / ATX power supplies
- Lighting
  - Two stage LED lighting

ORDERING INFORMATION				
Package	TO-220AB			
Lead (Pb)-free and halogen-free	SiHP25N50E-BE3 <sup>a</sup>			
	SiHP25N50E-GE3			

### Note

a. "-BE3" denotes alternate manufacturing location

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	500		
Gate-source voltage			$V_{GS}$	± 30	V	
Continuous drain current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I <sub>D</sub>	26	А	
		T <sub>C</sub> = 100 °C		16		
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	50		
Linear derating factor				0.2	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	273	mJ	
Maximum power dissipation			P <sub>D</sub>	250	W	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Drain-source voltage slope	T <sub>J</sub> = 125 °C		d///dt	65	1//20	
Reverse diode dV/dt <sup>d</sup>			dV/dt	25	V/ns	
Soldering recommendations (peak temperature) c	For 10 s			300	°C	

### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b.  $V_{DD}$  = 50 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 4.4 A
- c. 1.6 mm from case
- d.  $I_{SD} \le I_D$ , dI/dt = 100 A/ $\mu$ s, starting  $T_J = 25$  °C



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W	
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.5	G/VV	

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		•		Ţ	!	!	
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	500	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	Reference to 25 °C, I <sub>D</sub> = 1 mA			-	V/°C
Gate-source threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$			4.0	V
Osta saura laslana		V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Gate-source leakage	I <sub>GSS</sub>	,	$V_{GS} = \pm 30 \text{ V}$		-	± 1	μΑ
Zana anta nalta na dunia annuant		V <sub>DS</sub> =	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$		-	1	μА
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 400 V			-	25	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A	-	0.125	0.145	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 12 A		-	6.6	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ f = 1  MHz		-	1980	-	pF
Output capacitance	C <sub>oss</sub>			-	105	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	8	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		-	105	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	285	-	
Total gate charge	Qg			-	57	86	
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 12 \text{ A}, V_{DS} = 400 \text{ V}$		14	-	nC
Gate-drain charge	Q <sub>gd</sub>			-	25	-	1
Turn-on delay time	t <sub>d(on)</sub>	$V_{DD} = 400 \text{ V}, I_{D} = 12 \text{ A}$ $R_{g} = 9.1 \Omega, V_{GS} = 10 \text{ V}$		-	19	38	ns
Rise time	t <sub>r</sub>			-	36	72	
Turn-off delay time	t <sub>d(off)</sub>			-	57	86	
Fall time	t <sub>f</sub>			-	29	58	
Gate input resistance	$R_g$	f = 1 MHz, open drain		-	0.56	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	12	
Pulsed diode forward current	I <sub>SM</sub>			-	-	50	A
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 16.5 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	$T_J = 25 \text{ °C, } I_F = I_S,$ $dI/dt = 100 \text{ A/}\mu\text{s, } V_R = 25 \text{ V}$		-	338	-	ns
Reverse recovery charge	Q <sub>rr</sub>			-	5.3	-	μC
Reverse recovery current	I <sub>RRM</sub>			_	29	_	Α

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$  b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

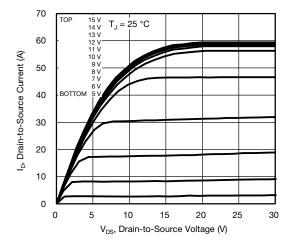


Fig. 1 - Typical Output Characteristics

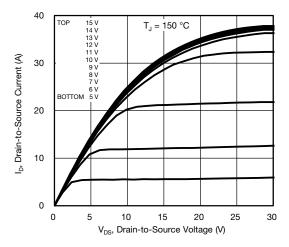


Fig. 2 - Typical Output Characteristics

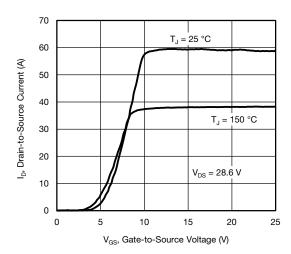


Fig. 3 - Typical Transfer Characteristics

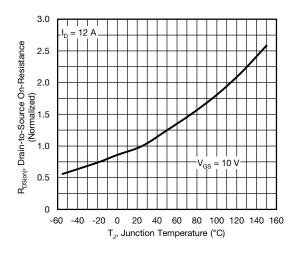


Fig. 4 - Normalized On-Resistance vs. Temperature

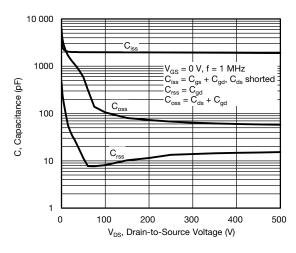


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

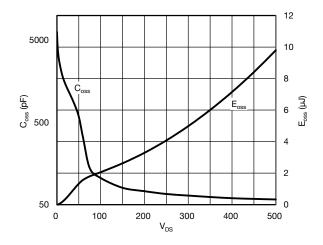


Fig. 6 -  $C_{OSS}$  and  $E_{OSS}$  vs.  $V_{DS}$ 



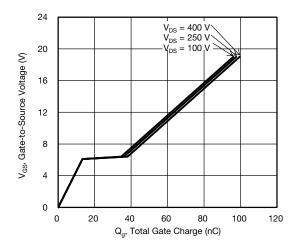


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

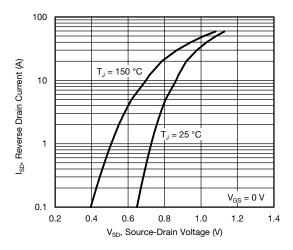


Fig. 8 - Typical Source-Drain Diode Forward Voltage

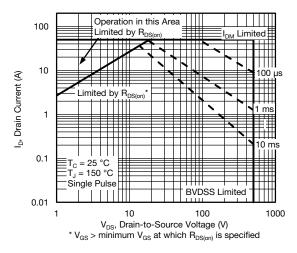


Fig. 9 - Maximum Safe Operating Area

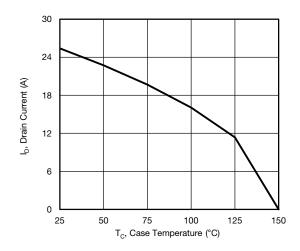


Fig. 10 - Maximum Drain Current vs. Case Temperature

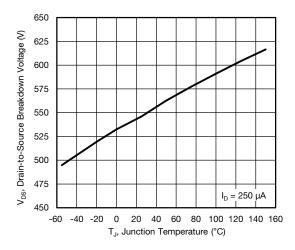


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature



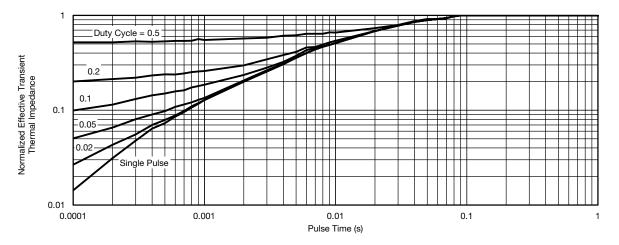


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

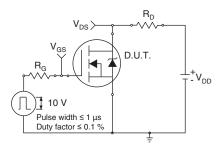


Fig. 13 - Switching Time Test Circuit

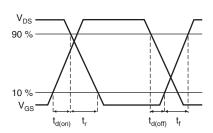


Fig. 14 - Switching Time Waveforms

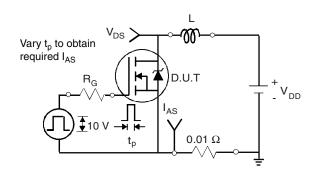


Fig. 15 - Unclamped Inductive Test Circuit

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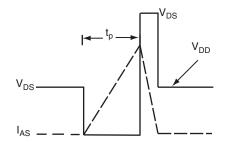


Fig. 16 - Unclamped Inductive Waveforms

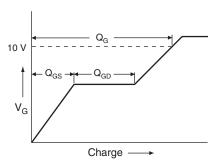


Fig. 17 - Basic Gate Charge Waveform

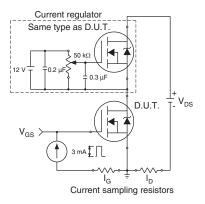
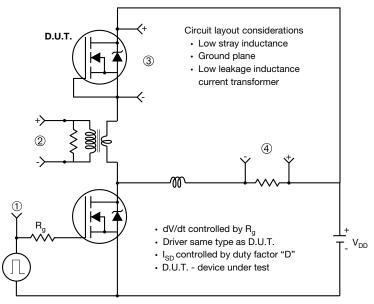


Fig. 18 - Gate Charge Test Circuit



## Peak Diode Recovery dV/dt Test Circuit



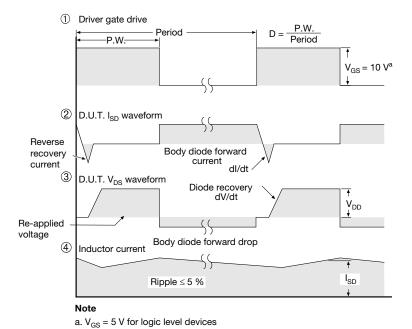


Fig. 19 - For N-Channel

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