

## E Series Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	550
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V   0.380
$Q_g$ max. (nC)	50
$Q_{gs}$ (nC)	6
$Q_{gd}$ (nC)	10
Configuration	Single

### FEATURES

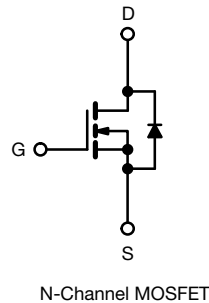
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Computing
  - PC silver box / ATX power supplies
- Lighting
  - Two stage LED lighting
- Consumer electronics
- Applications using hard switched topologies
  - Power factor correction (PFC)
  - Two switch forward converter
  - Flyback converter
- Switch mode power supplies (SMPS)




ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SiHD12N50E-GE3
	SiHD12N50E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	10.5
		$T_C = 100$ °C	6.6
Pulsed drain current <sup>a</sup>	$I_{DM}$	21	A
Linear derating factor		0.91	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	103	mJ
Maximum power dissipation	$P_D$	114	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$V_{DS} = 0$ V to 80 % $V_{DS}$	70	V/ns
Reverse diode dV/dt <sup>d</sup>		27	
Soldering recommendations (peak temperature) <sup>c</sup>	for 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.7$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction to ambient	$R_{thJA}$	-	62	°C/W
Maximum junction to case (drain)	$R_{thJC}$	-	1.1	

<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.60	-	V/ $^\circ\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	-	0.330	0.380	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 6\text{ A}$	-	3.1	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	886	-	pF
Output capacitance	$C_{oss}$		-	52	-	
Reverse transfer capacitance	$C_{rss}$		-	6	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	45	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$		-	131	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}, V_{DS} = 400\text{ V}$	-	25	50	nC
Gate-source charge	$Q_{gs}$		-	6	-	
Gate-drain charge	$Q_{gd}$		-	10	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 6\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$	-	13	26	ns
Rise time	$t_r$		-	16	32	
Turn-off delay time	$t_{d(off)}$		-	29	58	
Fall time	$t_f$		-	12	24	
Gate input resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$	-	0.92	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	10.5	A
Pulsed diode forward current	$I_{SM}$		-	-	21	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 7.5\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$	-	244	-	ns
Reverse recovery charge	$Q_{rr}$		-	2.5	-	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$		-	19	-	A

**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

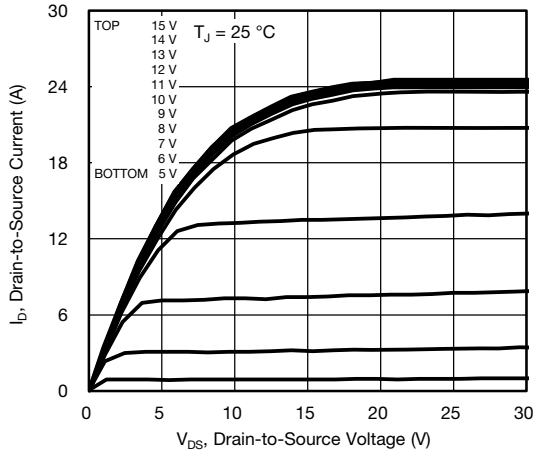


Fig. 1 - Typical Output Characteristics

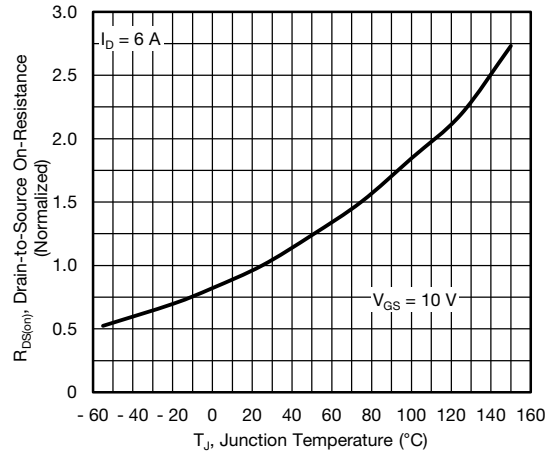


Fig. 4 - Normalized On-Resistance vs. Temperature

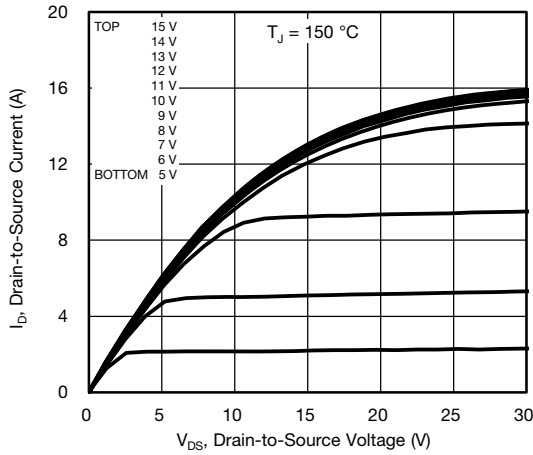


Fig. 2 - Typical Output Characteristics

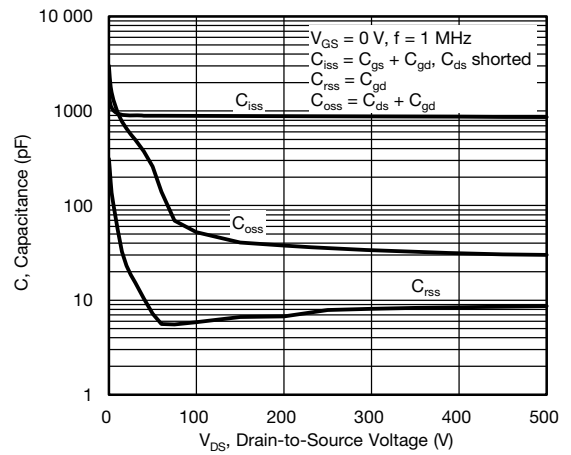


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

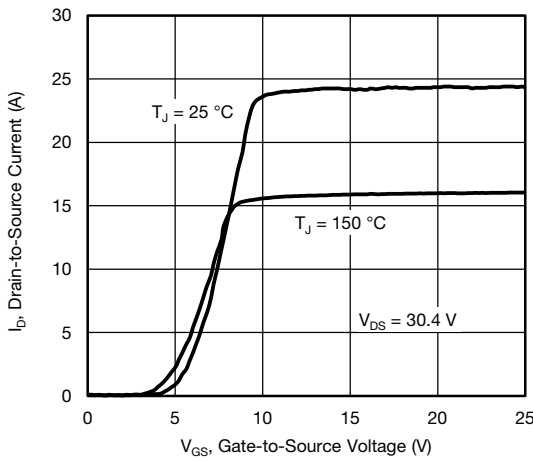


Fig. 3 - Typical Transfer Characteristics

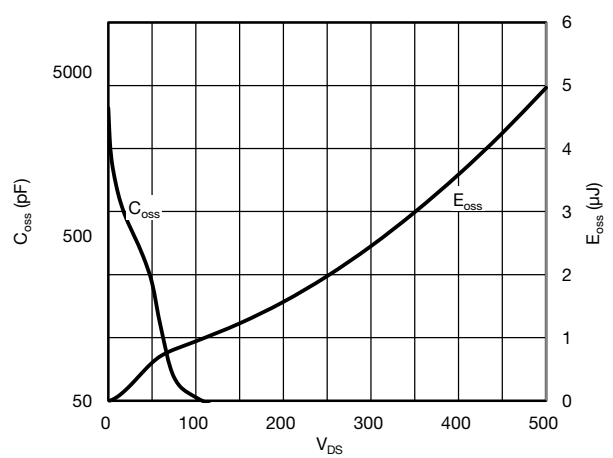


Fig. 6 -  $C_{OSS}$  and  $E_{OSS}$  vs.  $V_{DS}$

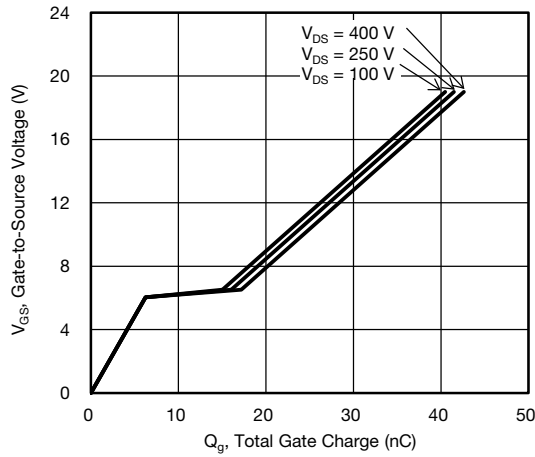


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

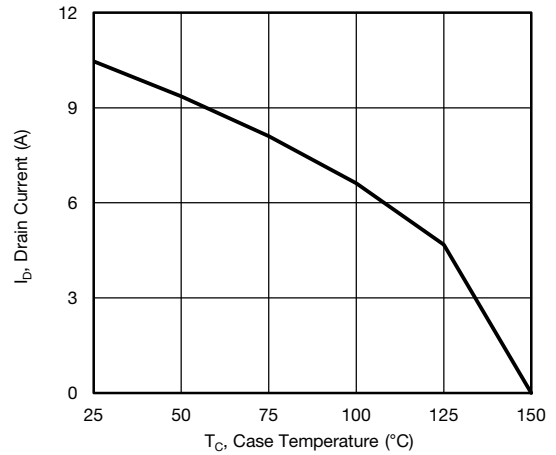


Fig. 10 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Typical Source-Drain Diode Forward Voltage

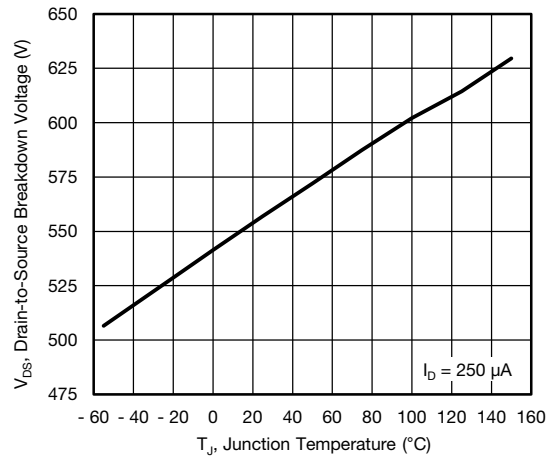


Fig. 11 - Temperature vs. Drain-to-Source Voltage

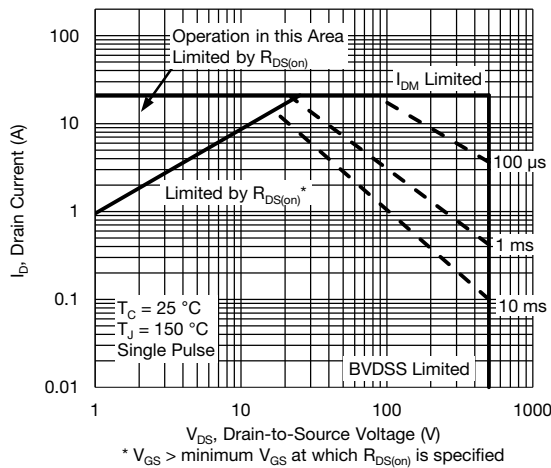
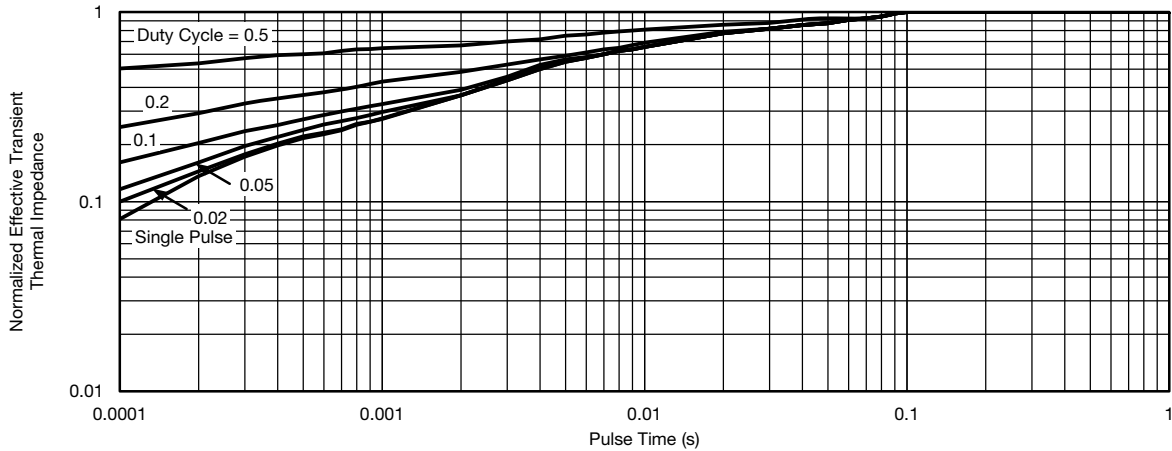


Fig. 9 - Maximum Safe Operating Area



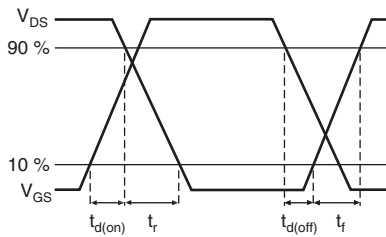
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



**Fig. 13 - Switching Time Test Circuit**



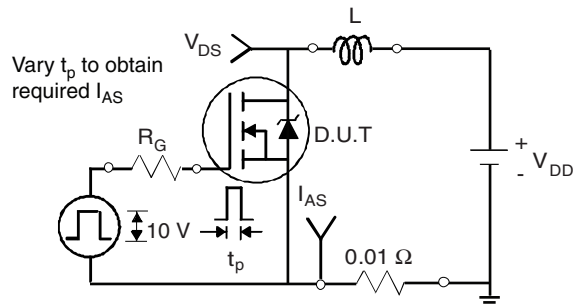
**Fig. 16 - Unclamped Inductive Waveforms**



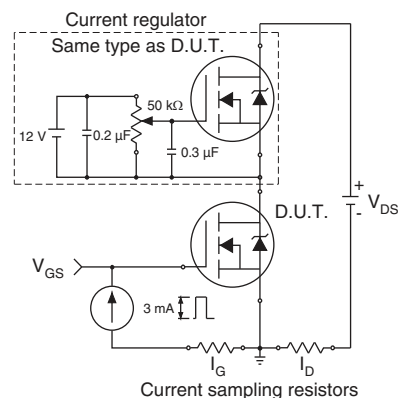
**Fig. 14 - Switching Time Waveforms**



**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

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# TO-252AA Case Outline

## VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

### Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022  
 DWG: 5347



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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