

**Vishay Siliconix** 

# **EF Series Power MOSFET with Fast Body Diode**

### DESCRIPTION

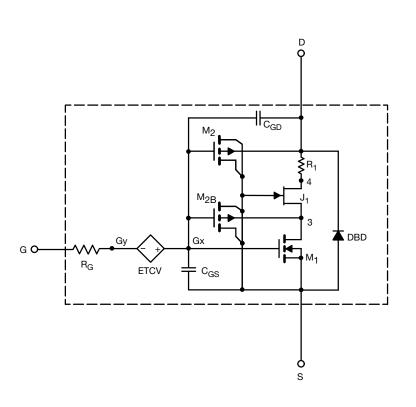
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched Cgd model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



#### Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



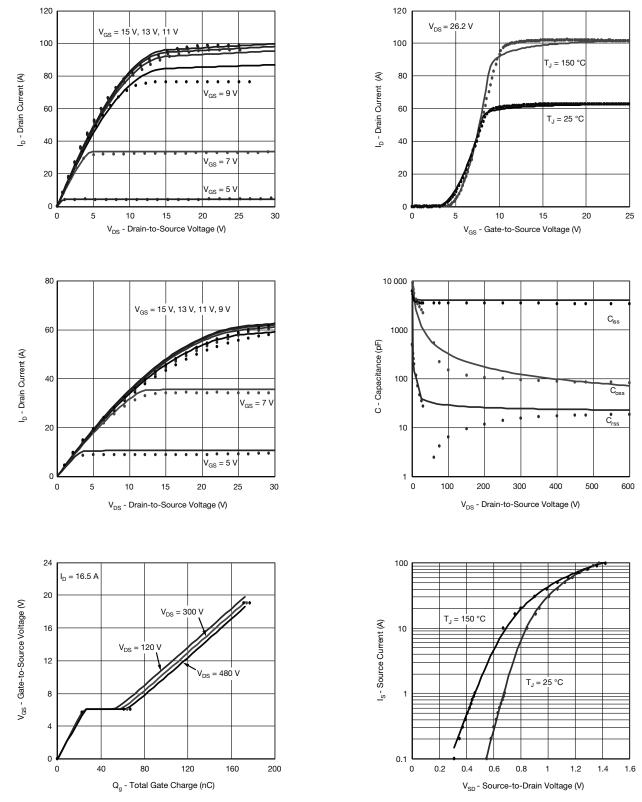
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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	3	-	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 16.5 \text{ A}$	0.098	0.085	Ω
Forward Transconductance	<b>g</b> fs	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 16.5 \text{ A}$	11	12	S
Dynamic					
Input Capacitance	C <sub>iss</sub>	$V_{DS}$ = 100 V, $V_{GS}$ = 0 V, f = 1 MHz	4080	3454	pF
Output Capacitance	Coss		320	154	
Reverse Transfer Capacitance	C <sub>rss</sub>		28	8	
Total Gate Charge	Qg	$V_{DS}$ = 480 V, $V_{GS}$ = 10 V, $I_{D}$ = 16.5 A	102	103	nC
Gate-Source Charge	Q <sub>gs</sub>		22	22	
Gate-Drain Charge	Q <sub>gd</sub>		43	43	
Drain-Source Body Diode Characteristics					
Diode Forward Voltage	V <sub>SD</sub>	$T_J=25~^\circ C,~I_S=16.5~A,~V_{GS}=0~V$	0.90	0.90	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = I_S = 16.5 \text{ A}, $ dl/dt = 100 A/µs, V <sub>R</sub> = 25 V	160	162	ns
Reverse Recovery Charge	Q <sub>rr</sub>		1.1	1	μC



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## COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

S16-1485-Rev. B, 01-Aug-16

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Document Number: 91660

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