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Vishay Siliconix

EF Series Power MOSFET with Fast Body Diode

DESCRIPTION

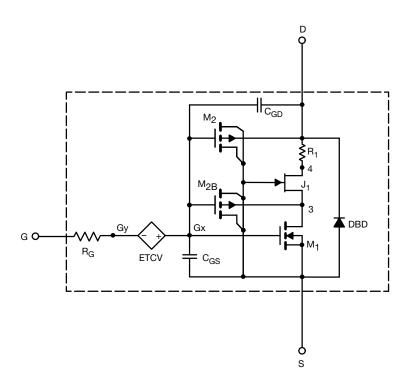
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- · Model the Gate Charge



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer
to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model SiHG70N60EF

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 35 \text{ A}$	0.043	0.033	Ω
Forward Transconductance a	9 _{fs}	$V_{DS} = 30 \text{ V}, I_D = 35 \text{ A}$	32	25	S
Diode Forward Voltage	V _{SD}	I _S = 35 A, V _{GS} = 0 V	0.90	0.90	V
Dynamic ^b					
Input Capacitance	C _{iss}		9640	7500	
Output Capacitance	C _{oss}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	441	378	pF
Reverse Transfer Capacitance	C _{rss}		57	5	
Total Gate Charge	Qg		247	253	
Gate-Source Charge	Q _{gs}	$V_{DS} = 480 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 35 \text{ A}$	62	62	nC
Gate-Drain Charge	Q _{gd}		102	102	

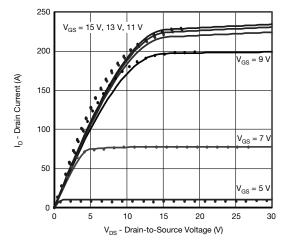
Notes

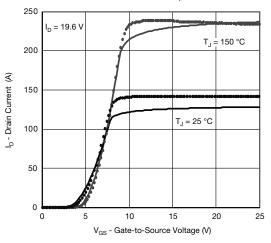
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

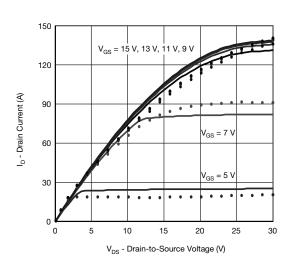
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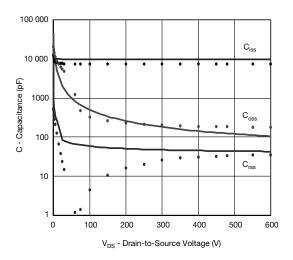
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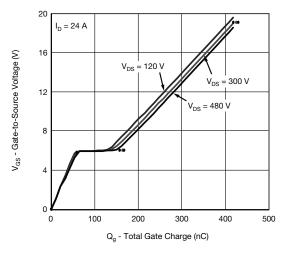
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25~^{\circ}\text{C}$, unless otherwise noted)

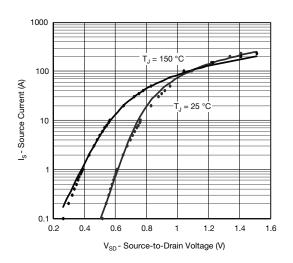












Note

Dots and squares represent measured data.
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