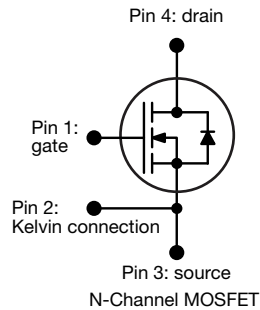
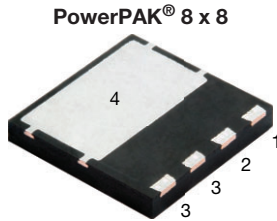


E Series Power MOSFET



FEATURES

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.148
Q_g max. (nC)	99	
Q_{gs} (nC)	16	
Q_{gd} (nC)	28	
Configuration	Single	

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION

Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH21N65E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	20.3	A
		$T_C = 100$ °C	12.8	
Pulsed drain current ^a	I_{DM}	53		
Linear derating factor		1.47	W/°C	
Single pulse avalanche energy ^b	E_{AS}	353	mJ	
Maximum power dissipation	P_D	156	W	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Drain-source voltage slope	dV/dt	$T_J = 125$ °C	70	V/ns
Reverse diode dV/dt ^c		17		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 5$ A
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C

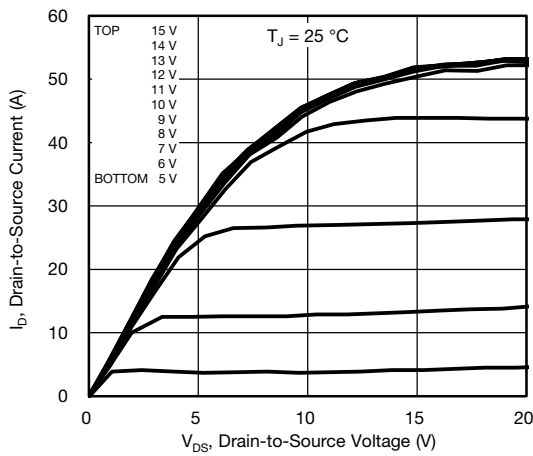
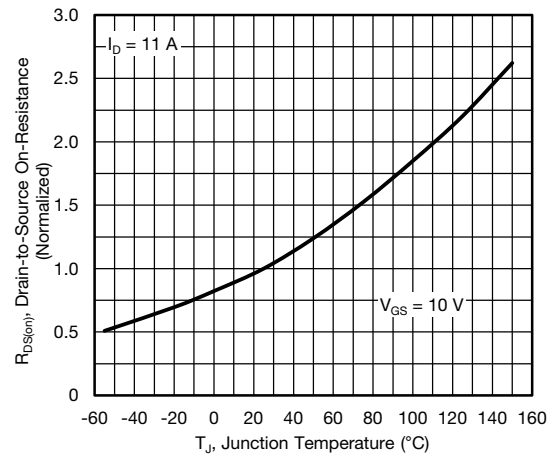
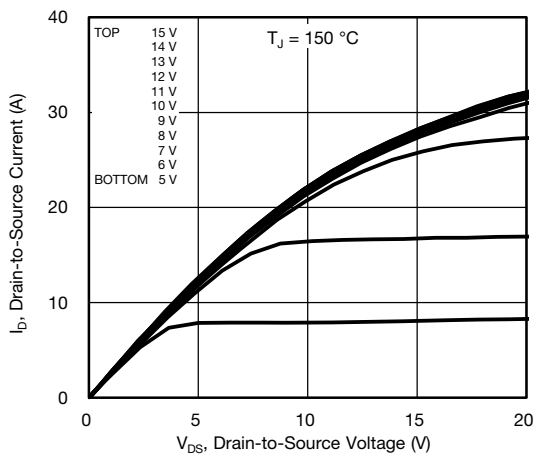
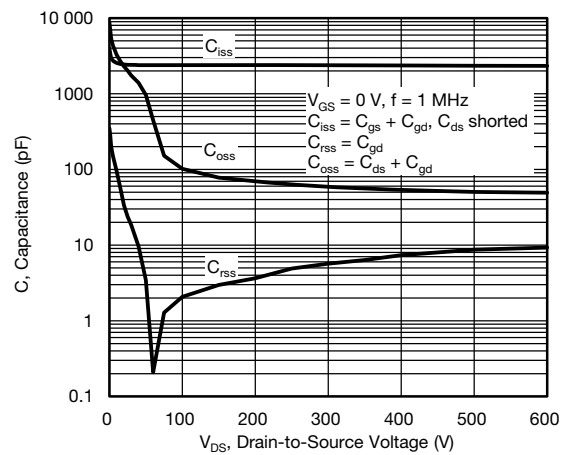
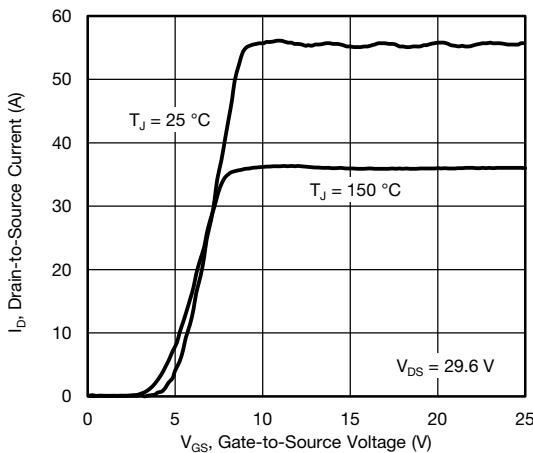
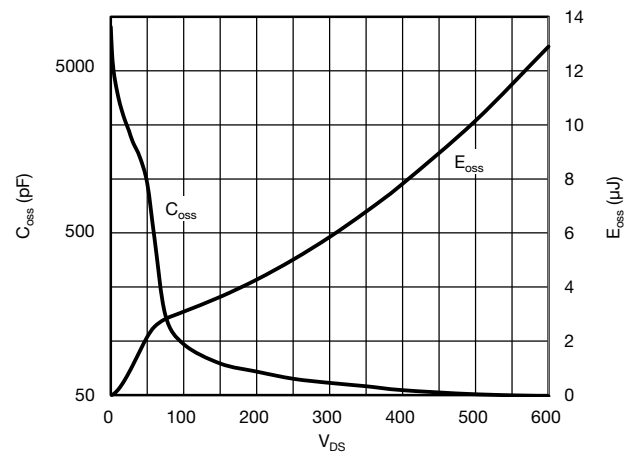


THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	39	51	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	0.51	0.68	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.81	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	25	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A	-	0.148	0.170	Ω
Forward Transconductance	g _{fs}	V _{DS} = 30 V, I _D = 11 A		-	8.5	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	2404	-	pF
Output Capacitance	C _{oss}			-	102	-	
Reverse Transfer Capacitance	C _{rss}			-	2	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}			-	75	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	314	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 11 A, V _{DS} = 520 V	-	66	99	nC
Gate-Source Charge	Q _{gs}			-	16	-	
Gate-Drain Charge	Q _{gd}			-	28	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 520 V, I _D = 11 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	26	52	ns
Rise Time	t _r			-	46	92	
Turn-Off Delay Time	t _{d(off)}			-	69	104	
Fall Time	t _f			-	44	88	
Gate Input Resistance	R _g			f = 1 MHz, open drain		0.27	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20.3	A
Pulsed Diode Forward Current	I _{SM}			-	-	53	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 11 A, V _{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 11 A, dI/dt = 100 A/μs, V _R = 25 V		-	396	792	ns
Reverse Recovery Charge	Q _{rr}			-	6.2	12.4	μC
Reverse Recovery Current	I _{RRM}			-	26	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Coss and Eoss vs. Vds

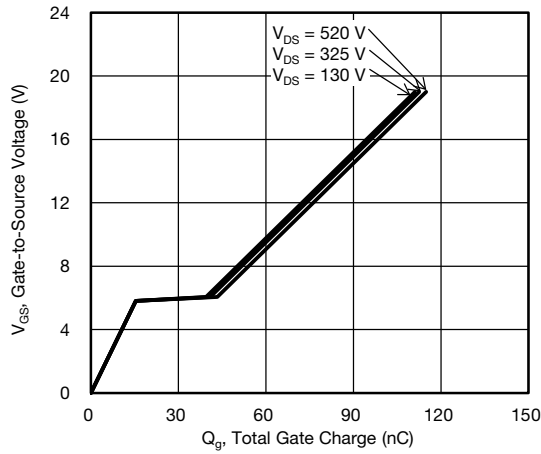


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

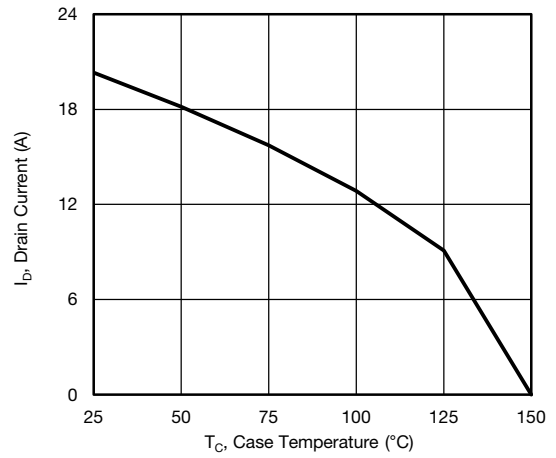


Fig. 10 - Maximum Drain Current vs. Case Temperature

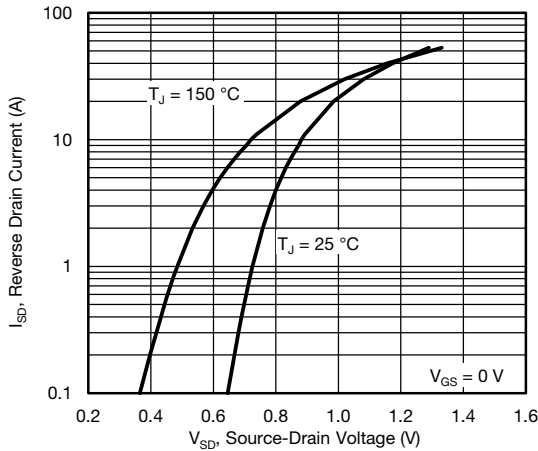


Fig. 8 - Typical Source-Drain Diode Forward Voltage

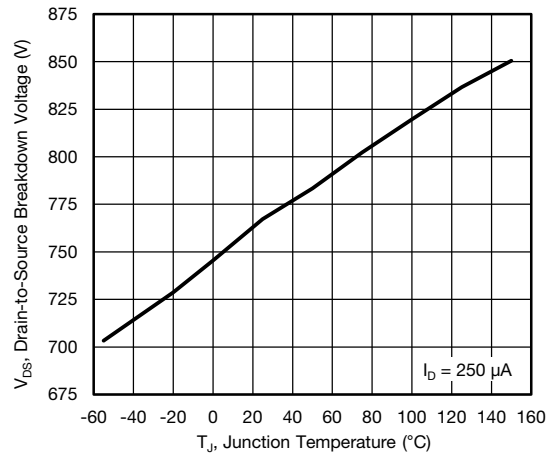


Fig. 11 - Temperature vs. Drain-to-Source Voltage

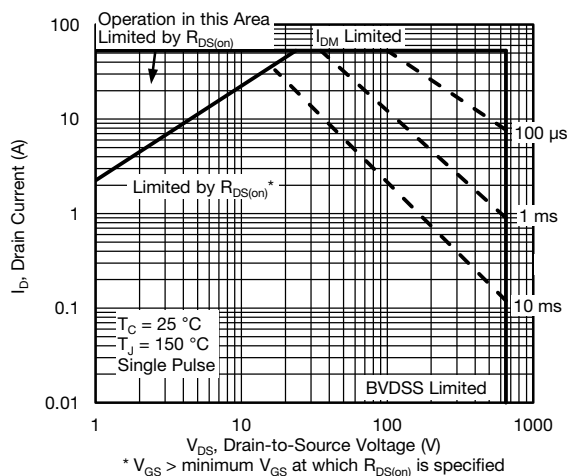


Fig. 9 - Maximum Safe Operating Area

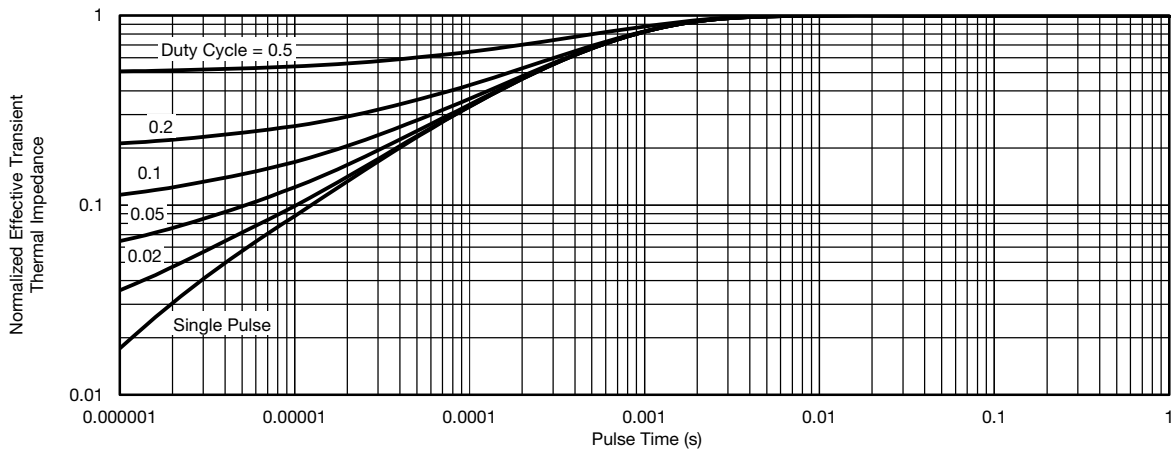


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

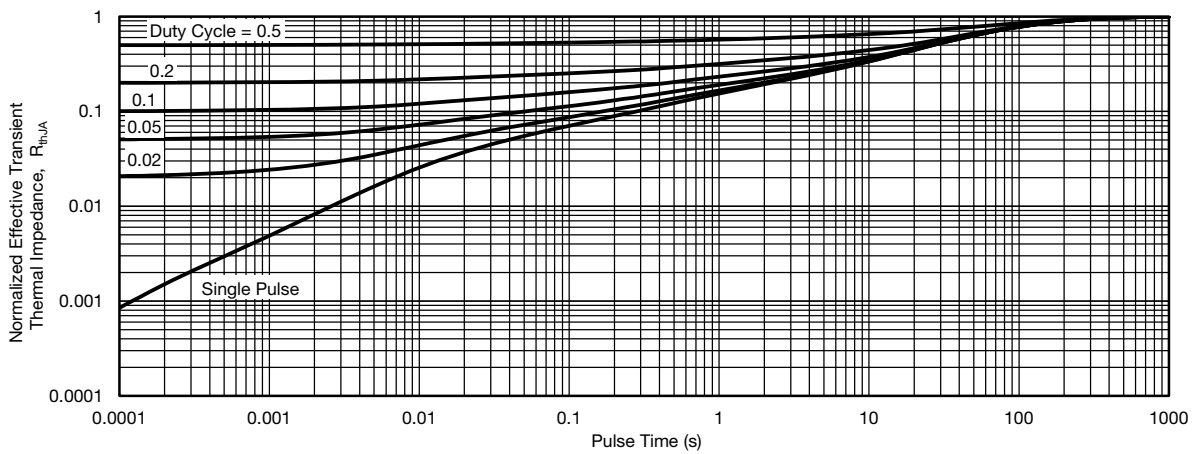


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

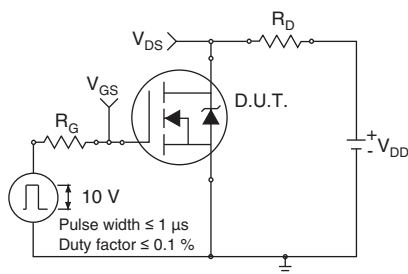


Fig. 14 - Switching Time Test Circuit

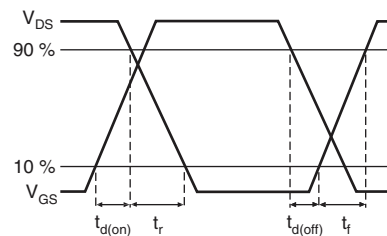


Fig. 15 - Switching Time Waveforms



Fig. 16 - Unclamped Inductive Test Circuit

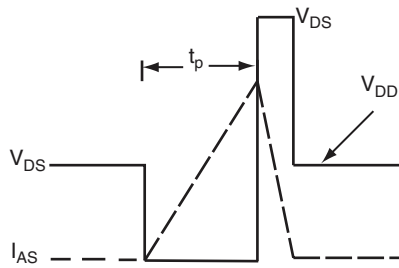


Fig. 17 - Unclamped Inductive Waveforms

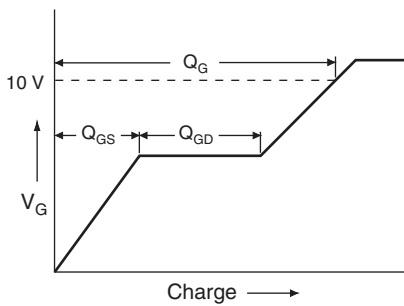


Fig. 18 - Basic Gate Charge Waveform

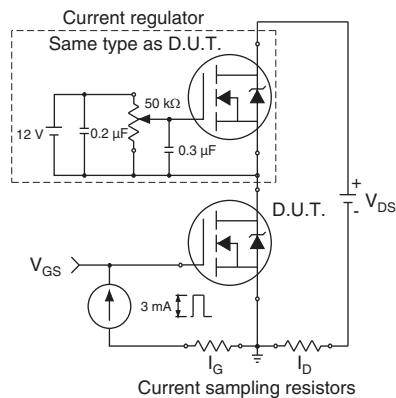
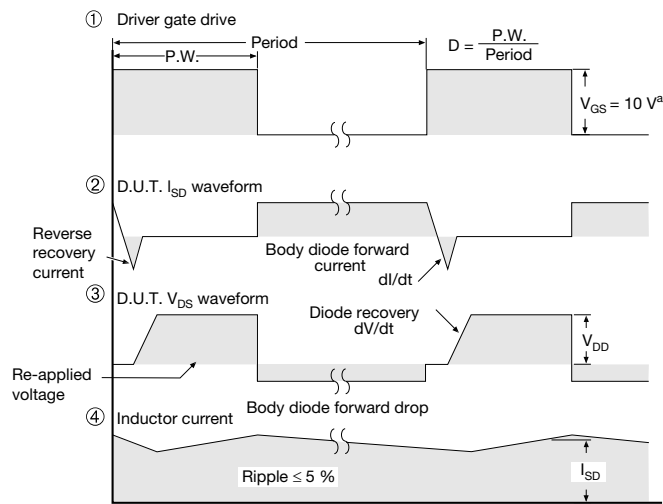
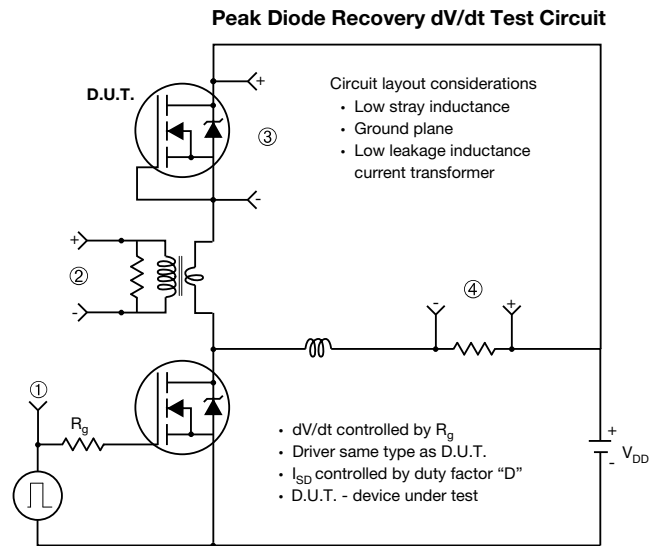


Fig. 19 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 20 - For N-Channel

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PowerPAK® 8 x 8 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N ⁽³⁾	8			8		

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M - 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

ECN: E20-0518-Rev. B, 28-Sep-2020
 DWG: 6041



Recommended Minimum PADs for PowerPAK[®] 8 mm x 8 mm



Dimensions in millimeters



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