Vishay Siliconix

## **D Series Power MOSFET**

### **DESCRIPTION**

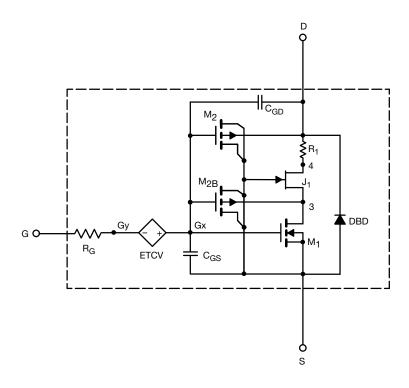
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



# **SPICE Device Model SiHG460B**

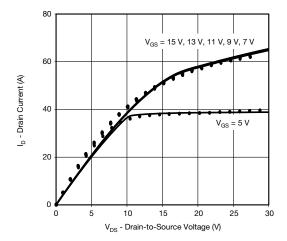
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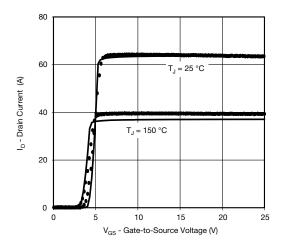
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	3	-	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	0.23	0.20	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 10 A	26	12	S
Dynamic					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	4270	3094	pF
Output Capacitance	C <sub>oss</sub>		161	152	
Reverse Transfer Capacitance	C <sub>rss</sub>		14	13	
Total Gate Charge	$Q_g$	$V_{DS} = 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	80	85	nC
Gate-Source Charge	Q <sub>gs</sub>		14	14	
Gate-Drain Charge	$Q_{gd}$		28	28	
Drain-Source Body Diode Characteristics					
Diode Forward Voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C},  I_S = 10  \text{A},  V_{GS} = 0  \text{V}$	0.9	-	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C},  I_F = I_S = 10  \text{A},  \\ dI/dt = 100  \text{A/} \mu \text{s},  V_R = 20  \text{V}$	430	437	ns
Reverse Recovery Charge	Q <sub>rr</sub>		6.3	5.9	μC

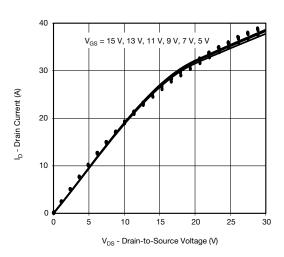
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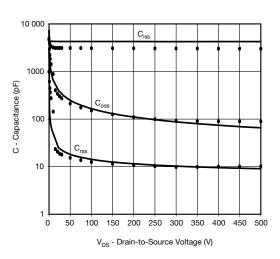
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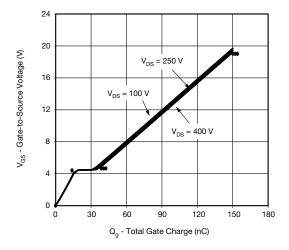
### COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)

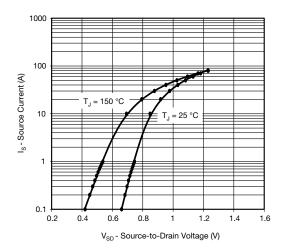












### Note

Dots and squares represent measured data.
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