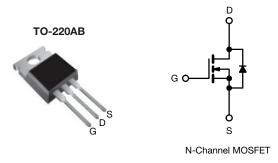
SiHP4N80E

Vishay Siliconix



E Series Power MOSFET



PRODUCT SUMMARY				
V_{DS} (V) at T_J max.	850			
R _{DS(on)} typ. (Ω) at 25 °C	$V_{GS} = 10 V$	1.1		
Q _g max. (nC)	32			
Q _{gs} (nC)	4			
Q _{gd} (nC)	6			
Configuration	Single			

FEATURES

- Low figure-of-merit (FOM) Ron x Qg
- Low input capacitance (Ciss)
- Reduced switching and conduction losses
- Ultra low gate charge (Qg)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	TO-220AB
Lood (Ph) free and hologon free	SiHP4N80E-BE3 ^a
Lead (Pb)-free and halogen-free	SiHP4N80E-GE3

Note

a. "-BE3" denotes alternate manufacturing location

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	800	- V	
Gate-source voltage			V _{GS}	± 30		
Continuous drain current (T _J = 150 $^{\circ}$ C)	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C		4.3		
	VGS at 10 V	T _C = 100 °C	I _D	2.7	А	
Pulsed drain current ^a			I _{DM}	11		
Linear derating factor				0.56	W/°C	
Single pulse avalanche energy ^b			E _{AS}	56	mJ	
Maximum power dissipation			PD	69	W	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C		
Drain-source voltage slope	T _J = 125 °C			70	1//20	
Reverse diode dv/dt ^d		dv/dt	0.3	V/ns		
Soldering recommendations (peak temperature) ^c	For 10 s			300	°C	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 2.0 A

c. 1.6 mm from case

d. $I_{SD} \leq I_D, \, di/dt$ = 100 A/µs, starting T_J = 25 $^\circ C$

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PARAMETER	SYMBOL	TYP.		MAX.	MAX.		UNIT		
Maximum junction-to-ambient	R _{thJA}	-		62					
Maximum junction-to-case (drain)	R _{thJC}	- 1.8				°C/W			
SPECIFICATIONS (T _J = 25 $^{\circ}$ C, u	unless otherw	ise noted)							
PARAMETER	SYMBOL	TES		ONS	MIN.	TYP.	MAX.	UNI	
Static					•		•		
Drain-source breakdown voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 25	60 μA	800	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I	_D = 1 mA	-	1.1	-	V/°0	
Gate-source threshold Voltage (N)	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 2	50 µA	2.0	-	4.0	V	
Cata aquiraa laakaga	1		$V_{GS} = \pm 20 V$ $V_{GS} = \pm 30 V$		-	-	± 100	nA	
Gate-source leakage	I _{GSS}				-	-	± 1	μA	
Zoro gato voltago drain ourront	lass	V _{DS} =	= 800 V, V _{GS}	= 0 V	-	-	1		
Zero gate voltage drain current	IDSS	V _{DS} = 640 \	$V_{DS} = 640 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$		-	-	10	μA	
Drain-source on-state resistance	R _{DS(on)}	$V_{GS} = 10 V$	V _{GS} = 10 V I _D = 2 A		-	1.1	1.27	Ω	
Forward transconductance	9 _{fs}	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 2 \text{ A}$		-	1.5	-	S		
Dynamic									
Input capacitance	C _{iss}	$V_{GS} = 0 V,$ $V_{DS} = 100 V,$ $f = 1 MHz$ $V_{DS} = 0 V \text{ to } 480 V, V_{GS} = 0 V$		-	622	-	pF		
Output capacitance	C _{oss}			-	34	-			
Reverse transfer capacitance	C _{rss}			-	5	-			
Effective output capacitance, energy related ^a	C _{o(er)}			-	21	-			
Effective output capacitance, time related ^b	C _{o(tr)}			-	91	-			
Total gate charge	Qg				-	16	32		
Gate-source charge	Q _{gs}	$V_{GS} = 10 V$ $I_D = 2 A, V_{DS} = 480 V$		-	4	-	nC		
Gate-drain charge	Q _{gd}			-	6	-			
Turn-on delay time	t _{d(on)}			-	12	24			
Rise time	t _r	Vpp	$V_{DD} = 480 \text{ V}, I_D = 2 \text{ A},$		-	7	14	ns	
Turn-off delay time	t _{d(off)}	$V_{GS} = 10 \text{ V}, \text{ R}_{g} = 9.1 \Omega$		-	26	52	115		
Fall time	t _f			-	20	40			
Gate input resistance	R _g	f = 1 MHz, open drain		0.6	1.2	2.4	Ω		
Drain-Source Body Diode Characteristi	cs								
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.4	- A		
Pulsed diode forward current	I _{SM}			-	-	11			
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 2 A, V _{GS} = 0 V		-	-	1.2	V		
Reverse recovery time	t _{rr}	$T_{J} = 25 \text{ °C, } I_{F} = I_{S} = 2 \text{ A,}$ di/dt = 100 A/ μ s, V _R = 25 V		-	248	496	ns		
Reverse recovery charge	Q _{rr}			_	1.4	2.8	μΟ		
Reverse recovery current	I _{RRM}			-	9.2	_	A		

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

b. Coss(tr) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 V to 480 V VDSS

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

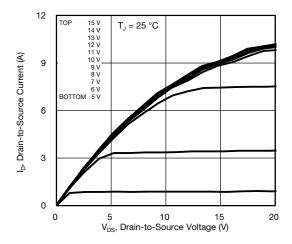
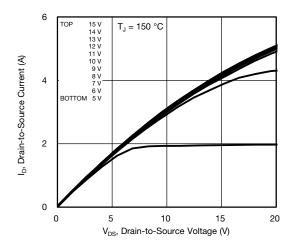


Fig. 1 - Typical Output Characteristics





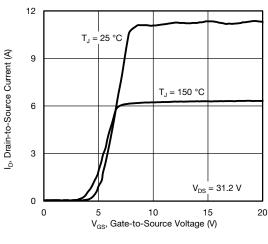


Fig. 3 - Typical Transfer Characteristics

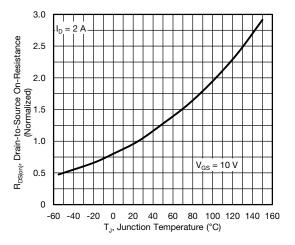


Fig. 4 - Normalized On-Resistance vs. Temperature

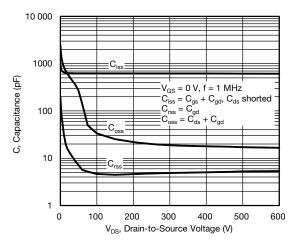


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

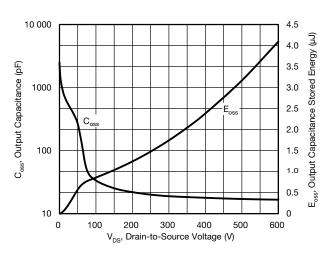


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

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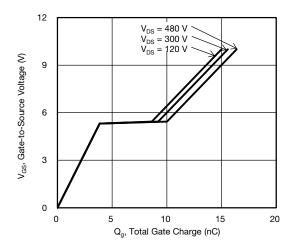


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

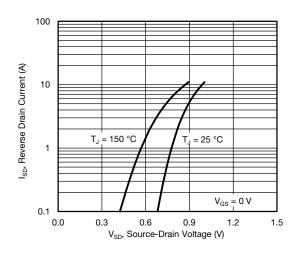


Fig. 8 - Typical Source-Drain Diode Forward Voltage

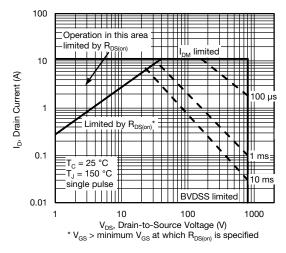


Fig. 9 - Maximum Safe Operating Area

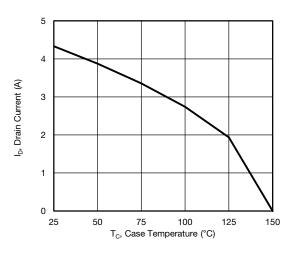


Fig. 10 - Maximum Drain Current vs. Case Temperature

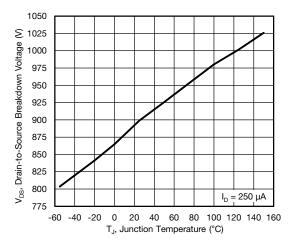
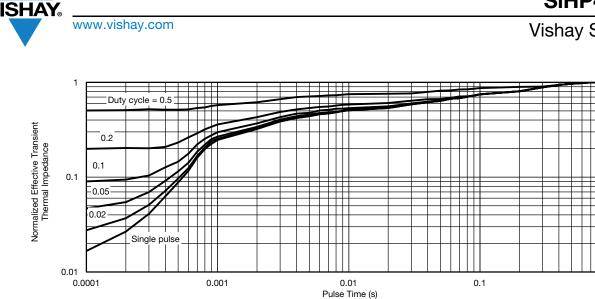


Fig. 11 - Temperature vs. Drain-to-Source Voltage

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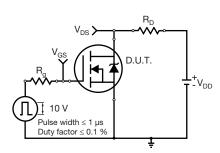


Fig. 13 - Switching Time Test Circuit

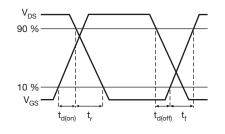


Fig. 14 - Switching Time Waveforms

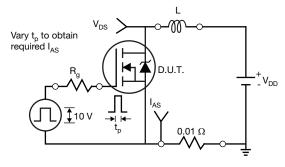


Fig. 15 - Unclamped Inductive Test Circuit

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 V_{DD} V_{DS} I_{AS}

Fig. 16 - Unclamped Inductive Waveforms

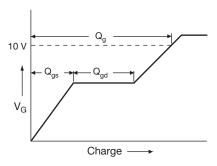
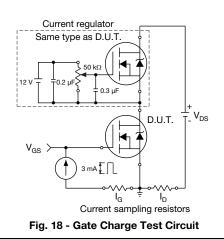


Fig. 17 - Basic Gate Charge Waveform



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Peak Diode Recovery dv/dt Test Circuit

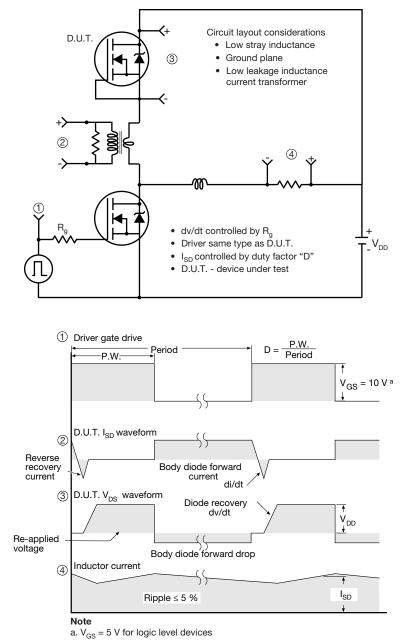


Fig. 19 - For N-Channel

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