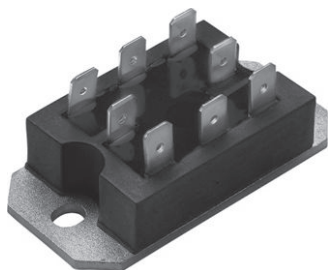



## Power Modules, Passivated Assembled Circuit Elements, 25 A



PACE-PAK (D-19)

### FEATURES

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200  $V_{RRM}/V_{DRM}$
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved 
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT

### DESCRIPTION

The VS-P100 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

### PRIMARY CHARACTERISTICS

$I_O$	25 A
Type	Modules - thyristor, standard
Package	PACE-PAK (D-19)

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_O$	85 °C	25	A
$I_{TSM}$	50 Hz	357	A
	60 Hz	375	
$I^2t$	50 Hz	637	A <sup>2</sup> s
	60 Hz	580	
$I^2\sqrt{t}$		6365	A <sup>2</sup> √s
$V_{DRM}, V_{RRM}$		400 to 1200	V
$V_{ISOL}$		2500	V
$T_J$	Range	-40 to +125	°C
$T_{Stg}$		-40 to +125	°C

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}$ MAXIMUM AT $T_J$ MAXIMUM mA
VS-P101, VS-P121, VS-P131	400	500	10
VS-P102, VS-P122, VS-P132	600	700	
VS-P103, VS-P123, VS-P133	800	900	
VS-P103, VS-P124, VS-P134	1000	1100	
VS-P105, VS-P125, VS-P135	1200	1300	



ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum DC output current at case temperature	I <sub>O</sub>	Full bridge			25	A
					85	°C
Maximum peak, one-cycle non-repetitive on-state or forward current	I <sub>TSM</sub> , I <sub>FSM</sub>	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T <sub>J</sub> = T <sub>J</sub> maximum	357	A
		t = 8.3 ms			375	
		t = 10 ms	100 % V <sub>RRM</sub> reapplied		300	
		t = 8.3 ms			315	
Maximum I <sup>2</sup> t for fusing	I <sup>2</sup> t	t = 10 ms	No voltage reapplied		637	A <sup>2</sup> s
		t = 8.3 ms			580	
		t = 10 ms	100 % V <sub>RRM</sub> reapplied		450	
		t = 8.3 ms			410	
Maximum I <sup>2</sup> √t for fusing	I <sup>2</sup> √t	t = 0.1 ms to 10 ms, no voltage reapplied I <sup>2</sup> t for time tx = I <sup>2</sup> √t · √tx			6365	A <sup>2</sup> √s
Maximum value of threshold voltage	V <sub>T(TO)</sub>	T <sub>J</sub> = 125 °C			0.82	V
Maximum level value of on-state slope resistance	r <sub>t1</sub>	T <sub>J</sub> = 125 °C, average power = V <sub>T(TO)</sub> × I <sub>T(AV)</sub> + r <sub>t</sub> + (I <sub>T(RMS)</sub> ) <sup>2</sup>			12	mΩ
Maximum on-state voltage drop	V <sub>TM</sub>	I <sub>TM</sub> = π × I <sub>T(AV)</sub>		T <sub>J</sub> = 25 °C	1.35	V
Maximum forward voltage drop	V <sub>FM</sub>	I <sub>FM</sub> = π × I <sub>F(AV)</sub>		T <sub>J</sub> = 25 °C	1.35	V
Maximum non-repetitive rate of rise of turned-on current	di/dt	T <sub>J</sub> = 125 °C from 0.67 V <sub>DRM</sub> I <sub>TM</sub> = π × I <sub>T(AV)</sub> , I <sub>g</sub> = 500 mA, t <sub>r</sub> < 0.5 μs, t <sub>p</sub> > 6 μs			200	A/μs
Maximum holding current	I <sub>H</sub>	T <sub>J</sub> = 25 °C anode supply = 6 V, resistive load, gate open			130	mA
Maximum latching current	I <sub>L</sub>	T <sub>J</sub> = 25 °C anode supply = 6 V, resistive load			250	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = 125\text{ °C}$ , exponential to 0.67 $V_{DRM}$ gate open			200 $V/\mu s$
Maximum peak reverse and off-state leakage current at $V_{RRM}, V_{DRM}$	$I_{RRM}, I_{DRM}$	$T_J = 125\text{ °C}$ , gate open circuit			10 mA
Maximum peak reverse leakage current	$I_{RRM}$	$T_J = 25\text{ °C}$			100 $\mu A$
RMS isolation voltage	$V_{ISOL}$	50 Hz, circuit to base, all terminals shorted, $T_J = 25\text{ °C}$ , $t = 1\text{ s}$			2500 V

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum peak gate power	P <sub>GM</sub>			8	W	
Maximum average gate power	P <sub>G(AV)</sub>			2		
Maximum peak gate current	I <sub>GM</sub>			2	A	
Maximum peak negative gate voltage	-V <sub>GM</sub>			10	V	
Maximum gate voltage required to trigger	V <sub>GT</sub>	T <sub>J</sub> = -40 °C	Anode supply = 6 V resistive load	3	V	
		T <sub>J</sub> = 25 °C		2		
		T <sub>J</sub> = 125 °C		1		
Maximum gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = -40 °C		90	mA	
		T <sub>J</sub> = 25 °C		60		
		T <sub>J</sub> = 125 °C		35		
Maximum gate voltage that will not trigger	V <sub>GD</sub>	T <sub>J</sub> = 125 °C, rated V <sub>DRM</sub> applied		0.2	V	
Maximum gate current that will not trigger	I <sub>GD</sub>			2	mA	

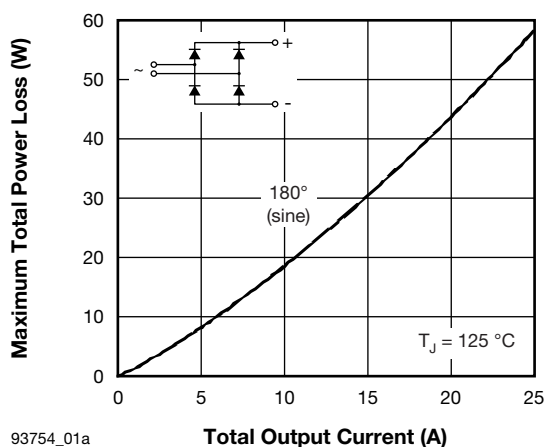


## THERMAL AND MECHANICAL SPECIFICATIONS

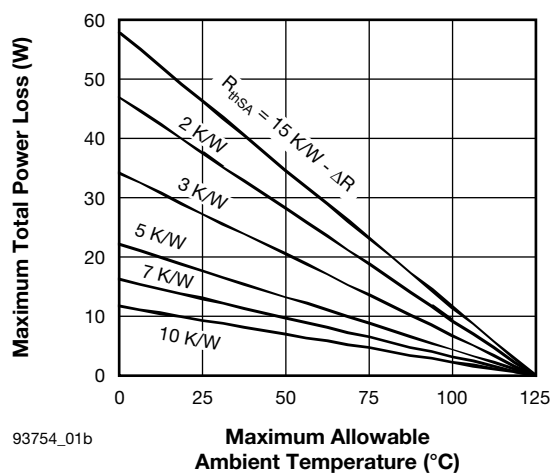
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating and storage temperature range	$T_J, T_{Stg}$		-40 to +125	°C
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	2.24	K/W
Maximum thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth and greased	0.10	
Mounting torque, base to heatsink <sup>(1)</sup>			4	Nm
Approximate weight			58	g
			2.0	oz.
Case style			PACE-PAK (D-19)	

### Note

(1) A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound

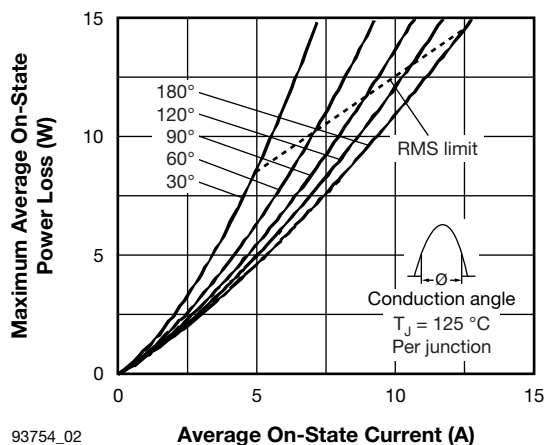


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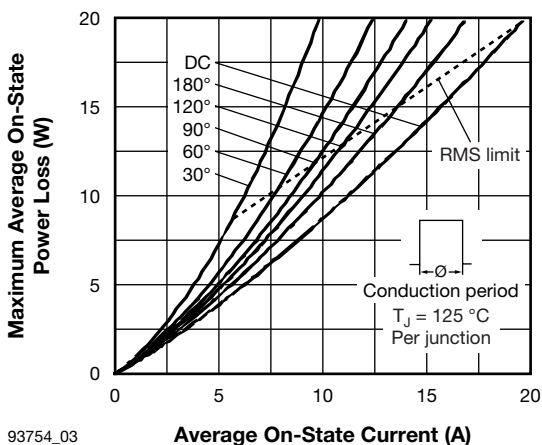
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Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)



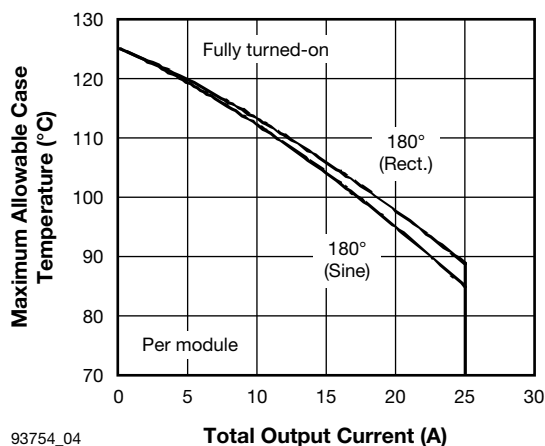
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Fig. 2 - On-State Power Loss Characteristics



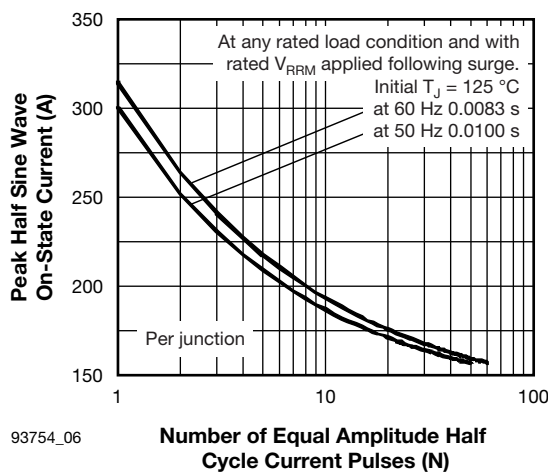
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Fig. 3 - On-State Power Loss Characteristics



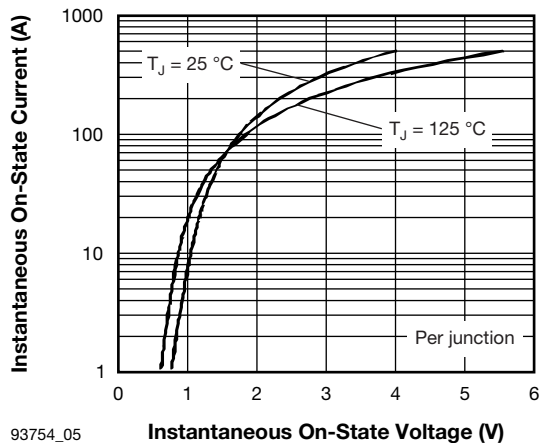
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Fig. 4 - Current Ratings Characteristics



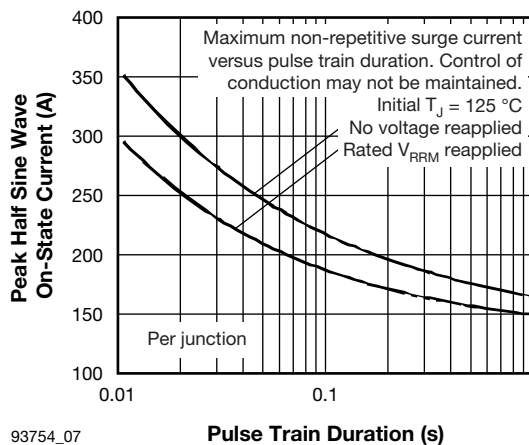
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Fig. 6 - Maximum Non-Repetitive Surge Current



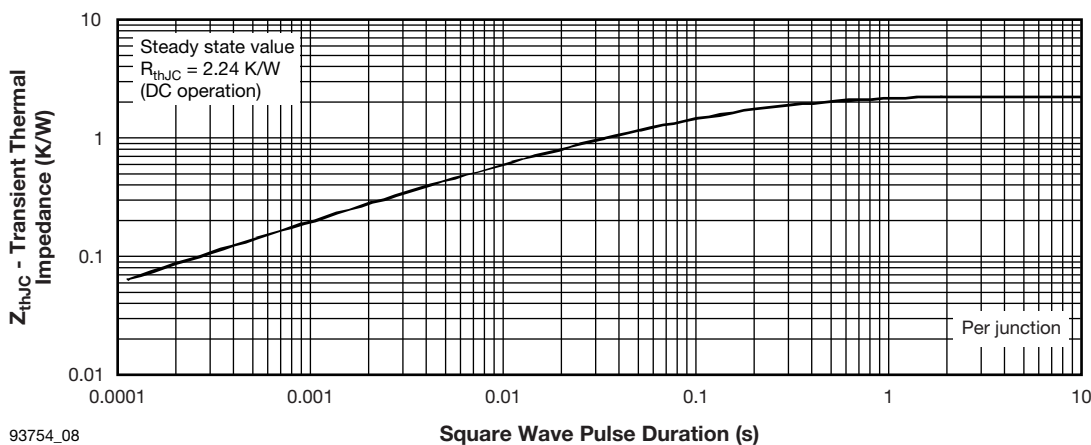
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Fig. 5 - On-State Voltage Drop Characteristics



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Fig. 7 - Maximum Non-Repetitive Surge Current



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Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

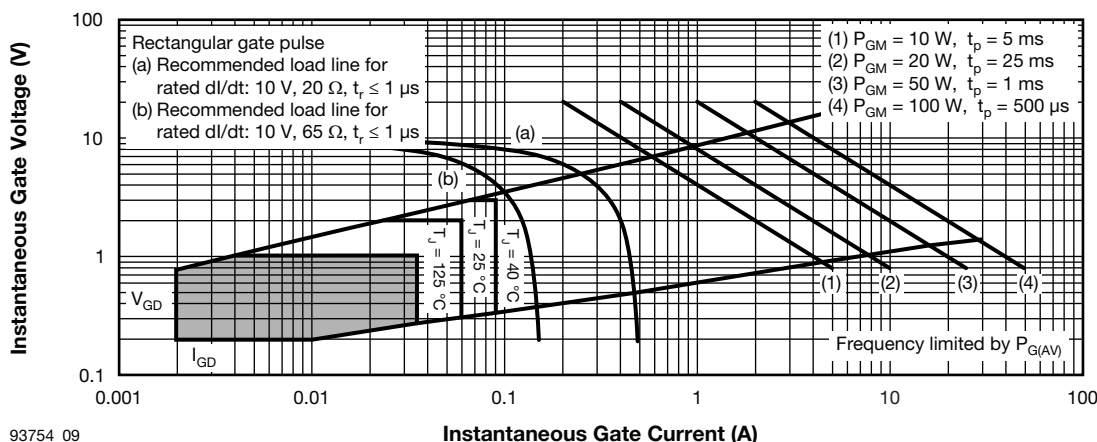


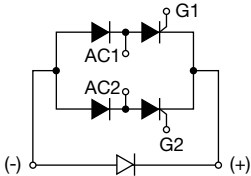
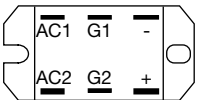
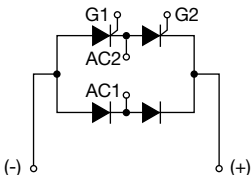
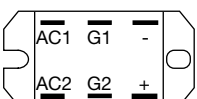
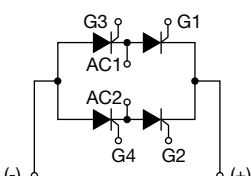
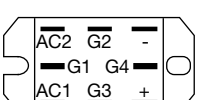
Fig. 9 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code

VS-	P	1	0	2	K	W
1	2	3	4	5	6	7

- 1** - Vishay Semiconductors product
- 2** - Module type
- 3** - Current rating  
1 = 25 A DC (P100 series)  
4 = 40 A DC (P400 series)
- 4** - Circuit configuration  
0 = single phase, hybrid bridge common cathode  
2 = single phase, hybrid bridge doubler connection  
3 = single phase, all SCR Bridge
- 5** - Voltage code  
1 = 400 V  
2 = 600 V  
3 = 800 V  
4 = 1000 V  
5 = 1200 V
- 6** - K = optional voltage suppression
- 7** - W = optional freewheeling diode

CIRCUIT CONFIGURATION			
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	SCHEMATIC DIAGRAM	TERMINAL POSITIONS
Single phase, hybrid bridge common cathode	0		
Single phase, hybrid bridge doubler connection	2		
Single phase, all SCR bridge	3		

CODING <sup>(1)</sup>					
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	BASIC SERIES	WITH VOLTAGE SUPPRESSION	WITH FREEWHEELING DIODE	WITH BOTH VOLTAGE SUPPRESSION AND FREEWHEELING DIODE
Single phase, hybrid bridge common cathode	0	P10.	P10.K	P10.W	P10.KW
Single phase, hybrid bridge doubler connection	2	P12.	P12.K	-	-
Single phase, all SCR bridge	3	P13.	P13.K	-	-

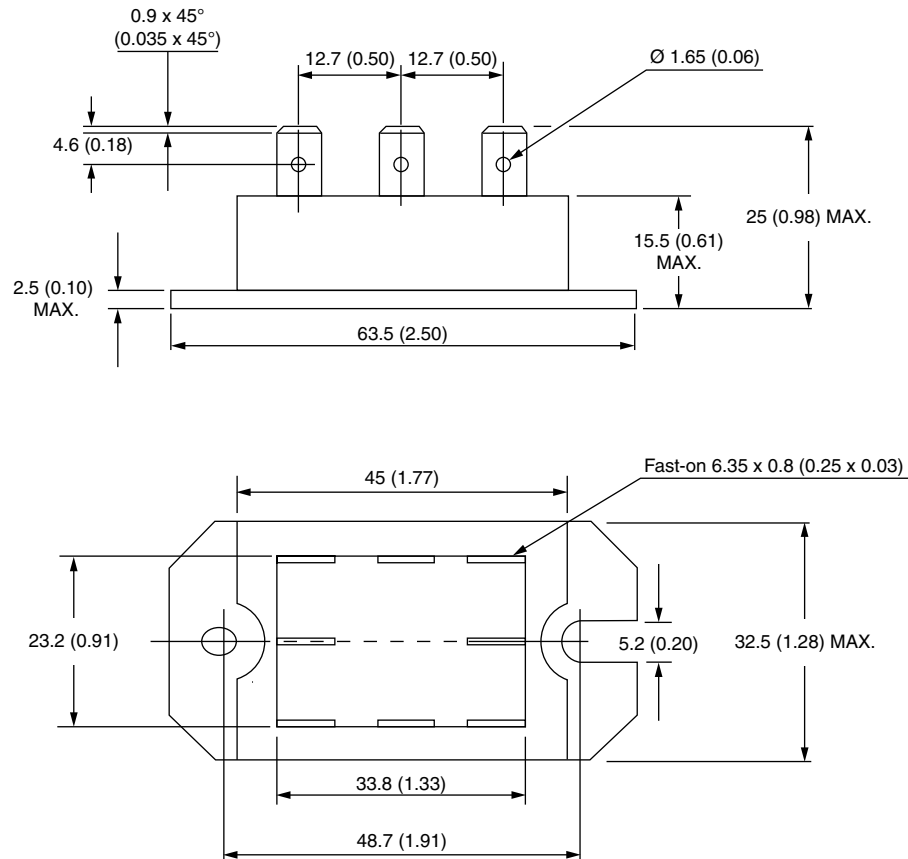
#### Note

<sup>(1)</sup> To complete code refer to Voltage Ratings table, i.e.: for 600 V P10.W complete code is P102W

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95335">www.vishay.com/doc?95335</a>

## D-19 PACE-PAK

**DIMENSIONS** in millimeters (inches)





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