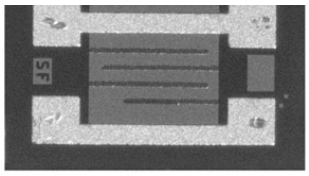
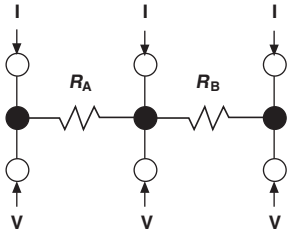
Thin Film, Center-Tapped Resistor Divider Network



Product may not be to scale

The CTA series resistor chips combine the best tolerances, stability and low shunt capacitance. The CTA offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTAs six bonding pads allows the user increased layout flexibility. The CTAs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTAs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.



FEATURES

- Wire bondable
- Center tap feature
- Tight ratio tolerances to: ± 0.1 %
- Chip size: 0.030" x 0.030"
- Case: 0303
- Resistance range total: 25 Ω to 35 kΩ
- Alumina substrate, low shunt capacitance: < 0.2 pF
- Resistor material nichrome
- Excellent stability: ± 0.025 % maximum Δ*R*/*R*
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

GREEN (5-2008)

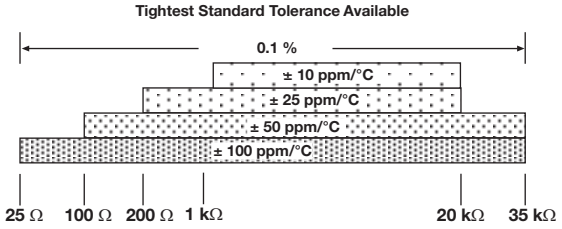
APPLICATIONS

The CTA center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, low shunt capacitance and tracking between two resistors is critical.

Recommended for hermetic environments where chip is not exposed to moisture.

For lower values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. Vishay EFI measures low-value resistors by the four-wire Kelvin technique. The measuring method is illustrated in the diagram to the right.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	**VALUE**	**UNIT**
Total Resistance Range	25 to 35K	Ω
Standard Tolerances	± 0.1	%
TCR	± 10, ± 25, ± 50, ± 100	ppm/°C

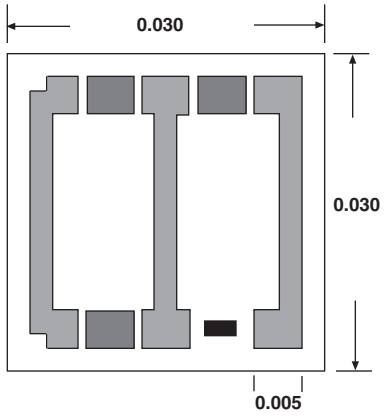


STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
TCR Tracking Between Halves (R_A/R_B)	± 2 (1)	ppm/°C
Center Tap Ratio, R_A/R_B: Tolerance	1 ± 1 standard	%
Noise, MIL-STD-202, Method 308	- 35 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106, (passivated only)	± 0.5 max. Δ*R*/*R*	%
Stability, 1000 h, + 125 °C, 62 mW	± 0.025 max. Δ*R*/*R*	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 max. Δ*R*/*R*	%
High Temperature Exposure, + 150 °C, 100 h	± 0.1 max. Δ*R*/*R*	%
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at + 70 °C (derated to zero at + 150 °C)	0.125 max.	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	+ 0.25 max. Δ*R*/*R*	%

Note

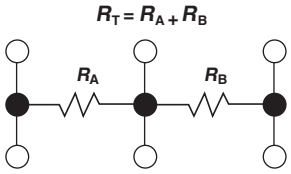
(1) 10 ppm/°C for *R* < 100

DIMENSIONS in inches



STANDARD CONFIGURATION
*Six locations. All pads 0.005 x 0.005

SCHEMATIC



MECHANICAL SPECIFICATIONS	
PARAMETER	**VALUE**
Chip Size	0.030" x 0.030" ± 0.002" (0.762 mm x 0.762 mm ± 0.050 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	99.6 % alumina
Resistor Material	Nichrome
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm)
Number of Pads	6
Pad Material	25 kÅ minimum gold
Backing	None (Au optional)

GLOBAL PART NUMBER INFORMATION

Global Part Number: CTA50000BBKKGNHWS

Global Part Number Description: CTA 5K 0.1 % RT 0.1 % ± 100 ppm/°C ± 10 ppm/°C Au None H WS

C	T	A	5	0	0	0	0	B	B	K	K	G	N	H	W	S

MODEL	RESISTANCE (*R* TOTAL)	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	RATIO TOL. (%)	TCR (ppm/°C)	TCR TRACK (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
CTA	First 4 digits are significant figures of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**B** = 0.1 **C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **J** = 5.0 **K** = 10.0	**B** = 0.1 **C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **U** = User **N** = No	**E** = ± 25 **C** = ± 50 **K** = ± 100	**G** = ± 2 **J** = ± 5 **K** = ± 10 **N** = No	**G** = Au **A** = Al	**G** = Au **N** = None	**H** = Class H **K** = Class K	**WS** = Waffle pack 100 min., 1 mult

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