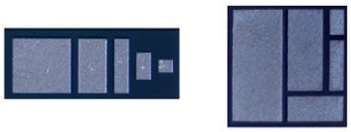
Thin Film Binary MOS Capacitors



Product may not be to scale

The CBB and CBC MOS capacitor chips each contain five different capacitors in binary increments allowing the user many choices in value selection.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBB and CBCs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032, class H or K.

FEATURES

- Wire bondable
- User value selection
- Five capacitors on a 0.019" x 0.048" (CBB) or 0.044" x 0.044" (CBC) chip
- Case size: 0402, 0404
- Capacitance range: up to 93 pF in binary increments
- Dielectric: silicon dioxide
- Low dielectric loss
- Substrate: silicon with gold backing
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

APPLICATIONS

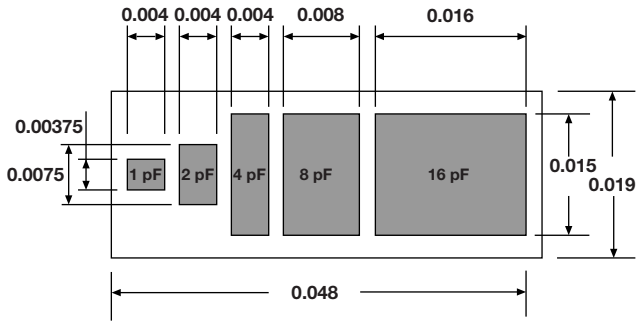
Vishay EFI CBB and CBC binary MOS multi-value capacitor chips are designed to be a useful device for trimming hybrid circuits by adding or subtracting capacitance, using normal wire-bonding techniques.

WV (DC) VALUES AND TOLERANCES			
CAPACITOR MODEL	**CBB**	**CBC**	**UNIT**
Case Size	0402	0404	
Total Capacitance	Up to 31	Up to 93	pF
Capacitance Values (31 pF / 93 pF)	1, 2, 4, 8, 16	3, 6, 12, 24, 48	pF
Tolerance	± 10	± 10	%
DC Working Voltage	75	75	V

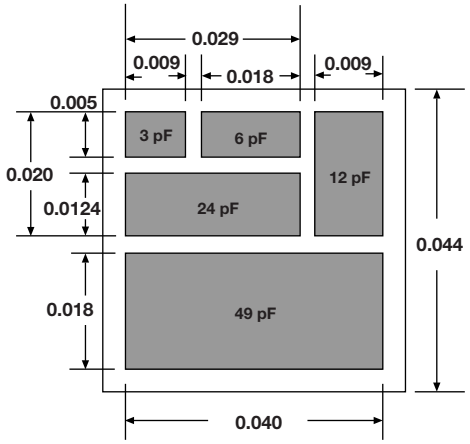
STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
Capacitance Range, CBB CBC	Up to 31 Up to 93	pF
Maximum Working Voltage	75	V
Peak Voltage at +25 °C	1.5 x working voltage	
Dissipation Factor, 1 kHz, 1 V_{RMS}, +25 °C	0.1 %	%
Q at 1 mHz, 50 mV_{RMS}, +25 °C	1000 min.	
TCC, -55 °C to +150 °C	+ 15 ± 25	ppm/°C
Insulation Resistance at Working Voltage, +25 °C	10^9 min.	Ω
Operating Temperature Range	-55 to +15	°C
Thermal Shock	± 0.25 + 0.25 pF max. ΔC/C	%
Moisture Resistance, MIL-STD-202, Method 106	± 1.0 + 0.25 pF max. ΔC/C	%
Short Time Overload, +25 °C, 5 s; 1.5 x Working Voltage	± 0.25 + 0.25 pF max. ΔC/C	%
High Temperature Exposure: 100 h at +150 °C Ambient	± 0.25 + 0.25 pF max.	%
Life, MIL-STD-202, Method 108, Condition D, +125 °C Ambient, 1000 h at Working Voltage	± 2.0 + 0.25 pF max. ΔC/C	%

CONFIGURATIONS in inches

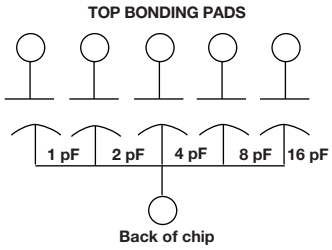
CBB

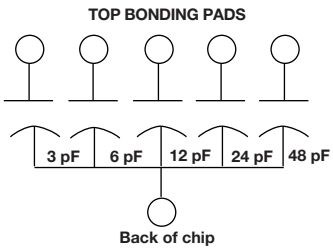


CBC



SCHEMATIC





MECHANICAL SPECIFICATIONS

PARAMETER	VALUE
Chip Size, CBB	0.019" x 0.048" ± 0.002" (0.48 mm x 1.2 mm ± 0.05 mm)
Chip Size, CBC	0.044" x 0.044" ± 0.002" (1.1 mm x 1.1 mm ± 0.05 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Semiconductor silicon
Dielectric	Silicon dioxide (MOS)
Bonding Pads	10 kÅ minimum aluminum (Au optional)
Backing	3 kÅ minimum gold

GLOBAL PART NUMBER INFORMATION

Global Part Number: CBB3100BLGKWS

Global Part Number Description: CBB 31 pF 25 % Au K WS

C	B	B	3	1	0	0	B	L	G	K	W	S

MODEL	SIZE	CAPACITANCE (pF)	CAPACITANCE MULTIPLIER CODE	TOLERANCE CODE	TERMINATION	VISUAL CLASS	PACKAGING CODE
CB Binary Capacitor	**B** = 19 x 48 **C** = 44 x 44	First 4 digits are significant figures of capacitance	**C** = 0.001 **B** = 0.01	**K** = 10 % **M** = 20 % **L** = 25 %	**G** = Au **A** = Al	**H** = class H **K** = class K	**WS** = Waffle pack, 100 min., 1 mult.

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