40 A VRPower® Integrated Power Stage

(Datasheet in Brief)

DESCRIPTION

The SiC544 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's 4.5 mm x 3.5 mm MLP package, SiC544 enables voltage regulator designs to deliver up to 40 A continuous current per phase.

The internal power MOSFETs utilize Vishay's state-of-the-art Gen IV TrenchFET® technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC544 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V PWM logic.

A user selectable diode emulation mode (ZCD_EN#) is included to improve the light load performance. The device also supports PS4 mode to reduce power consumption when system operates in standby state.

FEATURES

- Thermally enhanced PowerPAK® MLP4535-22L package
- Vishay's Gen IV MOSFET technology and a low-side MOSFET with integrated Schottky diode
- Delivers up to 40 A continuous current
- High efficiency performance
- High frequency operation up to 2 MHz
- Power on reset
- 5 V PWM logic with tri-state and hold-off
- Supports PS4 mode light load requirement for IMVP8 with low shutdown supply current (5 V, 3 µA)
- Under voltage lockout
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-8 VRPower delivery
  - V_{CORE}, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$ Skylake, Kabylake platforms
  - V_{CCGI} for Apollo Lake platforms
- Up to 24 V rail input DC/DC VR modules

TYPICAL APPLICATION DIAGRAM

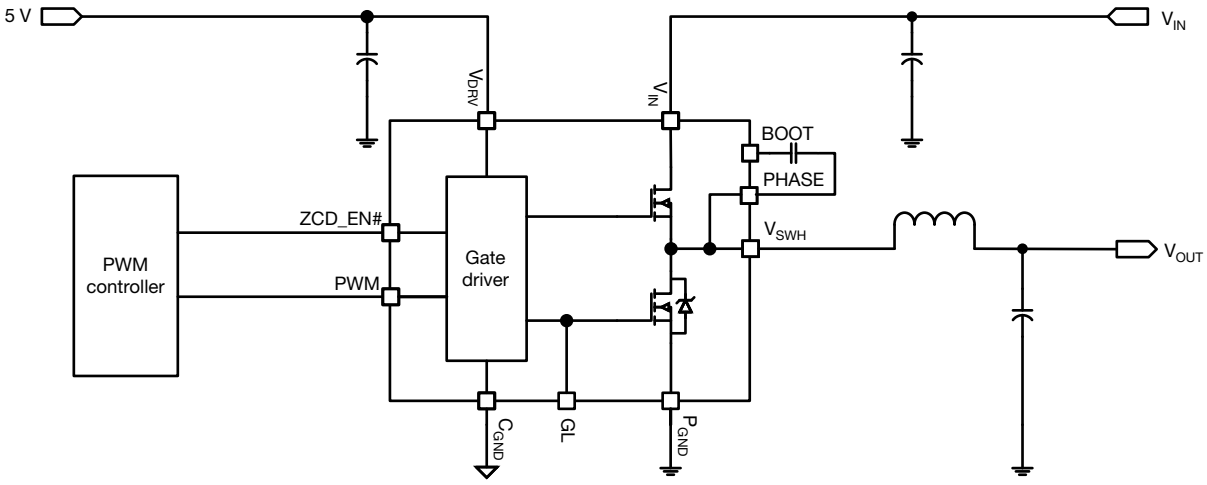

Fig. 1 - SiC544 Typical Application Diagram

PRODUCT SUMMARY	
Part number	SiC544
Description	40 A power stage, 4.5 V_{IN} to 24 V_{IN}, 5 V PWM with ZCD, PS4 mode
Input voltage min. (V)	4.5
Input voltage max. (V)	24
Continuous current rating max. (A)	40
Switch frequency max. (kHz)	2000
Enable (yes / no)	No
Monitoring features	-
Protection	UVLO
Light load mode	ZCD, PS4
Pulse-width modulation (V)	5
Package type	PowerPAK MLP4535-22L
Package size (W, L, H) (mm)	4.5 x 3.5 x 0.75
Status code	2
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

To request the full version of the datasheet, please contact: ICmarketing@vishay.com

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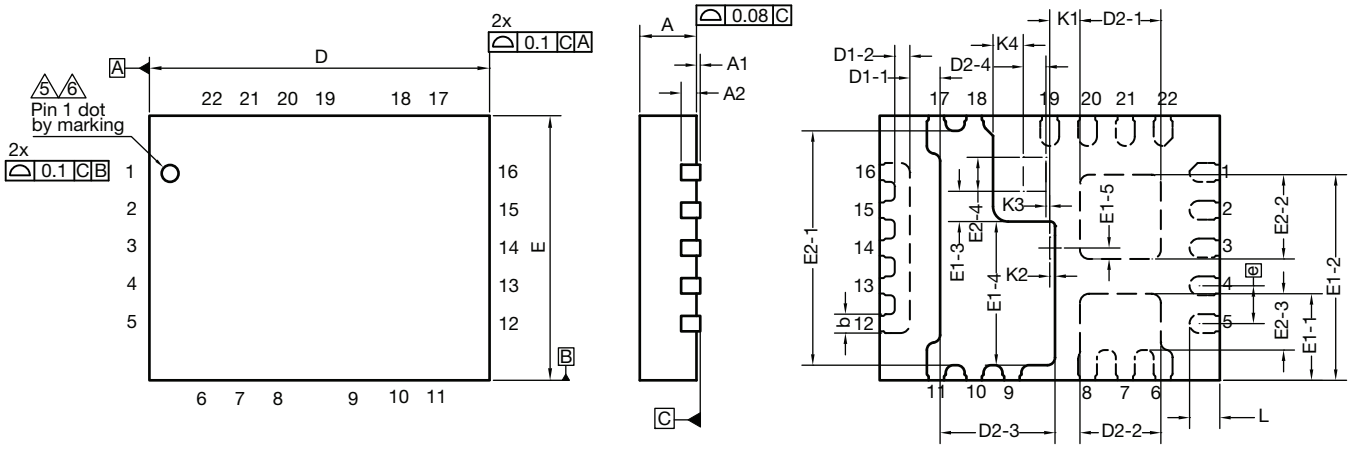
MLP 4.5 x 3.5-22L BWL Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.0029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.0078	0.0098	0.0110
D		4.50 BSC			0.177 BSC	
e		0.50 BSC			0.019 BSC	
E		3.50 BSC			0.137 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		22			22	
Nd (3)		6			6	
Ne (3)		5			5	
D1-1	0.35	0.40	0.45	0.013	0.015	0.017
D1-2	0.15	0.20	0.25	0.005	0.007	0.009
D2-1	1.02	1.07	1.12	0.040	0.042	0.044
D2-2	1.02	1.07	1.12	0.040	0.042	0.044
D2-3	1.47	1.52	1.57	0.057	0.059	0.061
D2-4	0.25	0.30	0.35	0.009	0.011	0.013
E1-1	1.095	1.145	1.195	0.043	0.045	0.047
E1-2	2.67	2.72	2.77	0.105	0.107	0.109
E1-3	0.35	0.40	0.45	0.013	0.015	0.017
E1-4	1.85	1.90	1.95	0.072	0.074	0.076
E1-5	0.095	0.145	0.195	0.0037	0.0057	0.0076
E2-1	3.05	3.10	3.15	0.120	0.122	0.124
E2-2	1.065	1.115	1.165	0.0419	0.0438	0.0458
E2-3	0.695	0.745	0.795	0.027	0.029	0.031
E2-4	0.40	0.45	0.50	0.015	0.017	0.019
K1		0.40 BSC			0.015 BSC	
K2		0.07 BSC			0.002 BSC	
K3		0.05 BSC			0.001 BSC	
K4		0.40 BSC			0.015 BSC	

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals,
   Nd is the number of terminals in X-direction and
   Ne is the number of terminals in Y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

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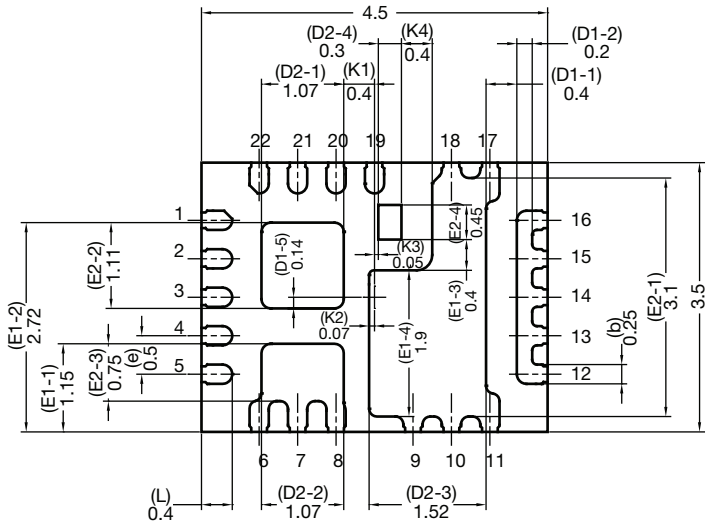
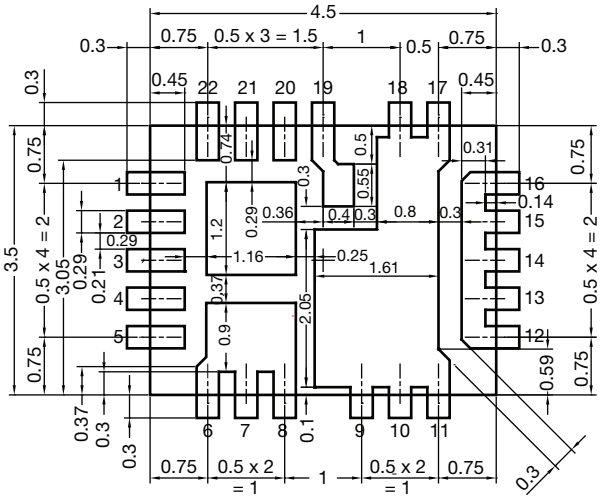
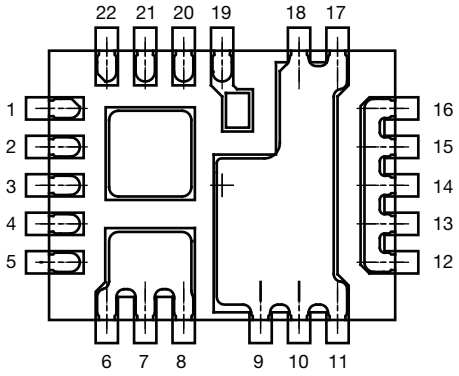
Recommended Land Pattern PowerPAK® MLP4535-22L

Package outline top view, transparent
(not bottom view)



Land pattern





All dimensions in millimeters

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