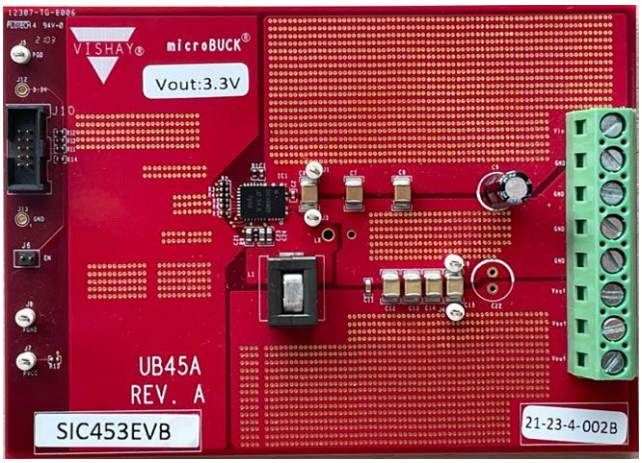
Reference Board User's Manual
Synchronous Buck Regulators: 4.5 V to 20 V
SiC450 (40 A), SiC451 (25 A), SiC453 (15 A) With PMBus



DESCRIPTION

The SiC450/1/3 is a PMBus 1.3 compliant non-isolated DC/DC buck regulator with integrated MOSFETs in a 5 mm x 7 mm thermally efficient package. It is capable of supplying 40 A (SiC450), 25 A (SiC451) and 15 A (SiC453) continuous output current. Its output voltage is digitally adjustable from 0.3 V to 12 V from a 4.5 V to 20 V input with switching frequencies up to 1.5 MHz. The SiC450/1/3 can accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial. SiC450/1/3's voltage mode constant ON time architecture delivers ultrafast transient response with minimum output capacitance and tight regulation over a broad load range. The device has integrated internal compensation and is stable with any type of output capacitor. The device incorporates a power saving scheme that significantly increases light load efficiency. The SiC450/1/3 allows power block configuration programs to be stored in nonvolatile memory (NVM). Operation parameters such as V_{OUT}, I_{OUT}, over temperature etc. can all be locally stored and used to determine fault behavior. Operation is firmware based and is field upgradable. The SiC450/1/3 is available in lead (Pb)-free power enhanced MLP 5 mm x 7 mm package. A full featured GUI and interface board is available to program and facilitate development of SiC450/1/3 based systems.

FEATURES

- Versatile
  - Single supply operation from 4.5 V to 20 V input voltage
  - Scalable solution with continuous output current of 40 A (SiC450), 25 A (SiC451), 15 A (SiC453)
  - Adjustable output voltage from 0.3 V to 12 V
  - Built in 5 V regulator for internal circuits and driver supply
  - 1 % output voltage accuracy over temperature
  - 0.5 % output accuracy at V_{OUT} = 3.3 V / 1.8 V, T_A = 25 °C
  - Ultrafast transient response
- Highly efficient
  - 98 % peak efficiency
  - Optional power save mode
- Highly configurable
  - PMBus 1.3 compliant with 1 MHz bus speed
  - Internal NVM
  - V_{OUT} adjustable with reading resolution of 2 mV
  - Supports over 50 PMBus commands
  - Supports in phase or 180° out of phase synchronization
  - Output voltage source and sink capability
- Robust and reliable
  - P_{VIN}, V_{OUT}, I_{IN} and I_{OUT} and temperature reporting
  - Over current protection in pulse-by-pulse mode
  - Output over and under voltage protection
  - Over temperature protection with hysteresis
  - Differential output remote sensing

APPLICATIONS

- Servers
- Networking, telecom, storage applications
- Ultrabook, notebook, desktop
- Distributed point of load power architectures
- Storage applications
- DDR memory

ORDERING TABLE

PART NUMBER	INPUT VOLTAGE	CURRENT RATING	EVAL BOARD PART NUMBER	EVB-KIT PART NUMBER	DONGLE PART NUMBER
SiC450ED-T1-GE3	4.5 V to 20 V	40 A	SiC450EVB-A	SiC450EVB-KIT-A	SiC400-DGL-01
SiC451ED-T1-GE3		25 A	SiC451EVB-A	SiC451EVB-KIT-A	
SiC453ED-T1-GE3		15 A	SiC453EVB-A	SiC453EVB-KIT-A	

SPECIFICATIONS

This reference board allows the end user to evaluate the SiC450/1/3 family device for its features and functionalities. It can also be served as a reference design for a user's application.

CONNECTION AND SIGNAL / TEST POINTS

This reference board is measured 97 mm x 69 mm and consists of all the components and connectors required as an reference board.

CONNECTOR J2

This is the connector for input voltage connection (V_{IN}, and the GND next to V_{IN}) and output voltage connection (3 V_{OUT}'s and 3 GND's).

J7 (PVCC) and J8 (PGND)

Device external drive voltage (5 V) supply pair.

CONNECTOR J10

This connector provides PMBus communication between this reference board and a dongle device through a 10 - pin flex cable.

J6 (EN)

Device enable signal input pin. 5 V logic, active HIGH.

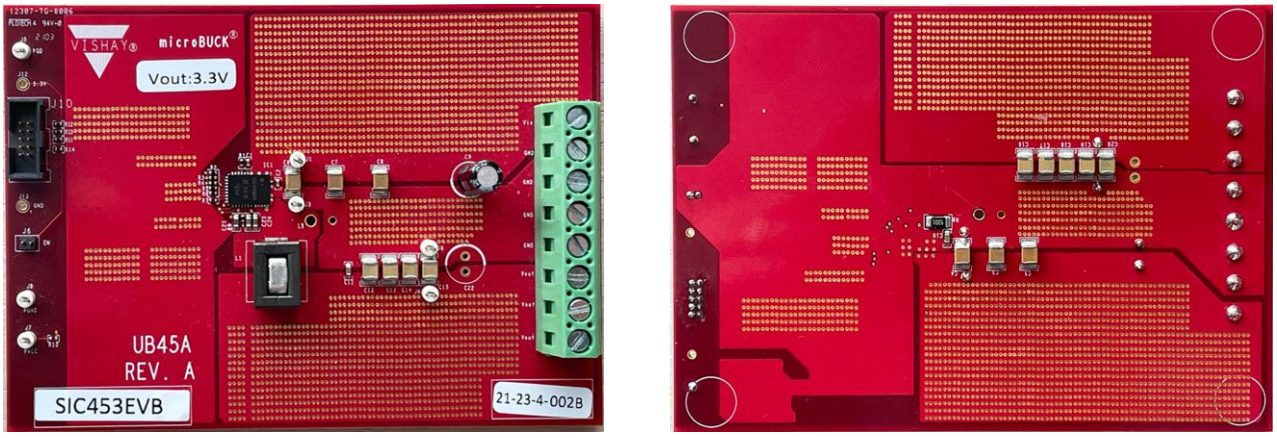


Fig. 1 - SiC450/1/3 EVB

SIGNALS AND TEST LEADS

Input Voltage Sense

J1 (V_{IN}) and J3 (V_{IN} Ground): Device input voltage check point for system efficiency and performance such as ripple in steady state and during load step.

Output Voltage Sense

J4 (V_{OUT}) and J9 (V_{OUT} Ground): Converter output voltage check point for system efficiency and performance such as ripple in steady state and during load step.

J11 (LX)

Switch node sense point for oscilloscope connection.

POWER GOOD INDICATOR

J5 (PG): Converter power good indicator. If a HIGH (5 V) is detected, the output voltage is within range (90 % - 115 % of set voltage); if a LOW (0 V) is detected, the output is out of range.

POWER UP PROCEDURE

There is no specific power sequence requirement to power up the board. The recommended power sequence is input voltage applied first and the enable signal.

Snubber Circuit

In some applications it may be needed to install an RC snubber from SW to GND if needed for EMC reduction purpose however this will slightly reduce efficiency. R8 and C10 are the place holders for the snubber, and the combination of 4 Ω and 1 nF is a reasonable staring point.

EVB KIT AND COMMUNICATION DONGLE

EVB KIT consists of the evaluation board, which has picture shown in Fig 1, dongle board and the cable connecting the two. The dongle board and cable are shown in Fig 2. Fig 3 shows the EVB KIT in a way the eval board is connected to the dongle board.

If only an eval board is needed, order using part number SiC45xEVB-A, where x stands for 0, 1 and 3; If only dongle is needed, order using part number, SiC400-DGL-01. If both are needed, order the EVB KIT with part number SiC45xEVB-KIT-A, where, again, x stands for 0, 1 and 3.

Fig. 2 - Dongle Board with Cable (Part number: SiC400-DGL-01) Front and Back View

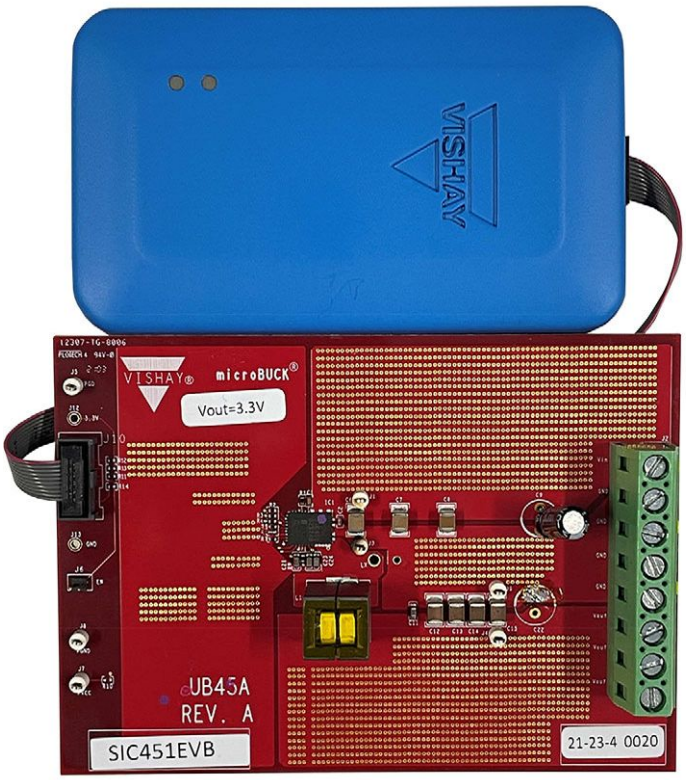
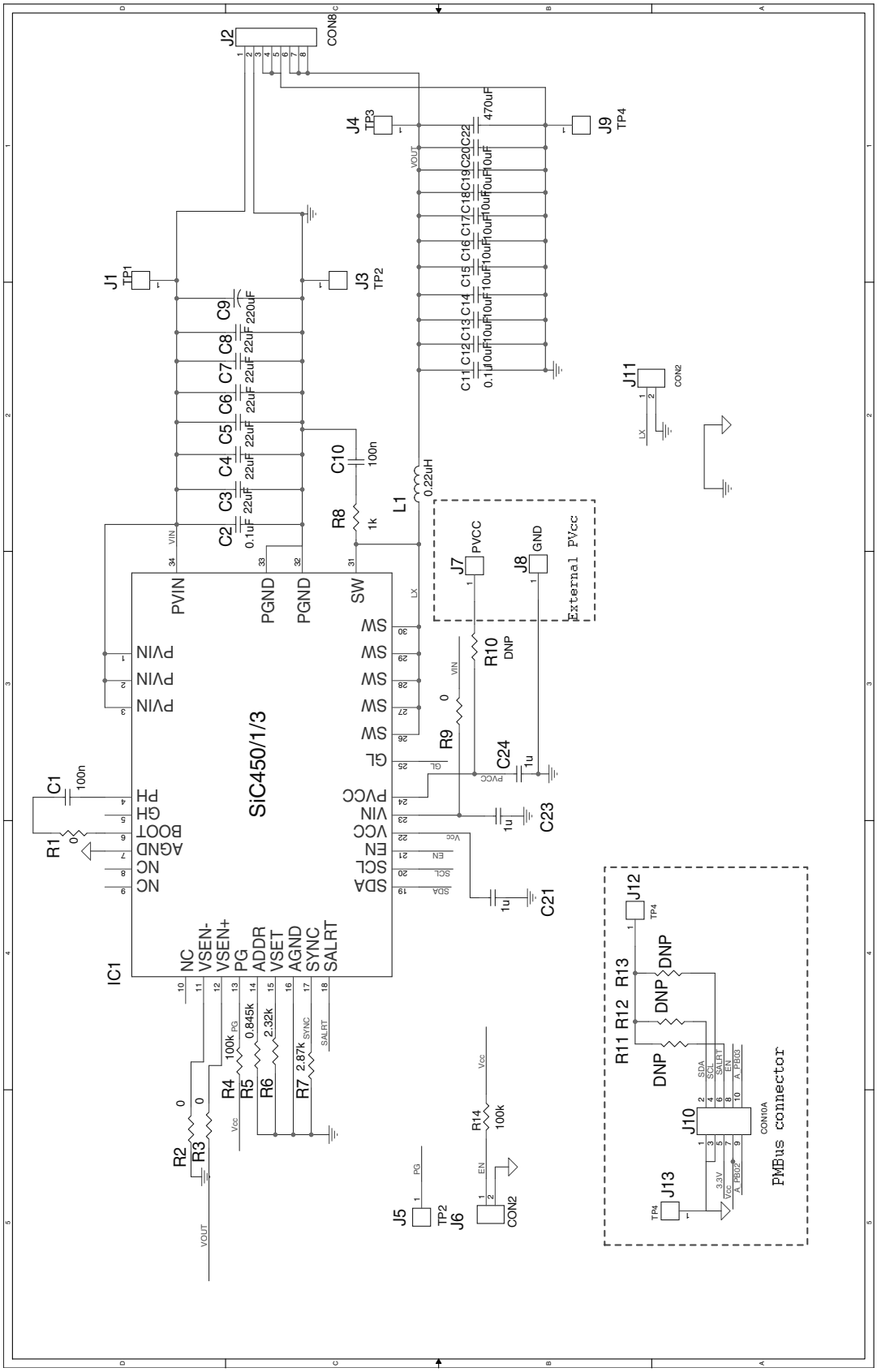


Fig. 3 - EVB Kit showing part number of SiC451EVB-KIT-A

SCHEMATIC FOR SiC450/1/3



PCB LAYOUT FOR SiC450/1/3

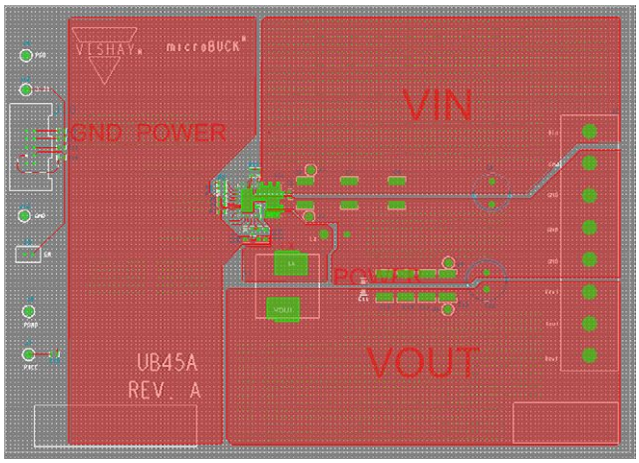


Fig. 4 - Top Layer

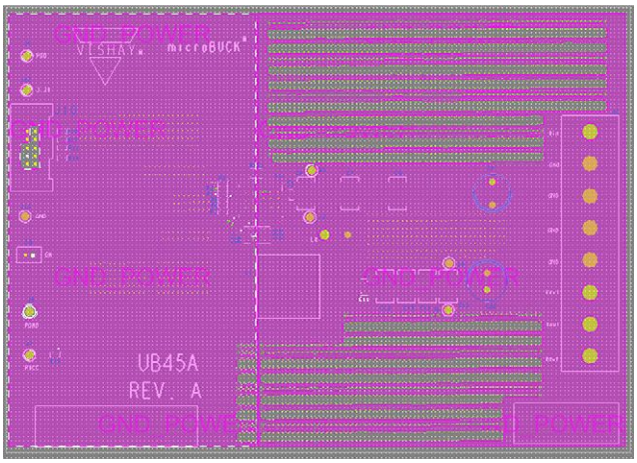


Fig. 7 - Inner Layer 3

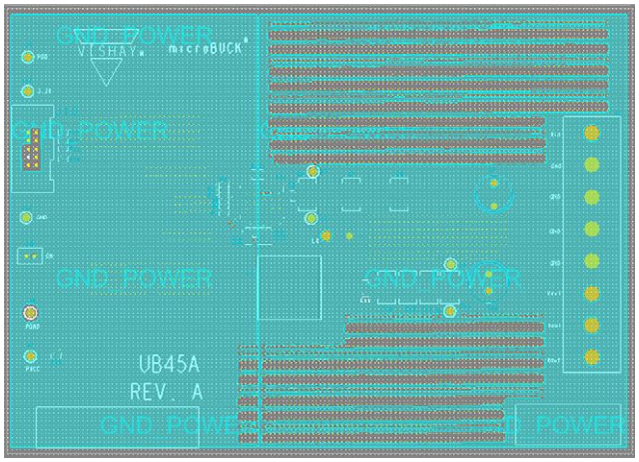


Fig. 5 - Inner Layer 1

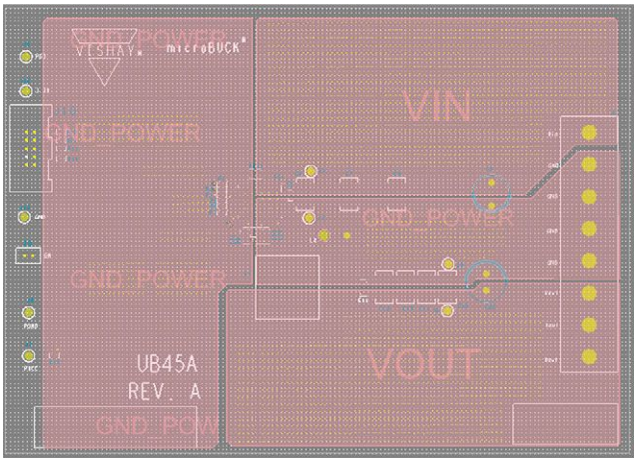


Fig. 8 - Inner Layer 4

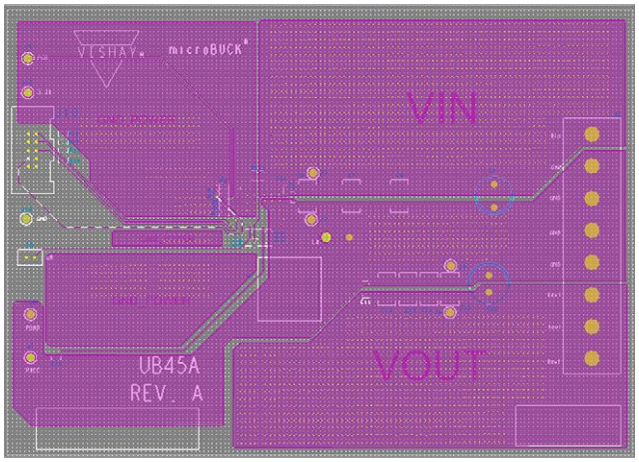


Fig. 6 - Inner Layer 2

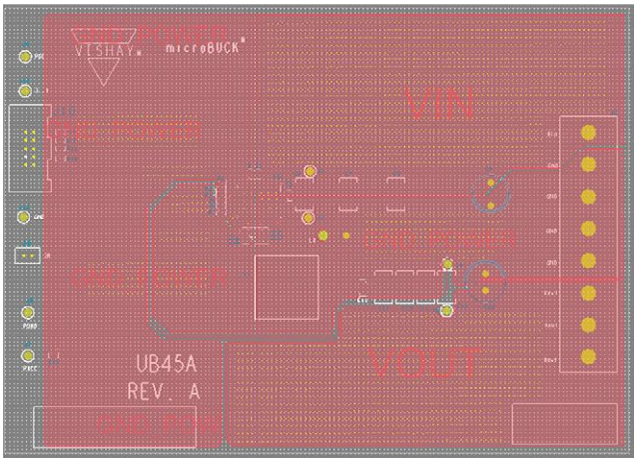


Fig. 9 - Inner Layer 5

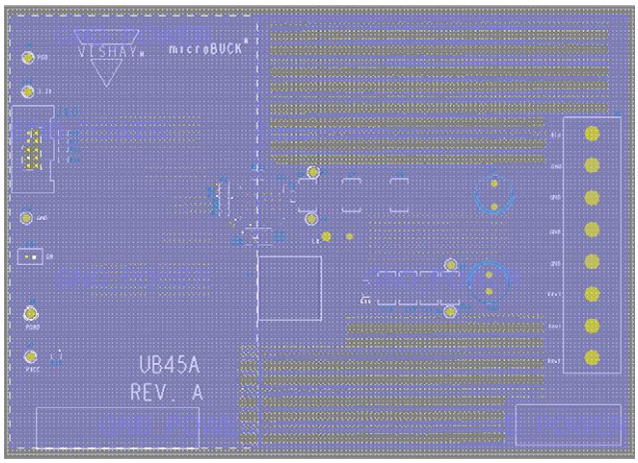


Fig. 10 - Inner Layer 6

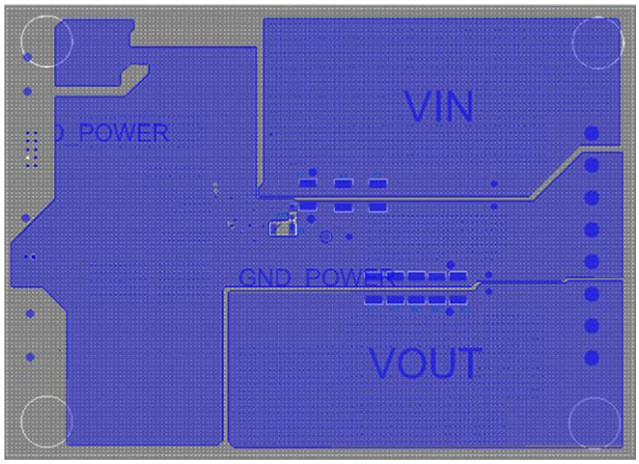


Fig. 11 - Bottom Layer

BILL OF MATERIAL REPORT, SiC450/1/3

SYM_NAME	COMP_DEVICE_TYPE	COMP_ VALUE	REFDES	USAGE		
				SiC450	SiC451	SiC453
C0402-TDK1	CAPACITORNON-POL_ C0402-TDK1_0.1u	0.1 µF	C1	-	-	-
C0402-TDK1	CAPACITOR NON-POL_ C0402-TDK1_0.1u	0.1 µF	C2	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_22U	22 µF	C3	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_22U	22 µF	C4	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_22U	22 µF	C5	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_22U	22 µF	C6	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_22U	22 µF	C7	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_22U	22 µF	C8	-	-	-
CAP_RAD	CAP_CAP_RAD_100UF	100 µF	C9	-	-	-
C0603-TDK1	CAPACITOR NON-POL_ C0603-TDK1_10	100n	C10	-	-	-
C0603-TDK1	CAPACITOR NON-POL_ C0603-TDK1_0.	0.1u	C11	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C12	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C13	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C14	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C15	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C16	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C17	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C18	-	-	-

BILL OF MATERIAL REPORT, SiC450/1/3						
SYM_NAME	COMP_DEVICE_TYPE	COMP_ VALUE	REFDES	USAGE		
				SiC450	SiC451	SiC453
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C19	-	-	-
C1210-TDK	CAPACITOR NON-POL_ C1210-TDK_100	100 µF	C20	-	-	-
C0603-TDK1	CAPACITOR NON-POL_ C0603-TDK1_1U	1 µF	C21	-	-	-
CAPR600	NP	NP	C22	-	-	-
C0603-TDK1	CAPACITOR NON-POL_ C0603-TDK1_1U	1 µF	C23	-	-	-
C0603-TDK1	CAPACITOR NON-POL_ C0603-TDK1_1U	1 µF	C24	-	-	-
SIC451A	SIC451_SIC451A_SIC451	SiC451	IC1	SiC450	SiC451	SiC453
TP30	CON1_TP30_TP1	TP1	J1	-	-	-
PHC8	CON8_PHC8_CON8	CON8	J2	-	-	-
TP30	CON1_TP30_TP2	TP2	J3	-	-	-
TP30	CON1_TP30_TP3	TP3	J4	-	-	-
TP30	CON1_TP30_TP2	TP2	J5	-	-	-
MINIJUMPER2	CON2_MINIJUMPER2_CON2	CON2	J6	-	-	-
TP30	CON1_TP30_PVCC	PVCC	J7	-	-	-
TP30	CON1_TP30_GND	GND	J8	-	-	-
TP30	CON1_TP30_TP4	TP4	J9	-	-	-
SWR6	CON6_SWR6_CON6	CON6	J10	-	-	-
2PROBE	CON2_2PROBE_CON2	CON2	J11	-	-	-
HCUVDE1	INDUCTOR_ HCUVDE1_0.47UH	0.47 µH	L1	ZPWE-101014MA-R47K	ZPWE-101014MA-R47K	ZPWE-107012NA-R47K
R0402-VISHAY1	R_R0402-VISHAY1_0	0	R1	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_0	0	R2	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_0	0	R3	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_100K	100K	R4	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_0.845K	0.845K	R5	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_ 2.87K;7.87K	2.87K; 7.87K	R6	2.87K for V_{OUT} = 1.05 V; 7.87K for V_{OUT} = 3.3 V	2.87K for V_{OUT} = 1.05 V; 7.87K for V_{OUT} = 3.3 V	2.87K for V_{OUT} = 1.05 V; 7.87K for V_{OUT} = 3.3 V
R0402-VISHAY1	R_R0402-VISHAY1_2.87K	2.87K	R7	-	-	-
R1206-VISHAY	R_R1206-VISHAY_1K	1k	R8	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_0	0	R9	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_DNP	DNP	R10	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_10K	10K	R11	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_10K	10K	R12	-	-	-
R0402-VISHAY1	R_R0402-VISHAY1_10K	10K	R13	-	-	-
R0402-VISHAY1	RESISTOR_ R0402-VISHAY1_100K	100K	R14	-	-	-

SCHEMATIC, DESIGN, BILL OF MATERIALS, AND GERBER FILES FOR PCB FABRICATION

These files are as follows and available for download at www.vishay.com/power-ics/list/product-74589/tab/designtools-ppg/

- "*.DSN" for schematic design file
- "*.DBK" for data backup file for Orcad
- ".opj" Orcad project file. Any schematic work should always be opened with the opj file. Use of a DSN file for this purpose is not advised
- "*.xlsx" is the bill of materials (BOM) derived from the schematic
- "*.PDF" is the PDF version of the schematic from the "*.DSN" file