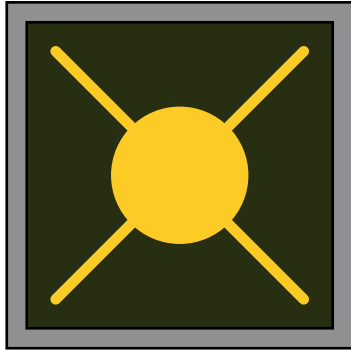


High Power IR Emitting Diode Chip



FEATURES

- Package type: chip
- Package form: single chip
- Technology: surface emitter
- Dimensions chip (L x W x H in mm): 0.260 x 0.260 x 0.170
- Peak wavelength: $\lambda = 855 \text{ nm}$
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

TSP8510VA is a high power infrared, 855 nm surface emitting diode in GaAIAs technology with high radiant power and high speed. Polarity configuration is “n-up”.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY

| COMPONENT | ϕ_e (mW) | ϕ (°) | λ_p (nm) | t_r (ns) |
|-----------|---------------|------------|------------------|------------|
| TSP8510VA | 19.5 | 55 | 855 | 25 |

Note

- Test condition see table “Basic Characteristics”

ORDERING INFORMATION

| ORDERING CODE | PACKAGING | REMARKS | PACKAGE FORM |
|----------------|-------------------------------------|------------------|--------------|
| TSP8510VA-SD-F | Wafer sawn on foil with disco frame | MOQ: 220 000 pcs | Chip |

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25 \text{ }^\circ\text{C}$, unless otherwise specified)

| PARAMETER | TEST CONDITION | SYMBOL | VALUE | UNIT |
|-----------------------------------|---------------------------------|------------|-------------|------------------|
| Forward current | | I_F | 100 | mA |
| Reverse voltage | $I_R = 10 \text{ } \mu\text{A}$ | V_R | 15 | V |
| Junction temperature | | T_j | 140 | $^\circ\text{C}$ |
| Operating temperature range | | T_{amb} | -55 to +140 | $^\circ\text{C}$ |
| Storage temperature range chip | | T_{stg1} | -55 to +150 | $^\circ\text{C}$ |
| Storage temperature range on foil | While on mylar membrane | T_{stg2} | 0 to +40 | $^\circ\text{C}$ |



| BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified) | | | | | | |
|---|-------------------------------|-----------------|------|------|------|------------|
| PARAMETER | TEST CONDITION | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Forward voltage ⁽¹⁾ | $I_F = 1\text{ mA}$ | V_F | - | 1.30 | - | V |
| | $I_F = 5\text{ mA}$ | V_F | - | 1.38 | - | V |
| | $I_F = 10\text{ mA}$ | V_F | - | 1.41 | - | V |
| | $I_F = 50\text{ mA}$ | V_F | - | 1.54 | - | V |
| Radiant power ⁽²⁾ | $I_F = 5\text{ mA}$ | ϕ_e | - | 1.6 | - | mW |
| | $I_F = 10\text{ mA}$ | ϕ_e | - | 3.5 | - | mW |
| | $I_F = 50\text{ mA}$ | ϕ_e | - | 19.5 | - | mW |
| Reverse voltage ⁽²⁾ | $I_R = 10\text{ }\mu\text{A}$ | V_R | 15 | 28 | - | V |
| Angle of half intensity | $I_F = 50\text{ mA}$ | ϕ | - | 55 | - | $^{\circ}$ |
| Peak wavelength | $I_F = 10\text{ mA}$ | λ_p | 840 | 855 | 870 | nm |
| | $I_F = 50\text{ mA}$ | λ_p | 840 | 858 | 870 | nm |
| Spectral bandwidth | $I_F = 50\text{ mA}$ | $\lambda_{0.5}$ | - | 33 | - | nm |
| Rise time ⁽³⁾ | $I_F = 7\text{ mA}$ | t_r | - | 25 | - | ns |
| | $I_F = 30\text{ mA}$ | t_r | - | 20 | - | ns |
| Fall time ⁽³⁾ | $I_F = 7\text{ mA}$ | t_f | - | 28 | - | ns |
| | $I_F = 30\text{ mA}$ | t_f | - | 26 | - | ns |

Notes

- ⁽¹⁾ Measured on TO-18 header in integrating sphere
- ⁽²⁾ Measured on Vishay automated testing system
- ⁽³⁾ Pulse width of $t_p = 40\text{ ns}$, $t_p/T = 0.04$

BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

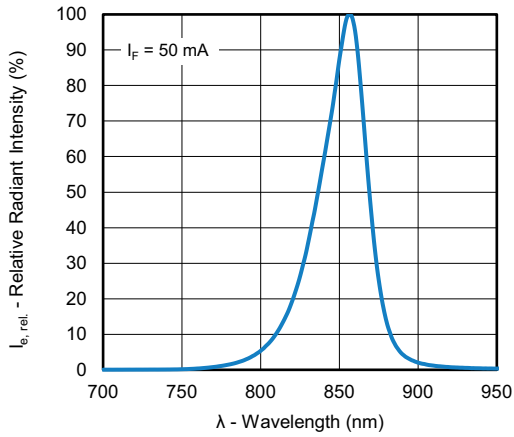


Fig. 1 - Relative Spectral Emission
 $I_{rel} = f(\lambda)$, $I_F = 50\text{ mA}$

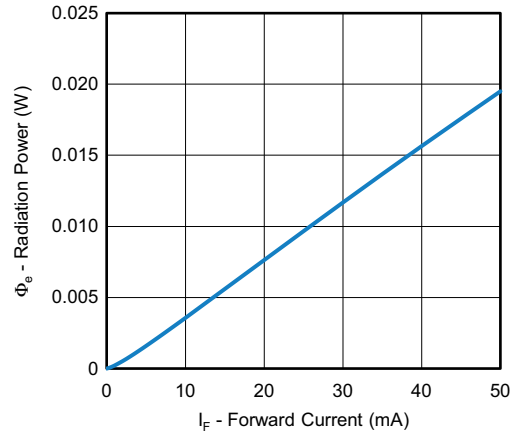


Fig. 3 - Radiant Power vs. Forward Current

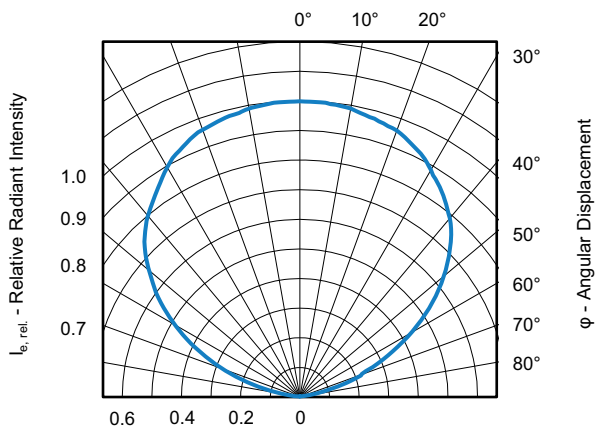


Fig. 2 - Radiant Characteristics
 $I_{rel} = f(\phi)$

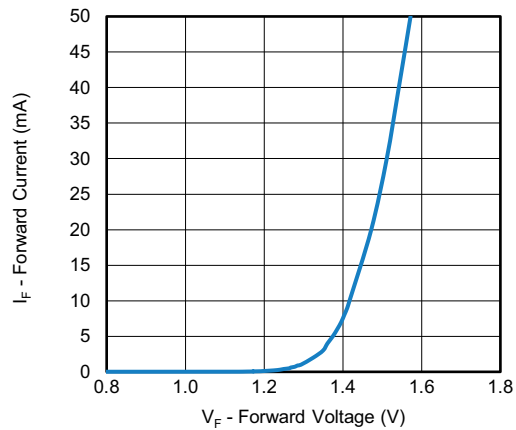


Fig. 4 - Forward Current vs. Forward Voltage

DIMENSIONS

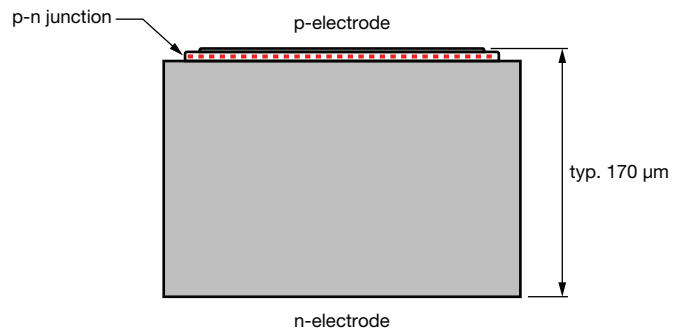
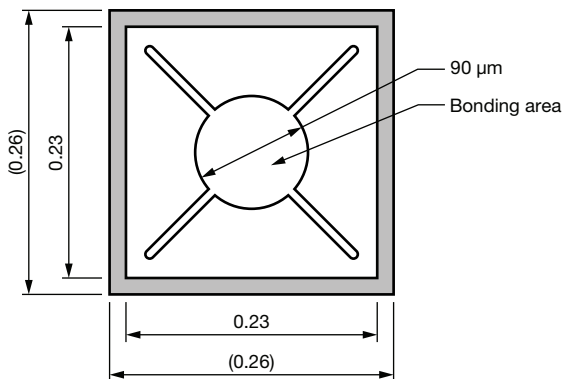


Fig. 5 - Sectional View



| MECHANICAL DIMENSIONS | | | | | |
|-----------------------------------|----------------|-------|-------|-------|------|
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Length of chip edge (x-direction) | L _x | 0.245 | 0.260 | 0.275 | mm |
| Length of chip edge (y-direction) | L _y | 0.245 | 0.260 | 0.275 | mm |
| Die height | H | 0.155 | 0.170 | 0.185 | mm |
| Diameter of bondpad | d | 0.080 | 0.090 | 0.100 | mm |

| ADDITIONAL INFORMATION | |
|----------------------------------|--|
| Frontside metallization, cathode | Gold alloy |
| Backside metallization, anode | Gold alloy |
| Dicing | Sawing |
| Die bonding technology | Epoxy bonding |
| Wire bonding technology | Ball, BSOB, not suitable for reverse bonding |
| Operation mode | Only suitable for forward current operation |

Note

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.
- The visual inspection shall be made in accordance with the “specification of visual inspection as referenced”. The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.
- The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.



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