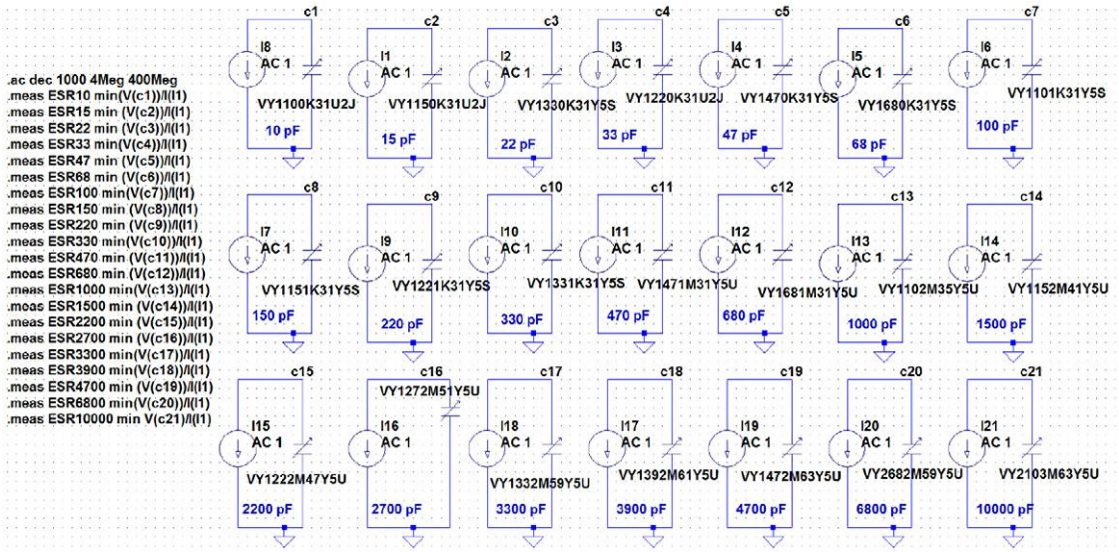
# LTspice® Simulations of Vishay Ceramic Capacitors VY1 / VY2 and AY2

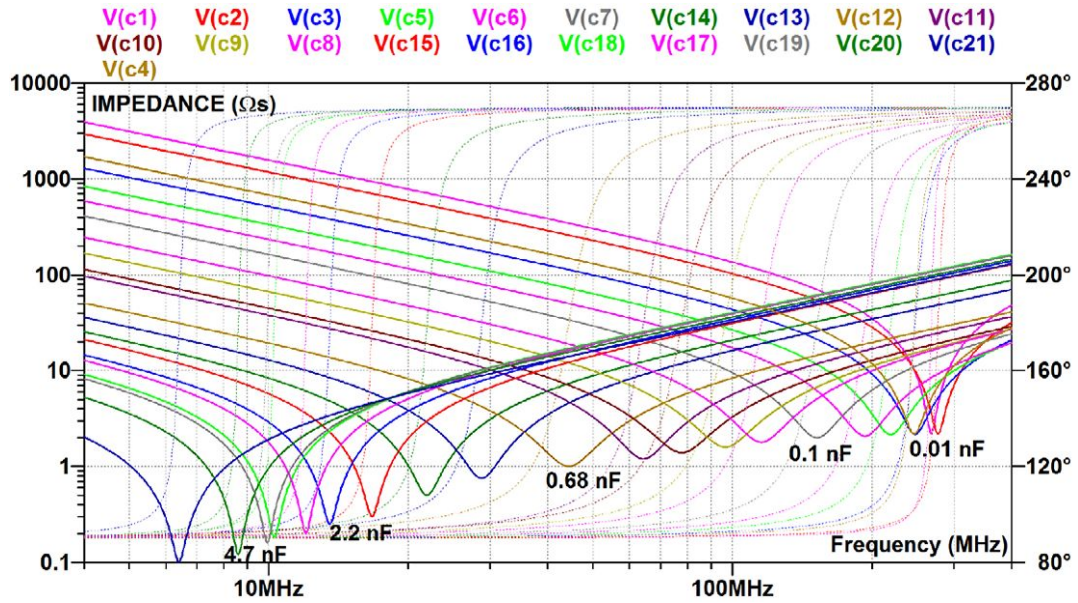
## 1. AC SWEEP

This simulation sweeps the frequency in an AC simulation where the impedance is computed.

File: ceracap_VY_freqsweep.asc



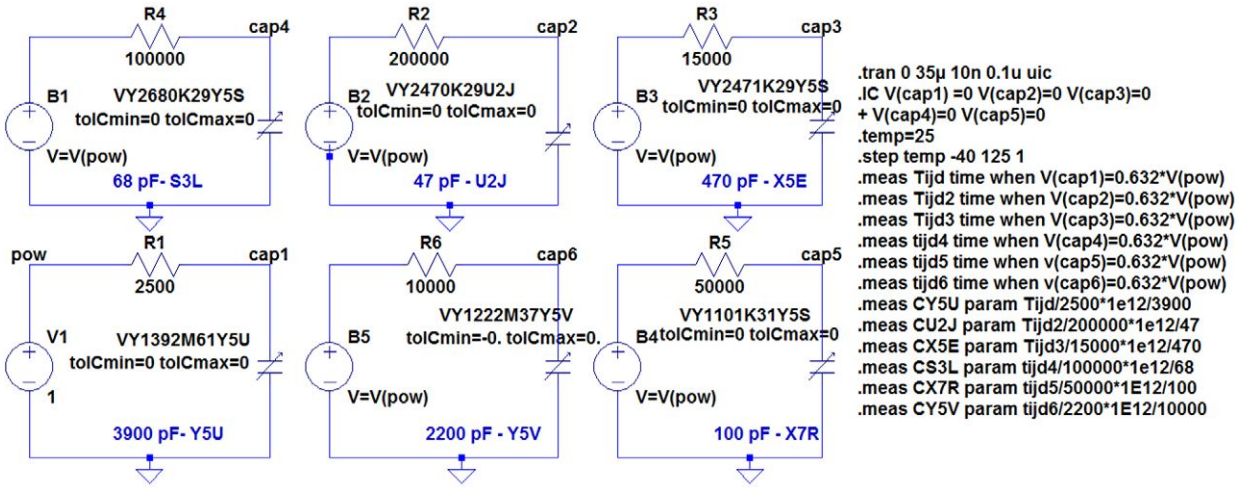

**Results**



## 2. TEMP SWEEP

In this simulation, the temperature is swept while a DC voltage is used to charge the capacity through a fixed resistor. The charging time is used to compute the capacity.

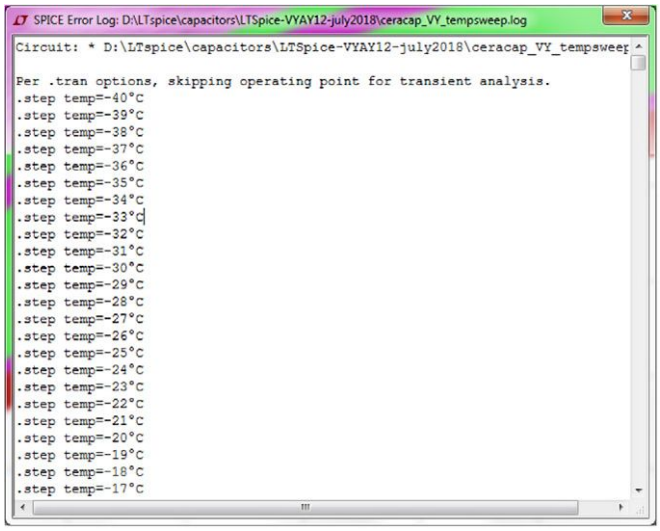
File: ceracap_VY_tempsweep.asc




### Results

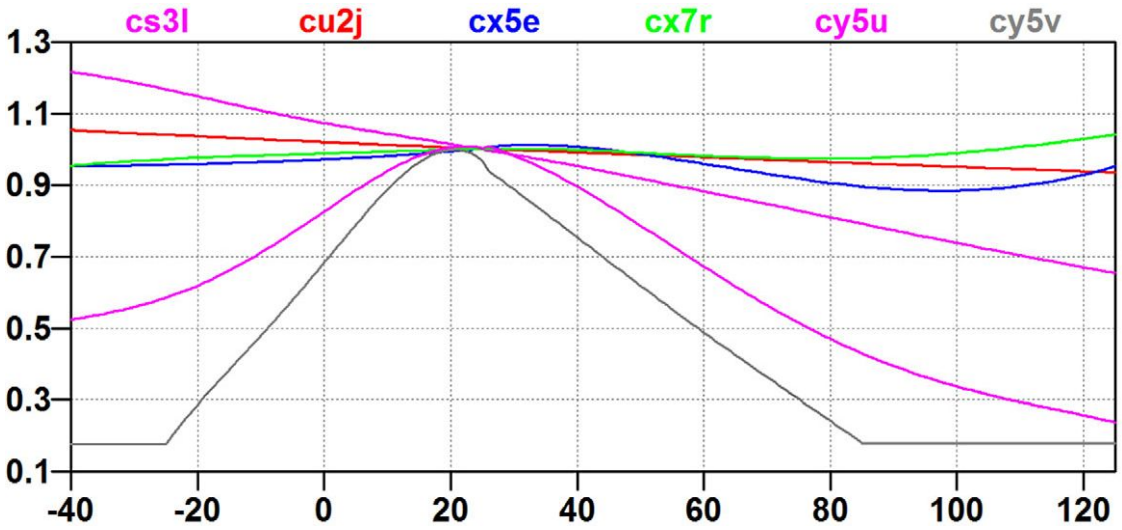
In the principal menu of the raw file, click on “view” then “spice error file”.

The following pop up screen shows up. Point out any place inside this screen.




Right click “plot measured data”.

The ratio capacitance (temperature) divided by the capacitance value at 25 °C is plotted in function of the temperature.




**Note**

- The Y5V material is specified between -25 °C and +85 °C and the curve is thus clipped outside this range

## 3. DC VOLTAGE SWEEP

These simulations apply a variable DC voltage on the components, plus an AC 5 V at 1 kHz. The measured difference between AC current and the leakage current at this DC voltage, is used to compute the capacitance. The B5 voltage control source is used to compute the voltage at the node C5YUmeas which represents the capacitance measured in Vishay laboratory.

The minimal and maximal capacitance values are visualized by driving the parameters tolCmin and tolCmax respectively at -20 and +20 (value expressed directly in %, NOT -0.2 and +0.2)

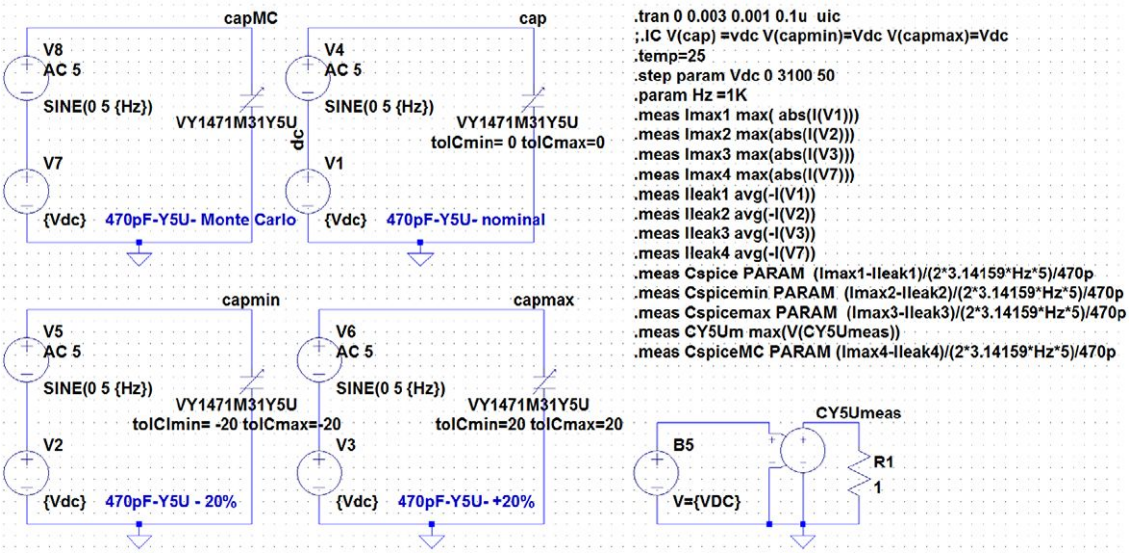
Files:

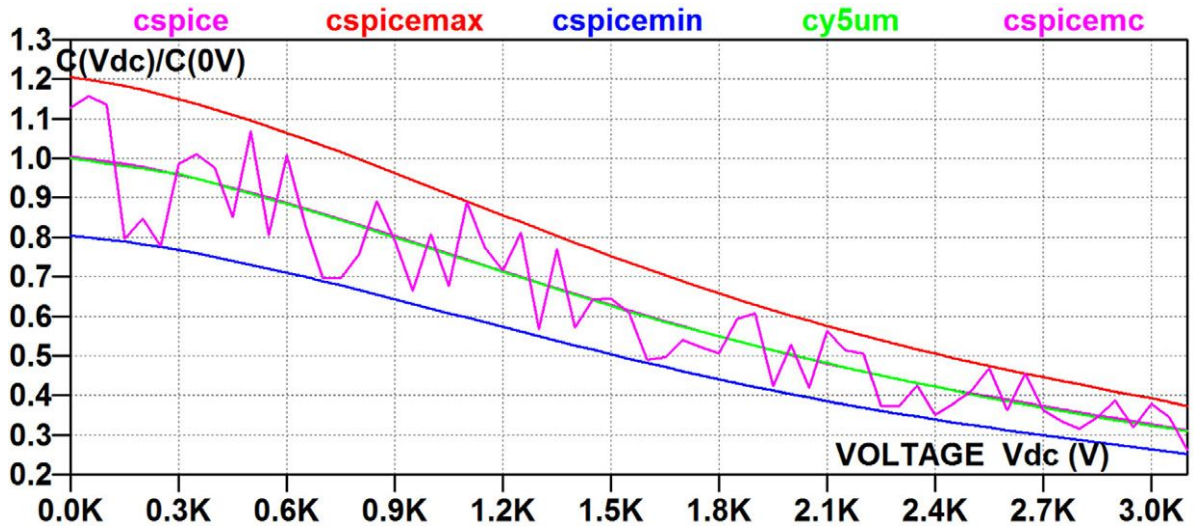
ceracap_VY_voltsweep1.asc

ceracap_VY_voltsweep2.asc

ceracap_VY_voltsweep3.asc

ceracap_VY_voltsweep4.asc






## 4. LEAKAGE CURRENT SIMULATION

The leakage current is measured for each capacitance value in function of the increasing applied DC voltage from 0 V to 4000 V.

File: ceracap_VY_leakage_current.asc