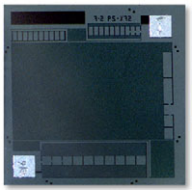
Thin Film, Top-Contact Megohm Resistor



Product may not be to scale

The SFX series resistor chips extends the range of available resistance to 20 MΩ These offer one of the best combinations of small size and high value available.

The SFXs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SFXs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or class K.

FEATURES

- Wire bondable
- Megohm resistance range: 0.36 MΩ to 30 MΩ
- Chip size: 0.040 inches square standard, 0.030 inches square and 0.055 inches square optional
- Case: 0303, 0404, 0505
- Reduced hybrid size
- Resistor material: tantalum nitride, self-passivating
- Oxidized silicon substrate
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

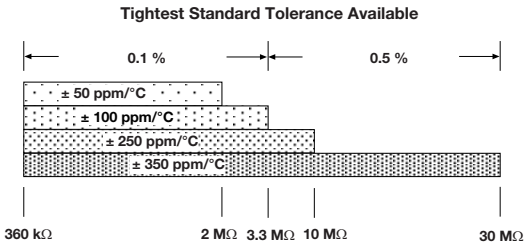
RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

APPLICATIONS

The SFX series megohm resistor chips are designed for use in hybrid packages which require small-size high-value resistors.

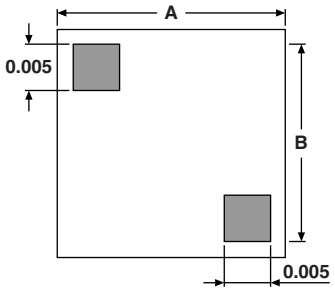
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	**VALUE**	**UNIT**
Total Resistance Range	360K to 30M	Ω
Standard Tolerances	± 0.1, ± 0.5	%
TCR	± 50, ± 100, ± 250, ± 350	ppm/°C



SIZE (in inches)	**MIN.**	**MAX.**
0.030 x 0.030	360 kΩ	10 MΩ
0.040 x 0.040	510 kΩ	20 MΩ
0.055 x 0.055	1 MΩ	30 MΩ

STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
Noise, MIL-STD-202, Method 308	-12 typ.	dB
Moisture Resistance, MIL-STD-202 Method 106, (Passivated only)	± 0.5 max. $\Delta R/R$	%
Stability, 1000 h, +125 °C, 10 mW	± 1.0 max. $\Delta R/R$	%
Operating Temperature Range	-55 to +125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. $\Delta R/R$	%
High Temperature Exposure, +150 °C, 100 h	± 0.5 max. $\Delta R/R$	%
Dielectric Voltage Breakdown	400	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at +70 °C (Derated to zero at +175 °C)	0.020	W
5x Rated Power Short-Time Overload, +25 °C, 5 s	± 0.25 max. $\Delta R/R$	%

DIMENSIONS in inches (millimeters)



A ± 0.002 (± 0.05)	B ± 0.002 (± 0.05)
0.030 (0.76)	0.027 (0.69)
0.040 (1.01)	0.037 (0.94)
0.055 (1.40)	0.052 (1.32)

SCHEMATIC

MECHANICAL SPECIFICATIONS

PARAMETER	VALUE
Chip Size	Per table above
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.050 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO_2
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm)
Number of Pads	2
Pad Material	10 kÅ minimum aluminum (gold pads available)
Backing	None, lapped semiconductor silicon (gold back available)

GLOBAL PART NUMBER INFORMATION

Global Part Number: SFX25003KR4GGKWS

Global Part Number Description: SFX 2.5M 10 % 0 ppm/°C/- 250 ppm/°C 40 Au Au K WS

S	F	X	2	5	0	0	3	K	R	4	G	G	K	W	S

MODEL	RESISTANCE	RESISTANCE MULTIPLIER CODE	TOLERANCE CODE	TCR (ppm/°C)	SIZE	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
SFX High value TaN on silicon	The first 4 digits are significant figures of resistance	**2** = 100 **3** = 1000 **4** = 10 000	**B** = 0.1 % **C** = 0.25 % **D** = 0.5 % **F** = 1.0 % **G** = 2.0 % **J** = 5.0 % **K** = 10.0 %	**C** = ± 50 **K** = ± 100 **M** = ± 250 **W** = ± 350 **I** = 0/- 200 **R** = 0/- 250 **P** = 0/- 350	**3** = 30 x 30 **4** = 40 x 40 **5** = 55 x 55	**G** = Au **A** = Al	**G** = Au **N** = none	**H** = class H **K** = class K	**WS** = waffle pack, 100 min., 1 mult.

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