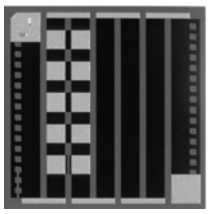
Thin Film Power Resistors



Product may not be to scale

The PWB series resistor chips offer a 1 W power rating in a relatively small size. They offer one of the best combinations of size and power available.

The PWBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The PWBs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032, class H or class K.

FEATURES

- Wire bondable
- Power: 1 W
- Chip size: 0.070 inches square
- Case: 0707
- Resistance range: 0.3 Ω to 20 kΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self-passivating
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

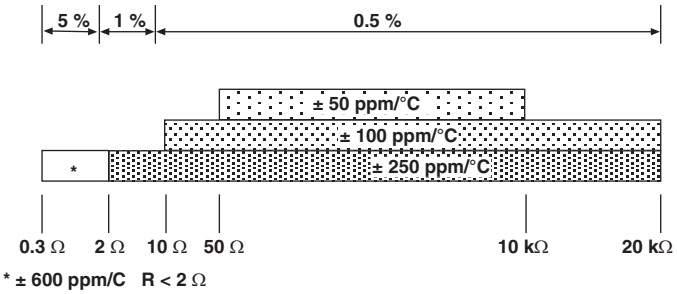
GREEN (5-2008)

APPLICATIONS

The PWB resistor chips are used mainly in higher power circuits of amplifiers where increased power loads require a more specialized resistor.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	**VALUE**	**UNIT**
Total Resistance Range	0.3 to 20K	Ω
Standard Tolerances	± 0.5, ± 1, ± 5	%
TCR	± 50, ± 100, ± 250	ppm/°C

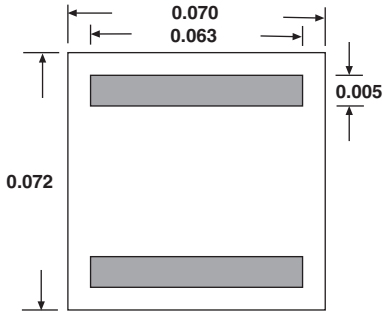
Tightest Standard Tolerance Available



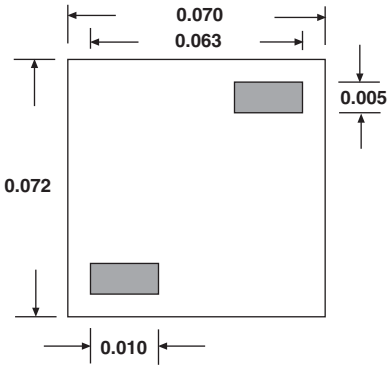
* ± 600 ppm/C R < 2 Ω

STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
Noise, MIL-STD-202, Method 308 100 Ω to 250 kΩ < 100 Ω or > 251 kΩ	 - 35 typ. - 20 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. Δ*R*/*R*	%
Stability, 1000 h, + 125 °C, 500 mW	± 0.5 max. Δ*R*/*R*	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 max. Δ*R*/*R*	%
High Temperature Exposure, + 150 °C, 100 h	± 0.2 max. Δ*R*/*R*	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage Steady State 5 x Rated Power	 100 max. 200 max.	V
DC Power Rating at + 70 °C (Derated to zero at + 175 °C) (Conductive epoxy die attach to alumina substrate)	1	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 max. Δ*R*/*R*	%

DIMENSIONS in inches



TYPICAL RANGE
R < 240 Ω



TYPICAL RANGE
240 Ω to 20 kΩ

SCHEMATIC

MECHANICAL SPECIFICATIONS	
PARAMETER	**VALUE**
Chip Size	0.070" x 0.070" ± 0.005" (1.781 mm x 1.781 mm ± 0.127 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO_2
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005" x 0.010" (0.127 mm x 0.254 mm) minimum
Number of Pads	2
Pad Material	10 kÅ minimum aluminum (Au optional)
Backing	None, lapped semiconductor silicon (Au back optional)

GLOBAL PART NUMBER INFORMATION

Global Part Number: **PWB50000FKANHWS** **PWB12500KCGGKWS**

Global Part Number Description: **PWB 5K 1 % 100 ppm Al None H WS** **PWB 1.25K 10 % 100 ppm Au Au K WS**

P	W	B	5	0	0	0	0	F	K	A	N	H	W	S

MODEL	RESISTANCE	RESISTANCE MULTIPLIER CODE	TOLERANCE CODE (%)	TCR (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
PWB 70 x 70 size Power resistor	First 4 digits are significant figures of resistance	**D** = 0.0001 **C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**D** = 0.5 **F** = 1.0 **G** = 2.0 **J** = 5.0 **K** = 10	**C** = ± 50 **K** = ± 100 **M** = ± 250 **Z** = + 600/ - 100	**G** = Au **A** = Al	**G** = Au **N** = None	**H** = Class H **K** = Class K	**WS** = Waffle pack 100 min, 1 mult

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