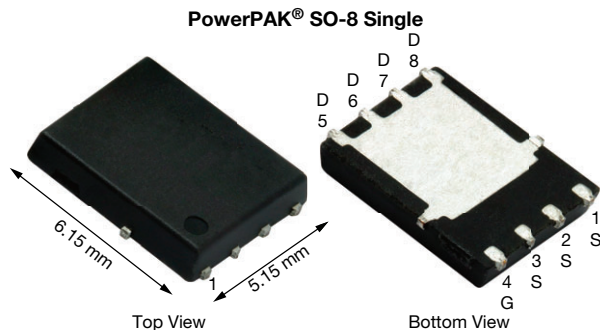


N-Channel 150 V (D-S) MOSFET



| PRODUCT SUMMARY | |
|--|--------|
| V_{DS} (V) | 150 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V | 0.0555 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V | 0.0624 |
| Q_g typ. (nC) | 5.8 |
| I_D (A) | 18 |
| Configuration | Single |

| ORDERING INFORMATION | |
|---------------------------------|------------------|
| Package | PowerPAK SO-8 |
| Lead (Pb)-free and halogen-free | SIR5712DP-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted) | | | | |
|---|---------------|----------------|-------------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | | V_{DS} | 150 | V |
| Gate-source voltage | | V_{GS} | ± 20 | |
| Continuous drain current ($T_J = 150$ °C) | $T_C = 25$ °C | I_D | 18 g | A |
| | $T_C = 70$ °C | | 14.9 | |
| | $T_A = 25$ °C | | 6.5 b, c | |
| | $T_A = 70$ °C | | 5.2 b, c | |
| Pulsed drain current ($t = 100$ μ s) | | I_{DM} | 25 | |
| Continuous source-drain diode current | $T_C = 25$ °C | I_S | 18 g | |
| | $T_A = 25$ °C | | 4.2 b, c | |
| Single pulse avalanche current | | I_{AS} | 10 | mJ |
| Single pulse avalanche Energy | | E_{AS} | 5 | |
| Maximum power dissipation | $T_C = 25$ °C | P_D | 40 | W |
| | $T_C = 70$ °C | | 26 | |
| | $T_A = 25$ °C | | 5 b, c | |
| | $T_A = 70$ °C | | 3.2 b, c | |
| Operating junction and storage temperature range | | T_J, T_{stg} | -55 to +150 | °C |
| Soldering recommendations (peak temperature) d, e | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|----------------------------------|---------------|------------|---------|---------|------|
| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum junction to ambient b, f | $t \leq 10$ s | R_{thJA} | 21 | 25 | °C/W |
| | Steady state | R_{thJC} | 2.5 | 3.1 | |

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- Package limited

FEATURES

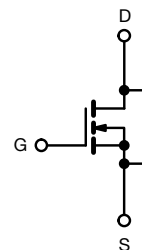
- TrenchFET® Gen V power MOSFET
- Very low R_{DS} - Q_g figure of merit (FOM)
- Tuned for the lowest R_{DS} - Q_{oss} FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Primary side switch
- DC/DC converters
- Motor drive control



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET



| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|--------------------------------------|---|------|--------|--------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | 150 | - | - | V |
| V _{DS} temperature coefficient | ΔV _{DS} /T _J | I _D = 250 μA | - | 96 | - | mV/°C |
| V _{GS(th)} temperature coefficient | ΔV _{GS(th)} /T _J | | - | -8 | - | |
| Gate-source threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 2 | - | 4 | V |
| Gate-source leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 20 V | - | - | ± 100 | nA |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = 120 V, V _{GS} = 0 V | - | - | 1 | μA |
| | | V _{DS} = 120 V, V _{GS} = 0 V, T _J = 55 °C | - | - | 10 | |
| Drain-source on-state resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 6.5 A | - | 0.0462 | 0.0555 | Ω |
| | | V _{GS} = 7.5 V, I _D = 6.2 A | - | 0.052 | 0.0624 | |
| Forward transconductance ^a | g _{fs} | V _{DS} = 10 V, I _D = 6.5 A | - | 12 | - | S |
| Dynamic ^b | | | | | | |
| Input capacitance | C _{iss} | V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz | - | 500 | - | pF |
| Output capacitance | C _{oss} | | - | 70 | - | |
| Reverse transfer capacitance | C _{rss} | | - | 6 | - | |
| C _{rss} /C _{iss} ratio | | | - | 0.012 | 0.024 | |
| Total gate charge | Q _g | V _{DS} = 75 V, V _{GS} = 10 V, I _D = 6.5 A | - | 7.5 | 11.3 | nC |
| | | V _{DS} = 75 V, V _{GS} = 7.5 V, I _D = 6.5 A | - | 5.8 | 8.7 | |
| Gate-source charge | Q _{gs} | | - | 3.4 | - | |
| Gate-drain charge | Q _{gd} | | - | 1.2 | - | |
| Output charge | Q _{oss} | V _{DS} = 75 V, V _{GS} = 0 V | - | 21 | - | |
| Gate resistance | R _g | f = 1 MHz | 0.2 | 0.9 | 1.8 | Ω |
| Turn-on delay time | t _{d(on)} | V _{DD} = 75 V, R _L = 14.4 Ω I _D ≅ 5.2 A, V _{GEN} = 10 V, R _g = 1 Ω | - | 15 | 30 | ns |
| Rise time | t _r | | - | 6 | 12 | |
| Turn-off delay time | t _{d(off)} | | - | 17 | 34 | |
| Fall time | t _f | | - | 8 | 16 | |
| Turn-on delay time | t _{d(on)} | V _{DD} = 75 V, R _L = 14.4 Ω I _D ≅ 5.2 A, V _{GEN} = 7.5 V, R _g = 1 Ω | - | 17 | 34 | |
| Rise time | t _r | | - | 7 | 14 | |
| Turn-off delay time | t _{d(off)} | | - | 18 | 36 | |
| Fall time | t _f | | - | 9 | 18 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous source-drain diode current | I _S | T _C = 25 °C | - | - | 34 | A |
| Pulse diode forward current (t = 100 μs) | I _{SM} | | - | - | 140 | |
| Body diode voltage | V _{SD} | I _S = 5.2 A | - | 0.8 | 1.2 | V |
| Body diode reverse recovery time | t _{rr} | I _F = 5.2 A, di/dt = 100 A/μs, T _J = 25 °C | - | 49 | 98 | ns |
| Body diode reverse recovery charge | Q _{rr} | | - | 96 | 192 | nC |
| Reverse recovery fall time | t _a | | - | 42 | - | ns |
| Reverse recovery rise time | t _b | | - | 7 | - | |

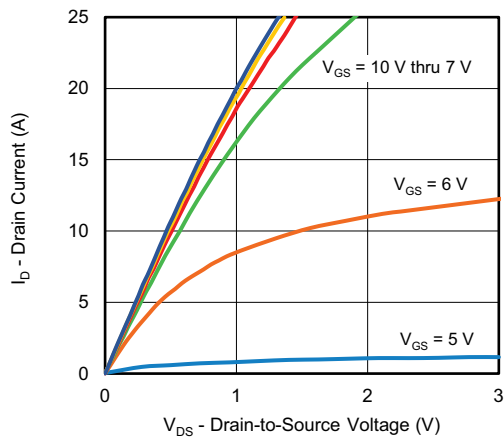
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. $T_{CASE} = 25\text{ }^{\circ}\text{C}$. Expected voltage stress during 100 % UIS test. Production datalog is not available

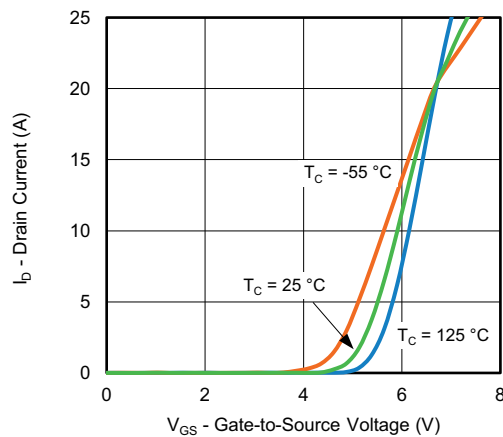
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability



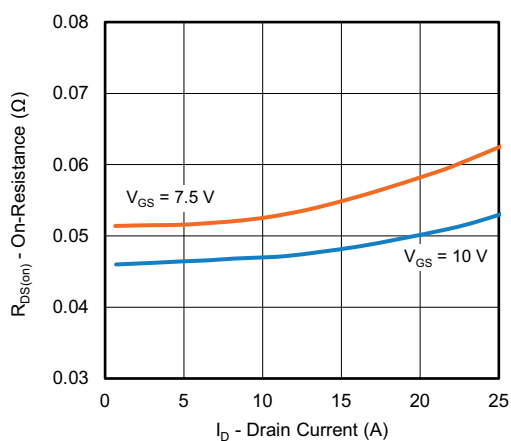
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



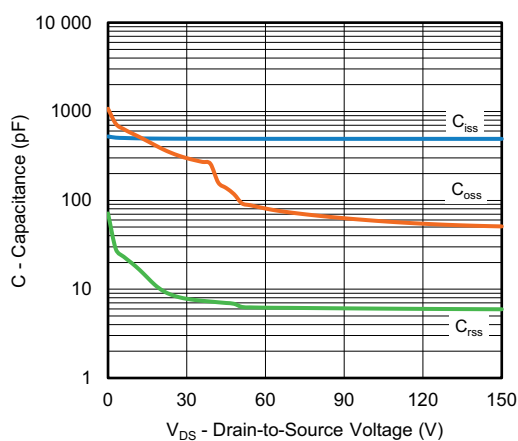
Output Characteristics



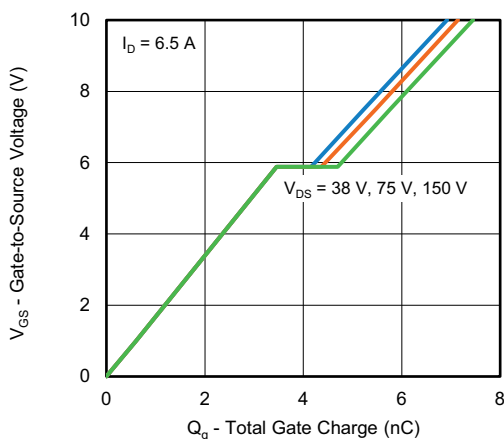
Transfer Characteristics



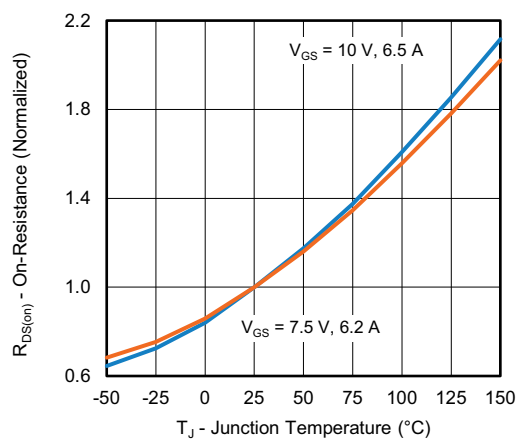
On-Resistance vs. Drain Current



Capacitance



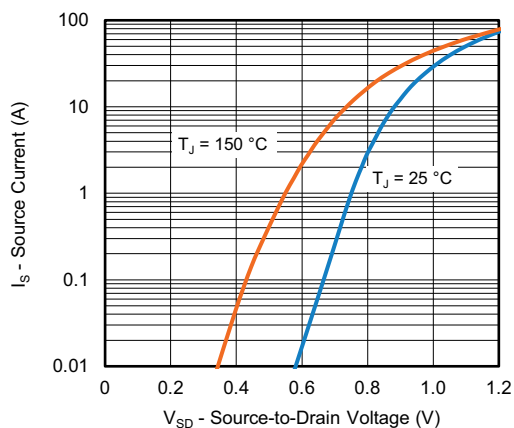
Gate Charge



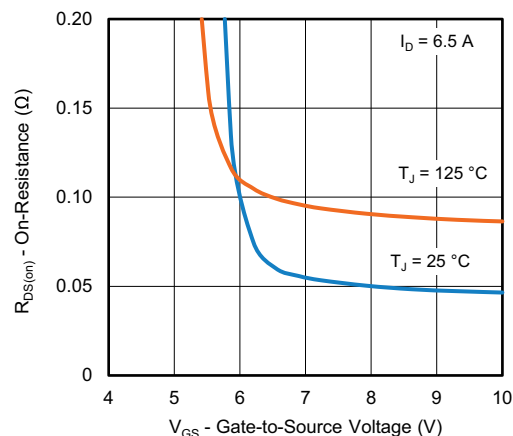
On-Resistance vs. Junction Temperature



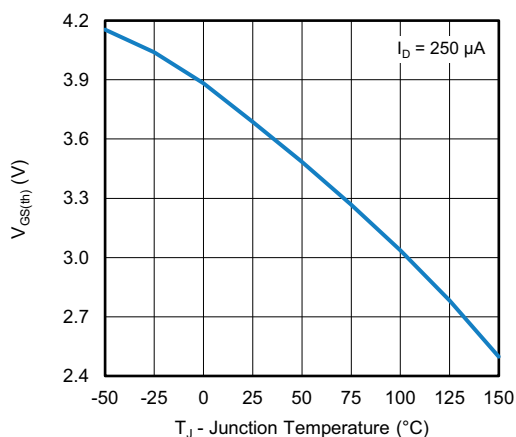
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



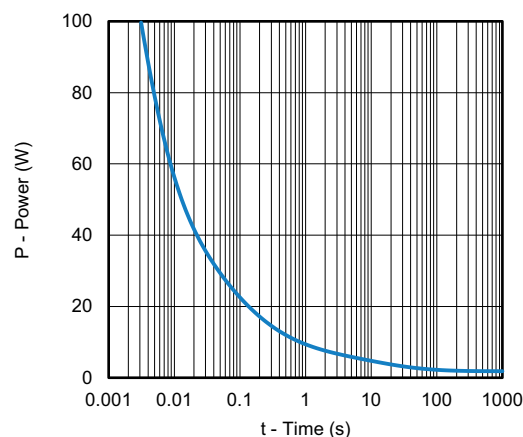
Source-Drain Diode Forward Voltage



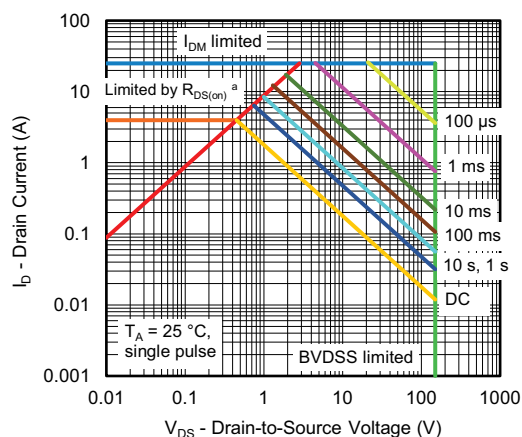
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



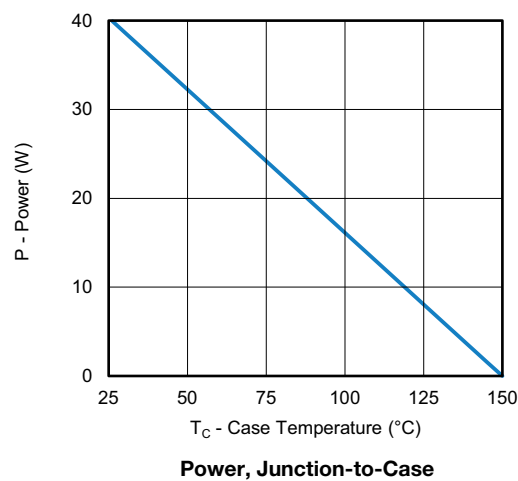
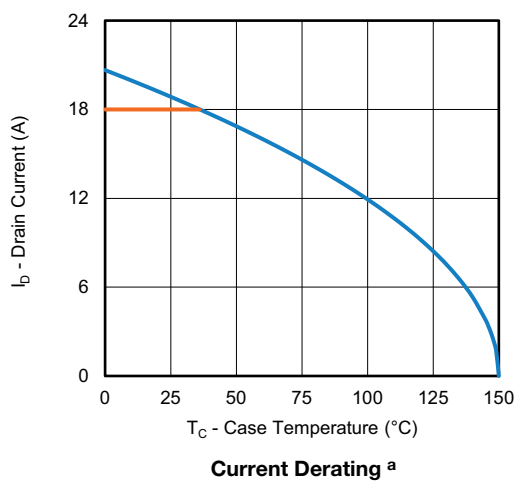
Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

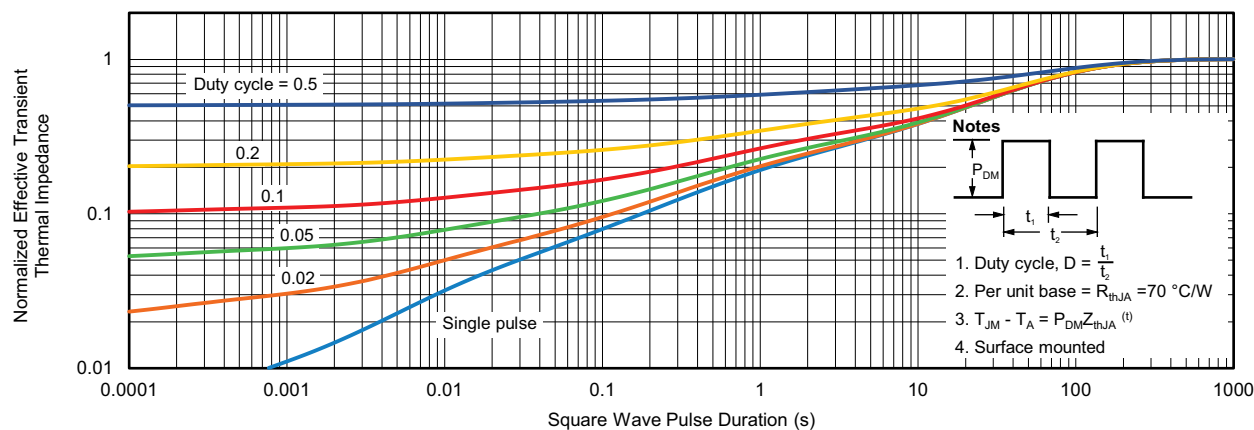


Note

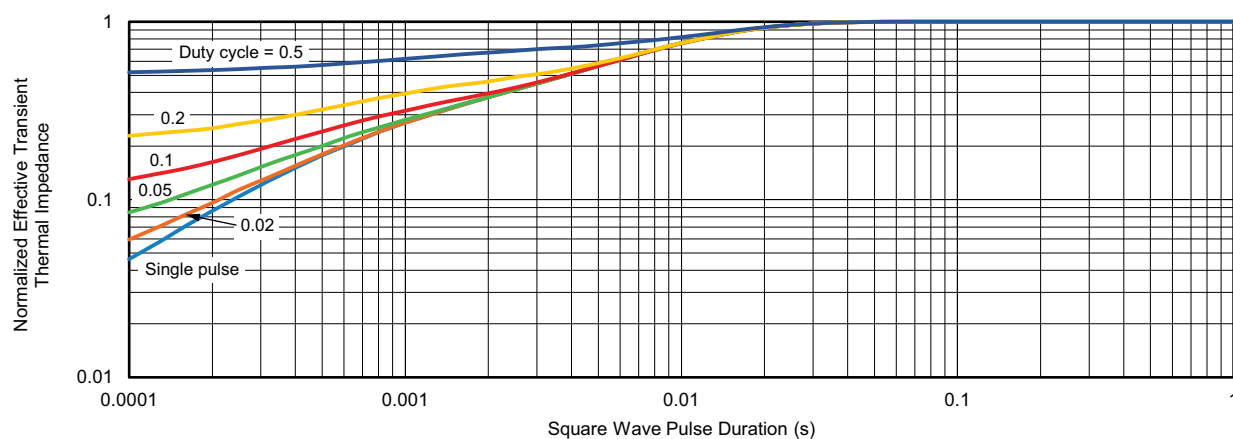
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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