Si3429EDV Vishay Siliconix

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P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^{a, e}	Q _g (TYP.)			
	0.0210 at V_{GS} = -4.5 V	-8				
-20	0.0240 at V_{GS} = -2.5 V	-8	43.2 nC			
	0.0380 at V _{GS} = -1.8 V	-8				

TSOP-6 Single

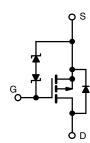


FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Built-in ESD protection
 - Typical ESD performance 3000 V
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Power management for portable and consumer
 - Load switches
 - DC/DC converters



P-Channel MOSFET

Marking Code: BM

Ordering Information: Si3429EDV-T1-GE3 (lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS ((T _A = 25 °C, unless	s otherwise note	ed)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	-20			
Gate-Source Voltage		V _{GS}	± 8	V	
	T _C = 25 °C		-8 ^e		
Continuous Drain Current (T _J = 150 $^{\circ}$ C)	T _C = 70 °C	1 . [-8 e		
	T _A = 25 °C	I _D	-8 b, c, e		
	T _A = 70 °C		-6.4 ^{b, c}	А	
Pulsed Drain Current (t = 300 µs)		I _{DM}	-40		
	T _C = 25 °C		-3.5		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	-1.7 ^{b, c}		
Maximum Power Dissipation	T _C = 25 °C		4.2		
	T _C = 70 °C		2.7	14/	
	T _A = 25 °C	P _D	2 ^{b, c}		
	T _A = 70 °C	1	1.3 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum Junction-to-Ambient b, d	t ≤ 5 s	R _{thJA}	45	62.5	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	25	30			

Notes

- a. T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. Maximum under steady state conditions is 110 °C/W.

e. Package limited.

S14-0913-Rev. A, 28-Apr-14

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COMPLIANT

HALOGEN

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Si3429EDV

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				•			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = -250 \mu A$	-20	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	L 050 A	-	-12	-		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	2.4	-	mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$		-	-1	V	
	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 8 V$	-	_	± 10		
Gate-Source Leakage		$V_{DS} = 0 V, V_{GS} = \pm 4.5 V$	-	_	± 1		
		$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	-1	μΑ	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V}$	-15	-	-	А	
	_ (***)	V _{GS} = -4.5 V, I _D = -4 A	-	0.0175	0.0210	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, \text{ I}_D = -4 \text{ A}$	-	0.0200	0.0240	Ω	
	23(01)	$V_{GS} = -1.8 \text{ V}, \text{ I}_D = -2 \text{ A}$	-	0.0250	0.0380		
Dynamic ^b						I	
Input Capacitance	C _{iss}		-	4083	-		
Output Capacitance	C _{oss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	_	395	-	pF	
Reverse Transfer Capacitance	C _{rss}		-	365	-		
	Orss	V _{DS} = -10 V, V _{GS} = -8 V, I _D = -8 A	- 78.2 118			+	
Total Gate Charge	Q _g Q _{qs}		-	43.2	65	nC	
Gate-Source Charge		V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -8 A	-	6.3	-		
Gate-Drain Charge	Q _{gs} Q _{gd}	$v_{\rm DS} = -10 v, v_{\rm GS} = -4.5 v, v_{\rm D} = -0 A$		4.3	-	1	
Gate Resistance	R _g	f – 1 MHz	1.8	9.4	18.8	Ω	
Turn-On Delay Time		1 - 1 10112	1.0	3.4	53	52	
Rise Time	t _{d(on)}	f = 1 MHz			45	-	
	t _r	V_{DD} = -10 V, R _L = 1.56 Ω I _D ≅ -6.4 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	30	-	- ns	
Turn-Off Delay Time	t _{d(off)}		-	174	261		
Fall Time	t _f		-	58	87		
Turn-On Delay Time	t _{d(on)}		-	10	20		
Rise Time	t _r	$V_{DD} = -10 \text{ V}, \text{ R}_{L} = 1.56 \Omega$ $I_{D} \cong -6.4 \text{ A}, \text{ V}_{\text{GEN}} = -8 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	17	26		
Turn-Off Delay Time	t _{d(off)}	10 = 0.4 A, VGEN = 0.0, Hg = 1.32	-	210	315		
Fall Time	t _f		-	64	96		
Drain-Source Body Diode Characterist				1			
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	-3.5	A	
Pulse Diode Forward Current	I _{SM}			-	-40		
Body Diode Voltage	V _{SD}	$I_{\rm S}$ = -6.4 A, $V_{\rm GS}$ = 0 V	-	-0.8	-1.2	V	
Body Diode Reverse Recovery Time	t _{rr}		-	28	42	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = -6.4 A, dl/dt = 100 A/μs, T _J = 25 °C	-	16	24	nC	
Reverse Recovery Fall Time	ta		-	13	-	- ns	
Reverse Recovery Rise Time	t _b		-	15	-		

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$

b. Guaranteed by design, not subject to production testing.

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Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

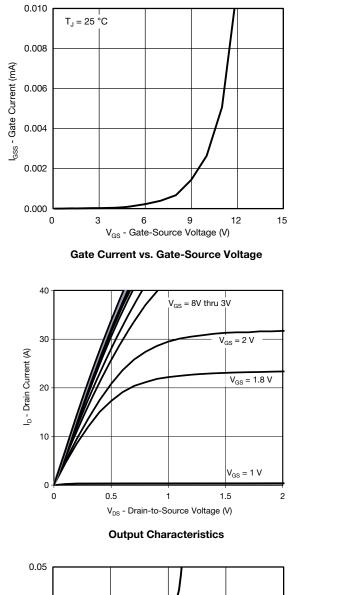
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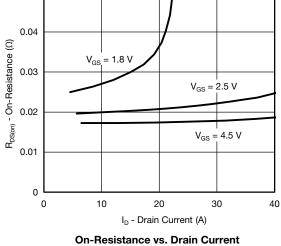


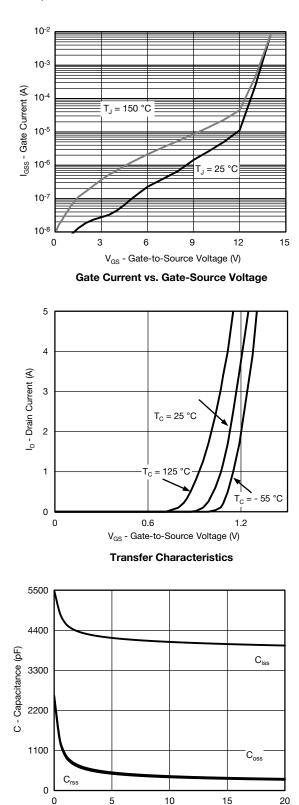
Si3429EDV

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)







Capacitance

10

V_{DS} - Drain-to-Source Voltage (V)

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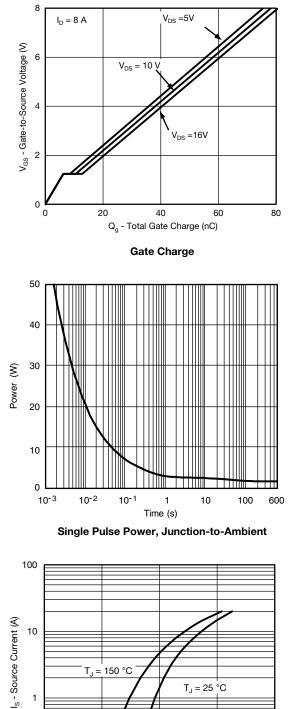
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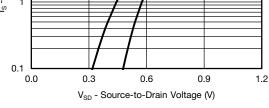


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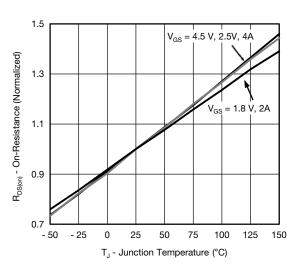
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

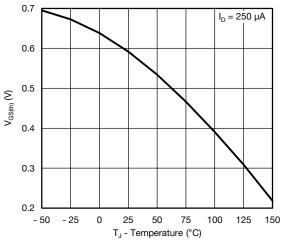




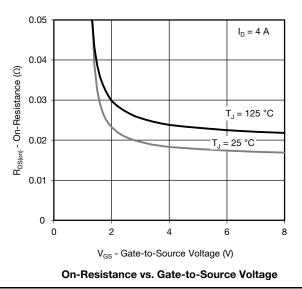
Source-Drain Diode Forward Voltage



On-Resistance vs. Junction Temperature







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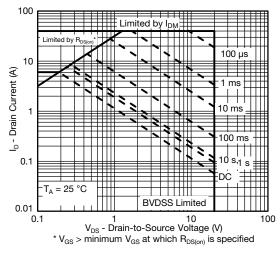
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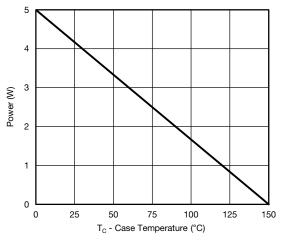


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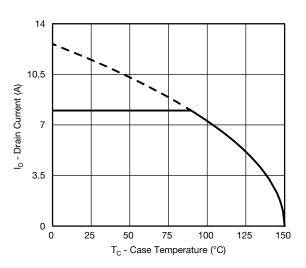
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



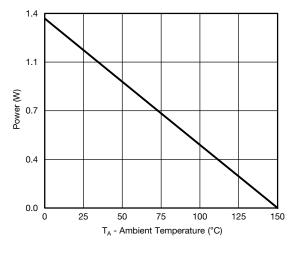
Safe Operating Area, Junction-to-Ambient



Power Junction-to-Foot



Current Derating*



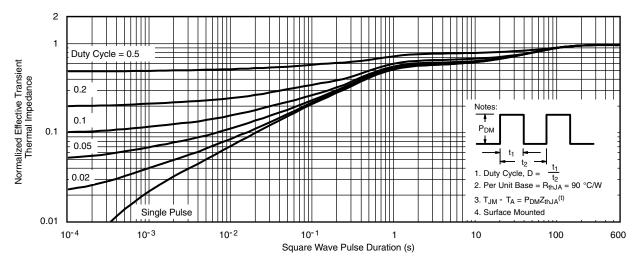
Power Junction-to-Ambient

* The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

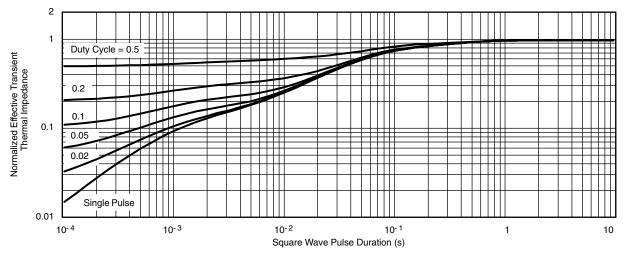


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62946.

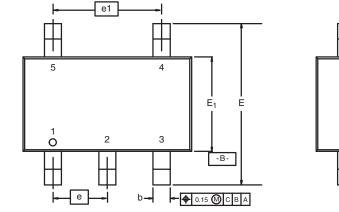
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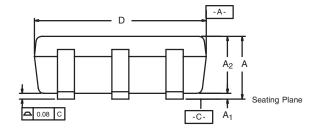
Package Information

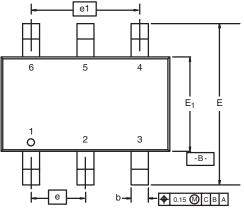
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TSOP: 5/6-LEAD JEDEC Part Number: MO-193C

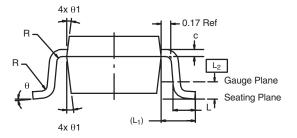








6-LEAD TSOP



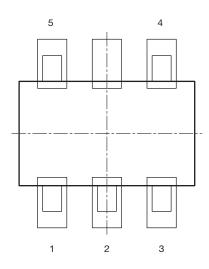
	MIL	LIMETER	RS	I	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max		
Α	0.91	-	1.10	0.036	-	0.043		
A ₁	0.01	-	0.10	0.0004	-	0.004		
A ₂	0.90	-	1.00	0.035	0.038	0.039		
b	0.30	0.32	0.45	0.012	0.013	0.018		
С	0.10	0.15	0.20	0.004	0.006	0.008		
D	2.95	3.05	3.10	0.116	0.120	0.122		
Е	2.70	2.85	2.98	0.106	0.112	0.117		
E ₁	1.55	1.65	1.70	0.061	0.065	0.067		
е		0.95 BSC		0.0374 BSC				
e ₁	1.80	1.90	2.00	0.071	0.075	0.079		
L	0.32	-	0.50	0.012	-	0.020		
L ₁		0.60 Ref		0.024 Ref				
L ₂	0.25 BSC				0.010 BSC			
R	0.10	-	-	0.004	-	-		
θ	0°	4°	8°	0°	4°	8°		
θ_1	7° Nom				7° Nom			
ECN: C DWG: 5		ev. I, 18-Dec	-06					

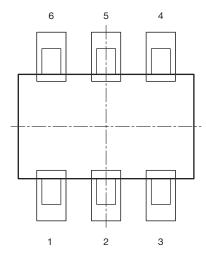
PAD Pattern



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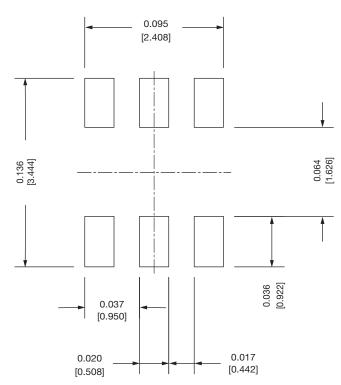
Recommended Land Pattern For TSOP-5L / TSOP-6L





TSOP 5L





Note

• All dimensions are in inches (millimeter)

ECN:	:22-0860-Rev. B, 24-Oct-2022	
DWG:	3010	

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