50 A VRPower® Integrated Power Stage

(Datasheet in Brief)

DESCRIPTION

The SiC673 is integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's 5 mm x 5 mm MLP package, SiC673 enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art Gen IV TrenchFET® technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC673 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V PWM logic.

A user selectable diode emulation mode (ZCD_EN#) is included to improve the light load performance. The device also supports PS4 mode to reduce power consumption when system operates in standby state.

FEATURES

RoHS COMPLIANT HALOGEN FREE

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's Gen I^V MOSFET technology and a low side MOSFET with integrated Schottky diode
- Delivers in excess of 50 A continuous current, 55 A at 10 ms peak current
- High efficiency performance
- High frequency operation up to 2 MHz
- Power MOSFETs optimized for 19 V input stage
- 5 V PWM logic with tri-state and hold-off
- Supports PS4 mode light load requirement for IMVP9 with low shutdown supply current (5 V, 3 µA)
- Under voltage lockout for V_{CIN}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-9 VRPower delivery
  - V_{CORE}, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$
  - V_{CCGI}
- Up to 24 V rail input DC/DC VR modules

TYPICAL APPLICATION DIAGRAM

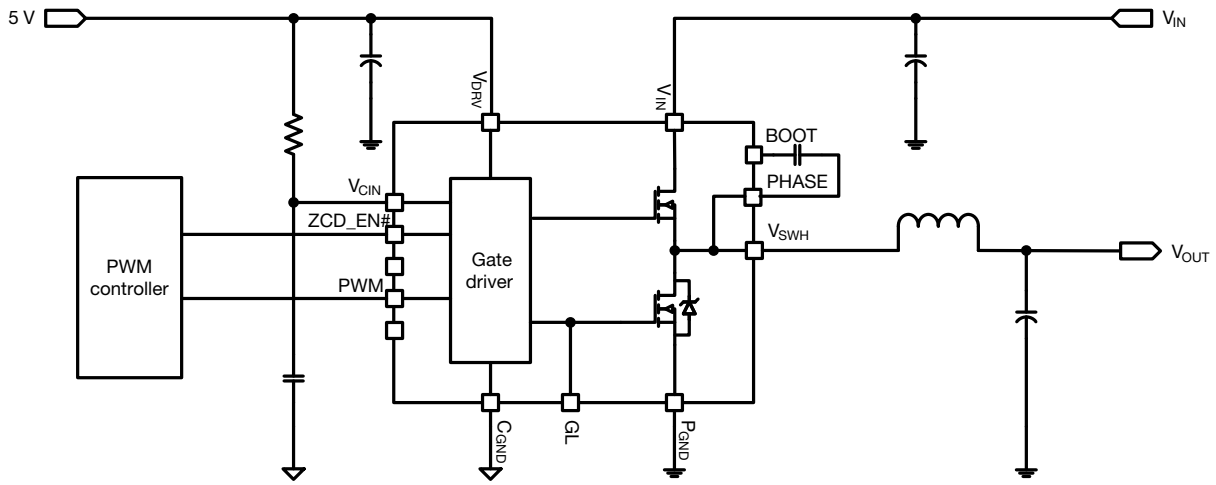


Fig. 1 - SiC673 Typical Application Diagram

For technical questions, contact: powerictechsupport@vishay.com

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PRODUCT SUMMARY	
Part number	SiC673
Description	50 A, 4.5 V to 24 V, 5 V PWM, Power stage with ZCD, with PS4 mode
Input voltage min. (V)	4.5
Input voltage max. (V)	24
Current rating (A)	50
Switch frequency max. (kHz)	2000
Enable (yes / no)	Yes
Monitoring features	None
Protection	UVLO
Light load mode	ZCD, PS4
Pulse-width modulation (V)	5
Package type	PowerPAK MLP55-31L
Package size (W, L, H) (mm)	5 x 5 x 0.7
Status code	2
Product type	VRPower (DrMOS)
Applications	Computer, industrial, networking

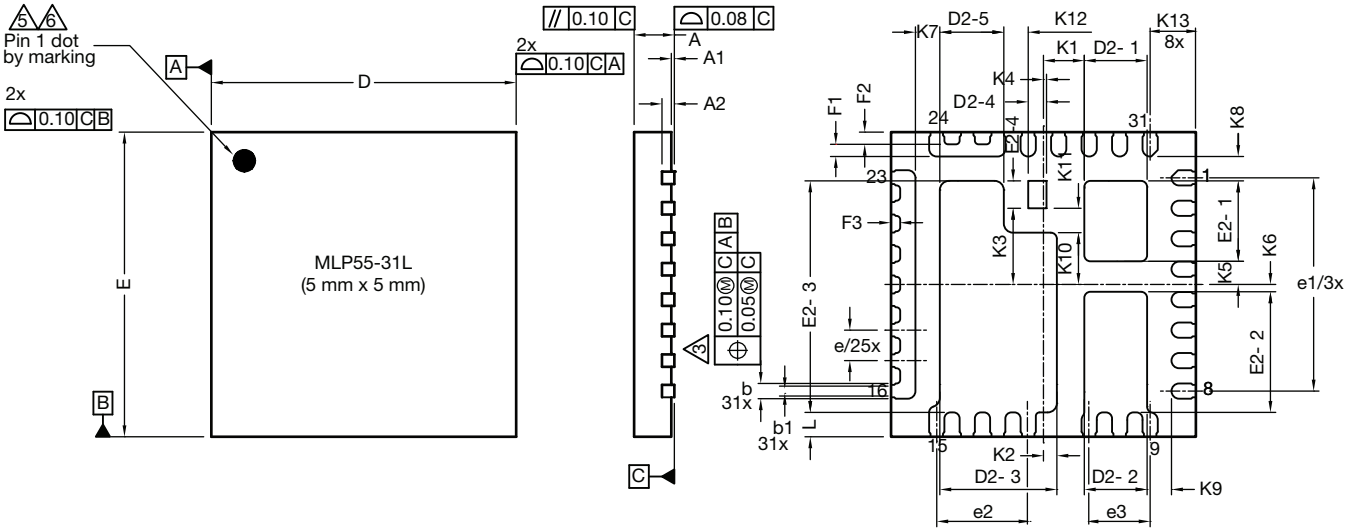
To request the full version of the datasheet, please contact: ICmarketing@vishay.com

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PowerPAK® MLP55-31L Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b	0.20	0.25	0.30	0.078	0.098	0.011
b1	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.196	0.200
e		0.50 BSC			0.019 BSC	
e1		3.50 BSC			0.138 BSC	
e2		1.50 BSC			0.060 BSC	
e3		1.00 BSC			0.040 BSC	
E	4.90	5.00	5.10	0.193	0.196	0.200
L	0.35	0.40	0.45	0.013	0.015	0.017
D2-1	0.98	1.03	1.08	0.039	0.041	0.043
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	1.87	1.92	1.97	0.074	0.076	0.078
D2-4		0.30 BSC			0.012 BSC	
D2-5	1.05	1.10	1.15	0.041	0.043	0.045
E2-1	1.27	1.32	1.37	0.050	0.052	0.054
E2-2	1.93	1.98	2.03	0.076	0.078	0.080
E2-3	3.75	3.80	3.85	0.148	0.150	0.152
E2-4		0.45 BSC			0.018 BSC	
F1	0.15	0.20	0.25	0.006	0.008	0.010
F2		0.20 ref.			0.008 ref.	
F3		0.15 ref.			0.006 ref.	

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DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K1		0.67 BSC			0.026 BSC	
K2		0.22 BSC			0.008 BSC	
K3		1.25 BSC			0.049 BSC	
K4		0.10 BSC			0.004 BSC	
K5		0.38 BSC			0.015 BSC	
K6		0.12 BSC			0.005 BSC	
K7		0.40 BSC			0.016 BSC	
K8		0.40 BSC			0.016 BSC	
K9		0.40 BSC			0.016 BSC	
K10		0.85 BSC			0.033 BSC	
K11		0.40 BSC			0.016 BSC	
K12		0.40 BSC			0.016 BSC	
K13		0.75 BSC			0.030 BSC	
ECN: T17-0423-Rev. F, 21-Aug-17 DWG: 6025						

Notes

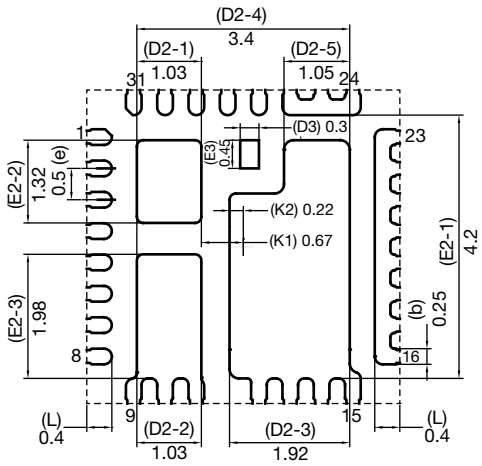
1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
4. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
5. Exact shape and size of this feature is optional
6. Package warpage max. 0.08 mm
7. Applied only for terminals

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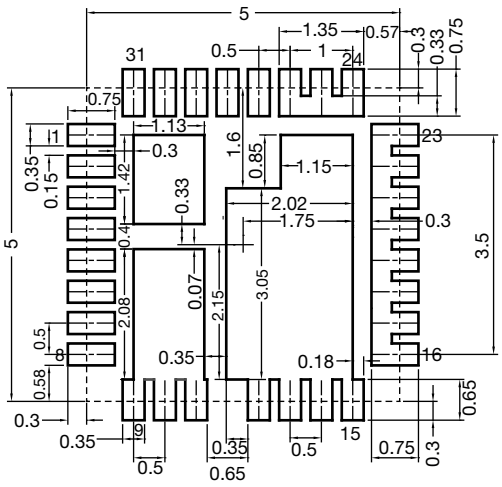
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Recommended Land Pattern
PowerPAK® MLP55-31L

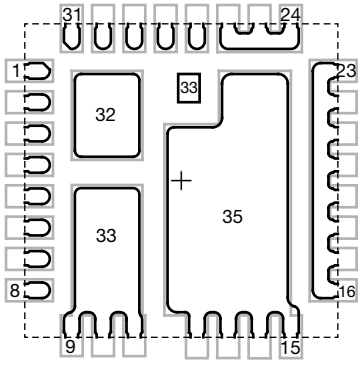
Top side transparent view
(not bottom view)



Land pattern for MLP55-31L



All dimensions in millimeters



Component for MLP55-31L

Land pattern for MLP55-31L

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