Vishay Siliconix

# Automotive N-Channel 60 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.012			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 6 \text{ V}$	0.014			
I <sub>D</sub> (A)	16			
Configuration	Single			

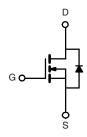
#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified<sup>c</sup>
- 100 % R<sub>q</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



N-Channel MOSFET

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4470EY (for detailed order number please see <a href="https://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS	<b>S</b> (T <sub>C</sub> = 25 °C, unless	s otherwise noted	d)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage		$V_{DS}$	60	V
Gate-source voltage		V <sub>GS</sub>	± 20	
Continuous drain current	T <sub>C</sub> = 25 °C		16	
	T <sub>C</sub> = 125 °C	- I <sub>D</sub>	9	
Continuous source current (diode conduction)		I <sub>S</sub>	6	Α
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	67	
Single pulse avalanche current		I <sub>AS</sub>	50	
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	125	mJ
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	D	7.1	10/
	T <sub>C</sub> = 125 °C	$P_{D}$	2.3	W
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to + 175	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount b	$R_{thJA}$	80	°C/W	
Junction-to-case (drain)		$R_{thJF}$	21	C/ VV	

#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. When mounted on 1" square PCB (FR-4 material)
- c. Parametric verification ongoing



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static				l			L	
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu A$		60	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu A$		3.0	3.5	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1.0		
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	250		
On-state drain current a	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	30	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A	-	0.010	0.012	Ω	
5.		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A, T <sub>J</sub> = 125 °C	-	-	0.021		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A, T <sub>J</sub> = 175 °C	-	-	0.025		
		V <sub>GS</sub> = 6 V	I <sub>D</sub> = 5 A	-	0.012	0.014		
Forward transconductance b	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 6 A		-	25	-	S	
Dynamic <sup>b</sup>								
Input capacitance	C <sub>iss</sub>		0 V V <sub>DS</sub> = 25 V, f = 1 MHz	-	2531	3165	pF	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	382	480		
Reverse transfer capacitance	C <sub>rss</sub>			-	153	195		
Total gate charge c	$Q_g$			-	45	68		
Gate-source charge c	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 30 \text{ V}, I_D = 12 \text{ A}$	-	9.9	-	nC	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	11.2	-	1	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.40	0.87	1.30	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	13	20		
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, \text{ R}_{L} = 2.5 \Omega$ $I_{D} \cong 12 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	12	18	- ns	
Turn-off delay time c	t <sub>d(off)</sub>			-	25	38		
Fall time c	t <sub>f</sub>			-	9	14		
Source-Drain Diode Ratings and Cha	racteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	_	67	Α	
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 1.7 A, V <sub>GS</sub> = 0		-	0.72	1.2	V	

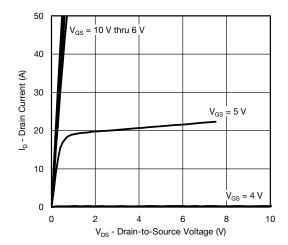
#### Notes

- d. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- e. Guaranteed by design, not subject to production testing
- f. Independent of operating temperature

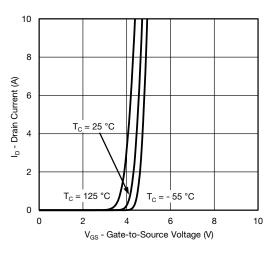
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



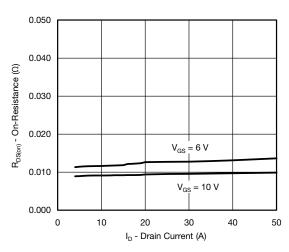
# TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



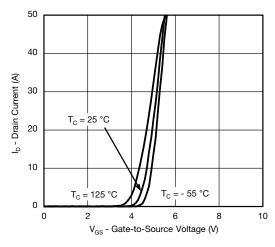
#### **Output Characteristics**



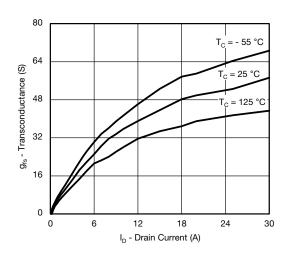
#### **Transfer Characteristics**



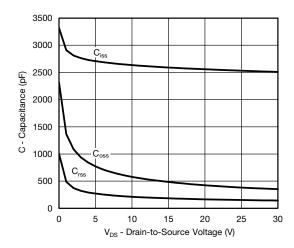
On-Resistance vs. Drain Current



#### **Transfer Characteristics**



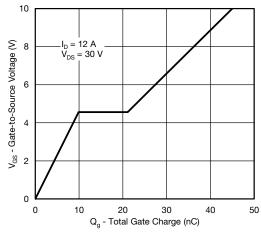
#### Transconductance



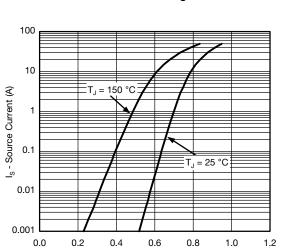
Capacitance



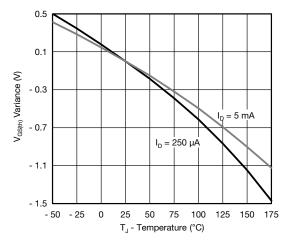
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



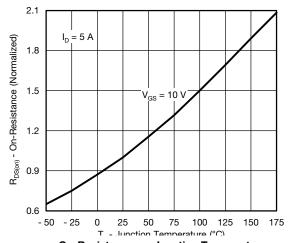
**Gate Charge** 



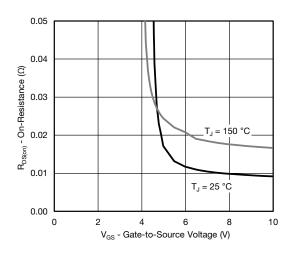
 $V_{SD}$  - Source-to-Drain Voltage (V) Source Drain Diode Forward Voltage



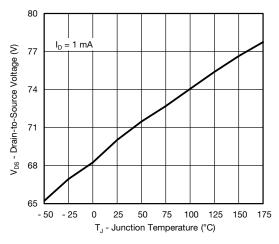
**Threshold Voltage** 



On-Resistance vs. Junction Temperature



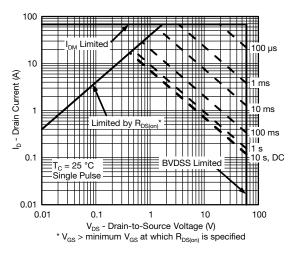
On-Resistance vs. Gate-to-Source Voltage



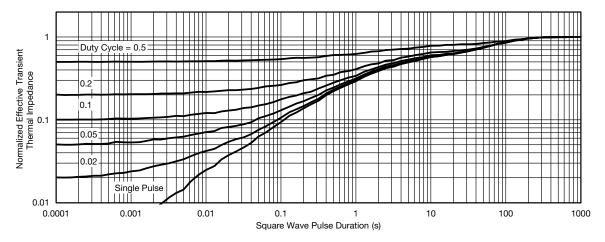
**Drain Source Breakdown vs. Junction Temperature** 



# **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



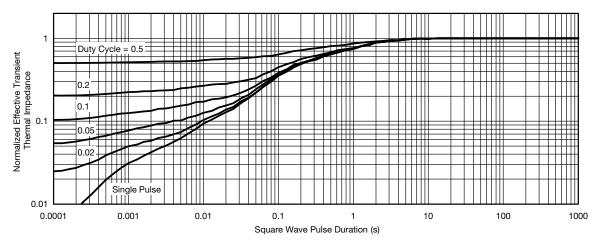
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg265673">www.vishay.com/ppg265673</a>.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







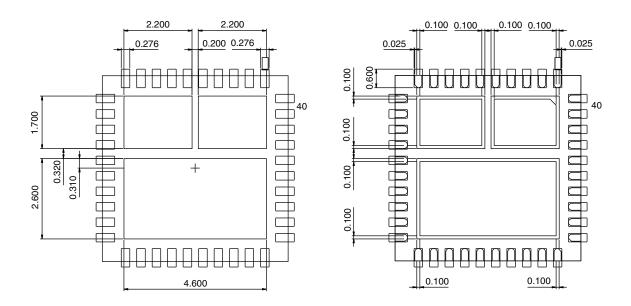
	MILLIM	IETERS	INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I. 11-Sep-06					

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



# Recommended Land Pattern PowerPAK® MLP66-40L



All Dimensions are in milimeters



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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