1.2 A Slew Rate Controlled Load Switch

DESCRIPTION

The SiP4282 series is a slew rate controlled high side switch. The switch is of a low on resistance p-channel MOSFET that supports continuous current up to 1.2 A.

The SiP4282 series operates with an input voltage from 1.8 V to 5.5 V. It offers under voltage lock out that turns the switch off when an input under voltage condition exists. The “A” option without UVLO extends the minimum operation voltage from 1.8 V down to 1.5 V. The SiP4282 is available in two different versions of slew rates, 100 µs and 1 ms. The SiP4282 series integrates load discharge circuit to ensure the discharge of capacitive load when the switch is disabled.

The SiP4282 features low input logic level to interface with low control voltage from microprocessors. This device has a very low operating current (typically 2.5 µA for SiP4282 and 50 pA for SiP4282A).

The SiP4282 is available in lead (Pb)-free package options including 6 pin PowerPAK® SC-75-6, and 4 pin TDFN4 1.2 mm x 1.6 mm DFN4 packages. The operation temperature range is specified from -40 °C to +85 °C.

The SiP4282 compact package options, operation voltage range, and low operating current make it a good fit for battery power applications.

FEATURES

- 1.8 V to 5.5 V input voltage range for SiP4282
- 1.5 V to 5.5 V input voltage range for SiP4282A
- Very low $R_{DS(on)}$, typically 105 mW at 5 V and 175 mW at 3 V
- Slew rate controlled turn-on time options: 100 µs and 1 ms
- Fast shutdown load discharge
- Low quiescent current, 4 µA for SiP4282
- Low quiescent current, 1 µA for SiP4282A
- Low shutdown current < 1 µA
- UVLO of 1.4 V for SiP4282
- PowerPAK SC-75 1.6 mm x 1.6 mm and TDFN4 1.2 mm x 1.6 mm packages
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Cellular telephones
- Digital still cameras
- Personal digital assistants (PDA)
- Hot swap supplies
- Notebook computers
- Personal communication devices
- Portable Instruments

TYPICAL APPLICATION CIRCUIT

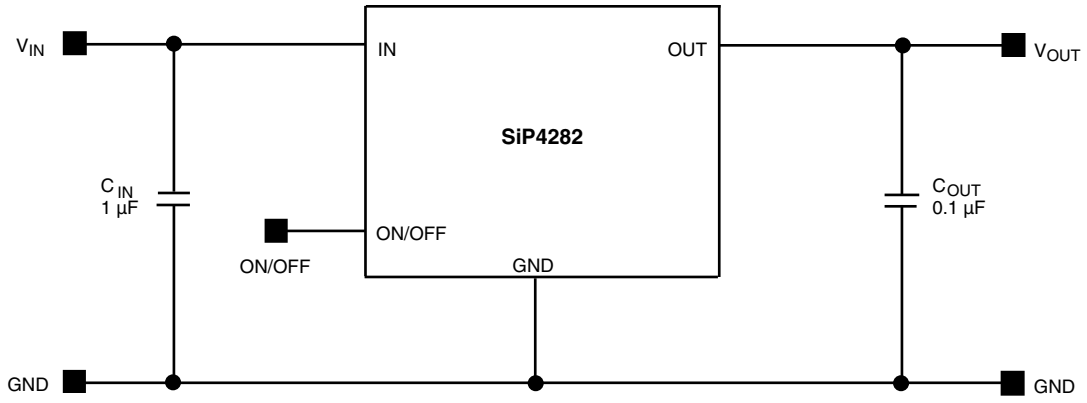


Fig. 1 - SiP4282 Typical Application Circuit

ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE	SLEW RATE (TYP.)	UNDER VOLTAGE LOCKOUT	MARKING	PART NUMBER
-40 °C to +85 °C	PowerPAK SC-75-6	100 µs	No	LExxx	SiP4282ADVP3-T1GE3
		100 µs	Yes	LFxxx	SiP4282DVP3-T1GE3
	TDFN4 1.2 x 1.6	100 µs	No	Bx	SiP4282ADNP3-T1GE4
		100 µs	Yes	Cx	SiP4282DNP3-T1GE4

Note
- xxx = lot code

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ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
Supply input voltage (V_{IN})		-0.3 to 6	V
Enable input voltage ($V_{ON / OFF}$)		-0.3 to 6	
Output voltage (V_{OUT})		-0.3 to V_{IN} + 0.3	
Maximum continuous switch current ($I_{max.}$)		1.4	A
Maximum pulsed current (I_{DM}) V_{IN}	$V_{IN} \geq 2.5$ V	3	
	$V_{IN} < 2.5$ V	1.6	
ESD rating (HBM)		4000	V
Junction temperature (T_J)		-40 to +125	°C
Thermal resistance (θ_{JA}) [a]	6 pin PPAK SC75 [b]	90	°C/W
	4 pin TDFN4 1.2 mm x 1.6 mm [c]	170	
Power fissipation (P_D) [a]	6 pin PPAK SC75 [b]	610	mW
	4 pin TDFN4 1.2 mm x 1.6 mm [c]	324	

Notes

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

a. Device mounted with all leads and power pad soldered or welded to PC board
b. Derate 11.1 mW/°C above T_A = 70 °C
c. Derate 5.9 mW/°C above T_A = 70 °C, see PCB layout

RECOMMENDED OPERATING RANGE

PARAMETER	LIMIT	UNIT
Input voltage range (V_{IN}) for SiP4282 version	1.8 to 5.5	V
Input voltage range (V_{IN}) for SiP4282A version	1.5 to 5.5	V
Operating temperature range	-40 to +85	°C

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_{IN} = 5, T_A = -40 °C to +85 °C (typical values are at T_A = 25 °C)	LIMITS -40 °C to +85 °C			UNIT
			MIN. [a]	TYP. [b]	MAX. [a]	
Operating voltage [c]	V_{IN}	For SiP4282xxx	1.8	-	5.5	V
Operating voltage		For SiP4282Axxx	1.5	-	5.5	
Under voltage lockout	V_{UVLO}	For SiP4282xxx, V_{IN} falling	1	1.4	1.8	
Under voltage lockout hysteresis	$V_{UVLO(hyh)}$	For SiP4282xxx	-	250	-	mV
Quiescent current	I_Q	For SiP4282xxx, on / off = active	-	2.5	4	µA
		For SiP4282Axxx, on / off = active	-	0.00005	1	
On-resistance	$R_{DS(on)}$	V_{IN} = 5 V, I_L = 500 mA, T_A = 25 °C	-	105	230	mΩ
		V_{IN} = 4.2 V, I_L = 500 mA, T_A = 25 °C	-	110	250	
		V_{IN} = 3 V, I_L = 500 mA, T_A = 25 °C	-	135	290	
		V_{IN} = 1.8 V, I_L = 500 mA, T_A = 25 °C	-	230	480	
		For SiP4282Axxx, V_{IN} = 1.5 V, I_L = 500 mA, T_A = 25 °C	-	350	520	
On-resistance temp. coefficient	TC_{RDS}		-	2800	-	ppm/°C
On / off input low voltage [d]	V_{IL}	For SiP4282Axxx, $V_{IN} \geq 1.5$ V to < 1.8 V	-	-	0.3	V
		$V_{IN} \geq 1.8$ V to < 2.7 V	-	-	0.4	
		$V_{IN} \geq 2.7$ V to ≤ 5.5 V	-	-	0.6	

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SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V_{IN} = 5, T_A = -40 °C to +85 °C (typical values are at T_A = 25 °C)	LIMITS -40 °C to +85 °C			UNIT
			MIN. [a]	TYP. [b]	MAX. [a]	
On / off input high voltage [d]	V_{IH}	$V_{IN} \geq 1.5$ V to < 2.7 V	1.3	-	-	V
		$V_{IN} \geq 2.7$ V to < 4.2 V	1.5	-	-	
		$V_{IN} \geq 4.2$ V to ≤ 5.5 V	1.8	-	-	
On / off input leakage	I_{SINK}	$V_{On / off}$ = 5.5 V	-	-	1	µA
Output pulldown resistance	R_{PD}	On / off = Inactive, T_A = 25 °C	-	180	250	Ω
SiP4282xxx3 and SiP4282Axxx3 Versions						
Output turn-on delay time	$t_{d(on)}$	V_{IN} = 5 V, R_{LOAD} = 10 Ω, T_A = 25 °C	-	20	40	µs
Output turn-on rise time	$t_{(on)}$	V_{IN} = 5 V, R_{LOAD} = 10 Ω, T_A = 25 °C	-	140	180	
Output turn-off delay time	$t_{d(off)}$	V_{IN} = 5 V, R_{LOAD} = 10 Ω, T_A = 25 °C	-	4	10	

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

c. Part requires minimum start-up of $V_{IN} \geq 2$ V to ensure operation down to 1.8 V

d. For V_{IN} outside this range consult typical on / off threshold curve

PIN CONFIGURATION

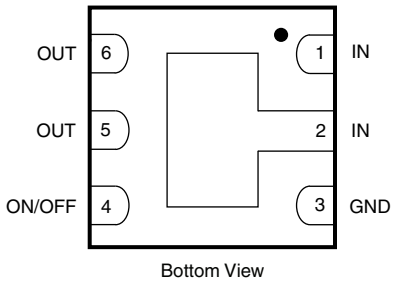


Fig. 2 - PPAK SC75-6 Package

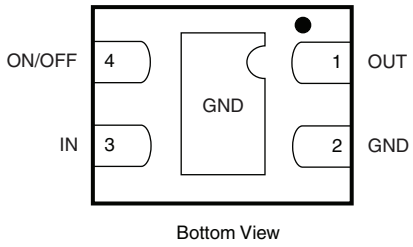


Fig. 3 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION			
PIN NUMBER		NAME	FUNCTION
PPAK	TDFN4		
1, 2	3	IN	This pin is the p-channel MOSFET source connection. Bypass to ground through a 1 µF capacitor
3	2	GND	Ground connection
4	4	ON/OFF	Enable input
5, 6	1	OUT	This pin is the p-channel MOSFET drain connection. Bypass to ground through a 0.1 µF capacitor

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TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

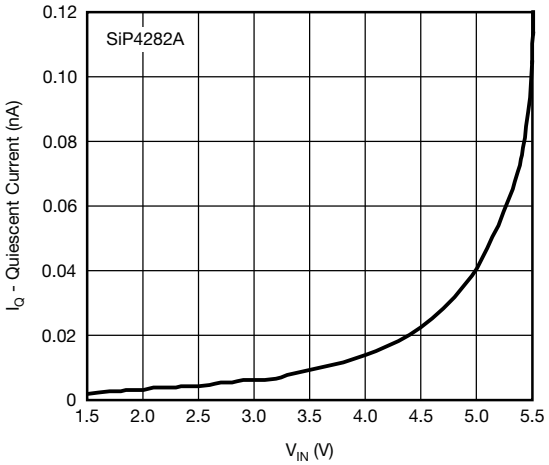


Fig. 4 - Quiescent Current vs. Input Voltage

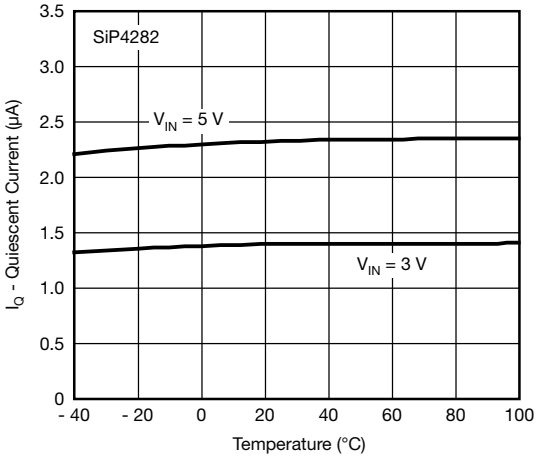


Fig. 7 - Quiescent Current vs. Temperature

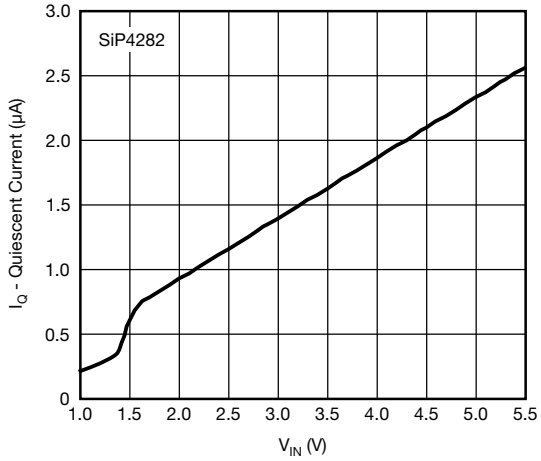


Fig. 5 - Quiescent Current vs. Input Voltage

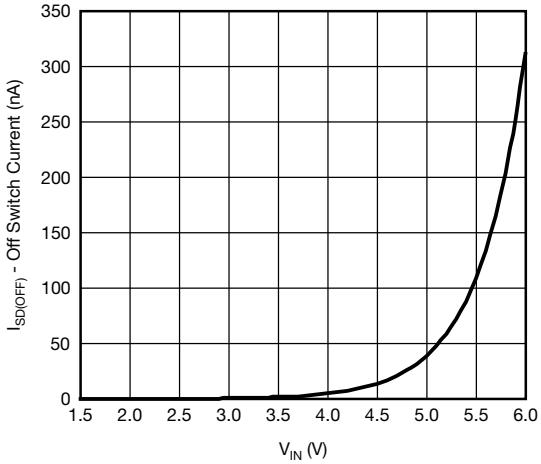


Fig. 8 - Off Switch Current vs. Input Voltage

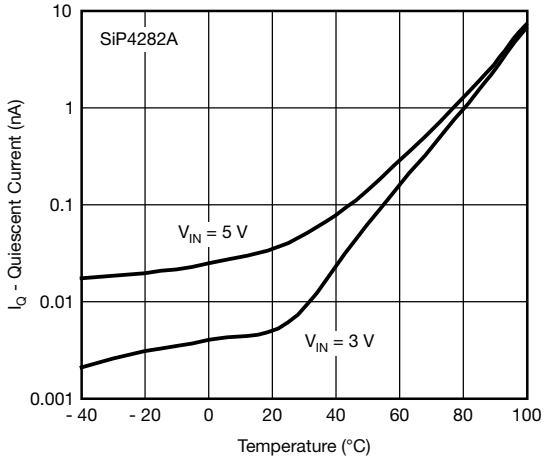


Fig. 6 - Quiescent Current vs. Temperature

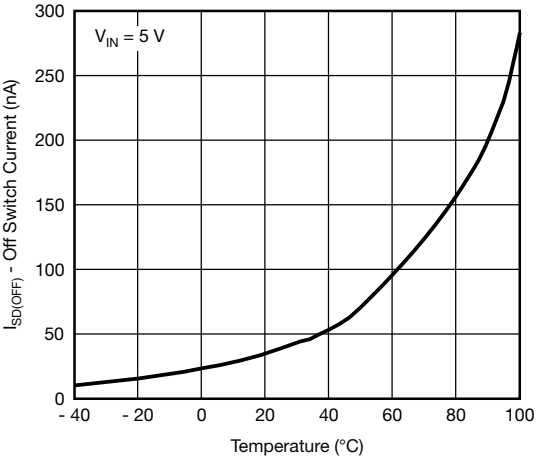


Fig. 9 - Off Switch Current vs. Temperature

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TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

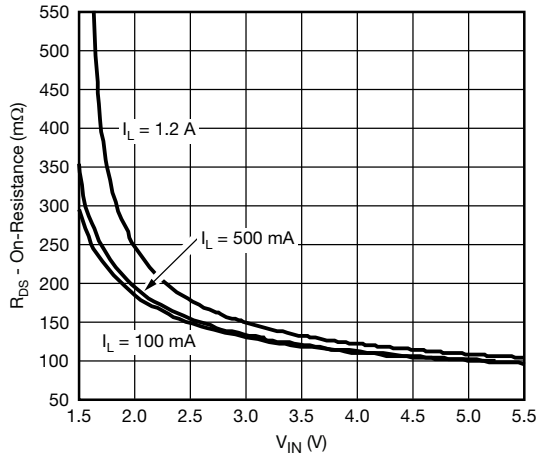


Fig. 10 - $R_{DS(on)}$ vs. Input Voltage

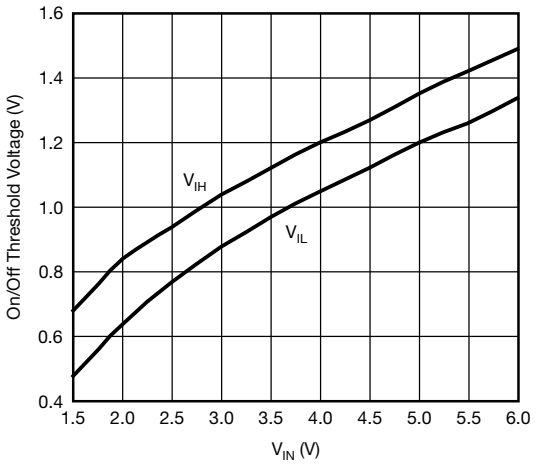


Fig. 13 - On / Off Threshold vs. Input Voltage

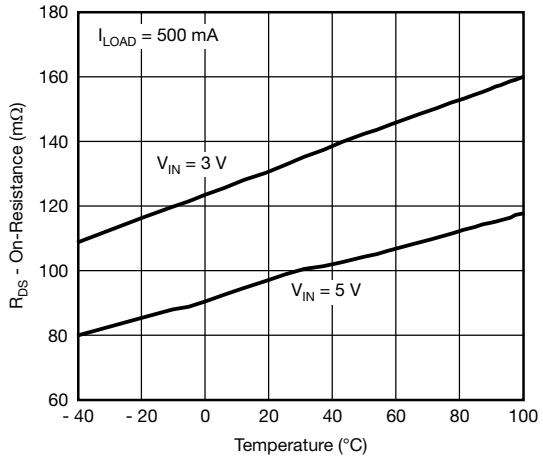


Fig. 11 - $R_{DS(on)}$ vs. Temperature

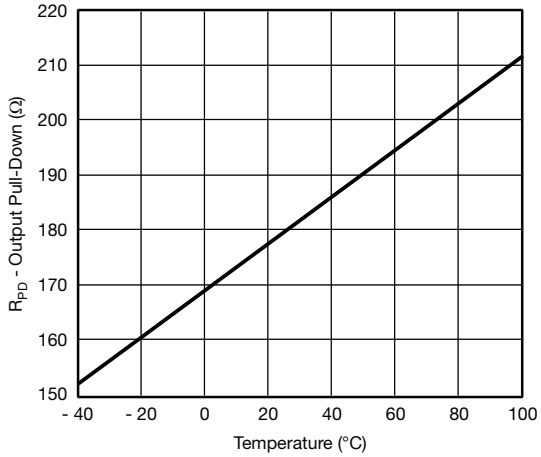
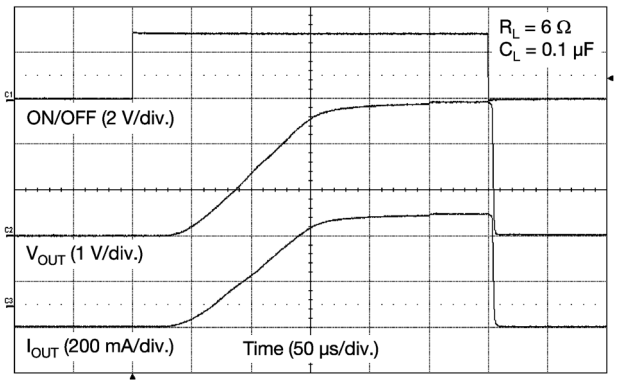


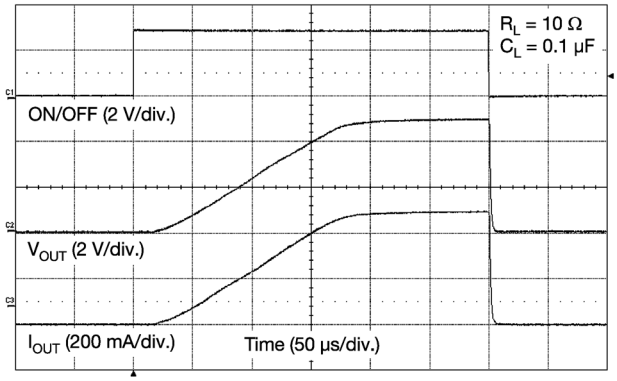
Fig. 12 - Output Pull-Down Resistance vs. Temperature

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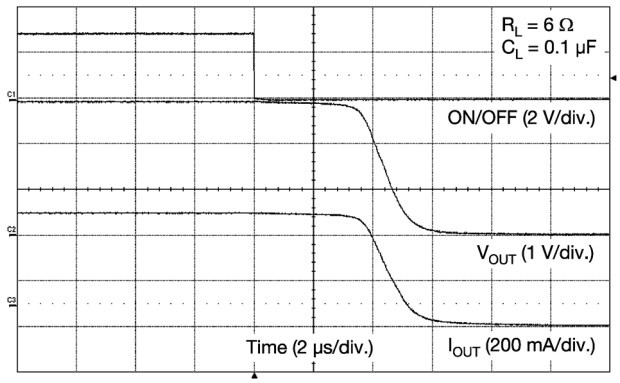
TYPICAL WAVEFORMS



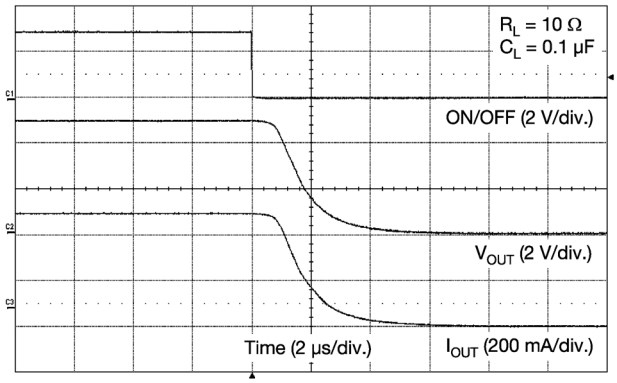
SiP4282xxx3 and SiP4282Axxx3 Switching
(V_{IN} = 3 V)



SiP4282xxx3 and SiP4282Axxx3 Switching
(V_{IN} = 5 V)



SiP4282xxx3 and SiP4282Axxx3 Turn-Off
(V_{IN} = 3 V)



SiP4282xxx3 and SiP4282Axxx3 Turn-Off
(V_{IN} = 5 V)

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BLOCK DIAGRAM

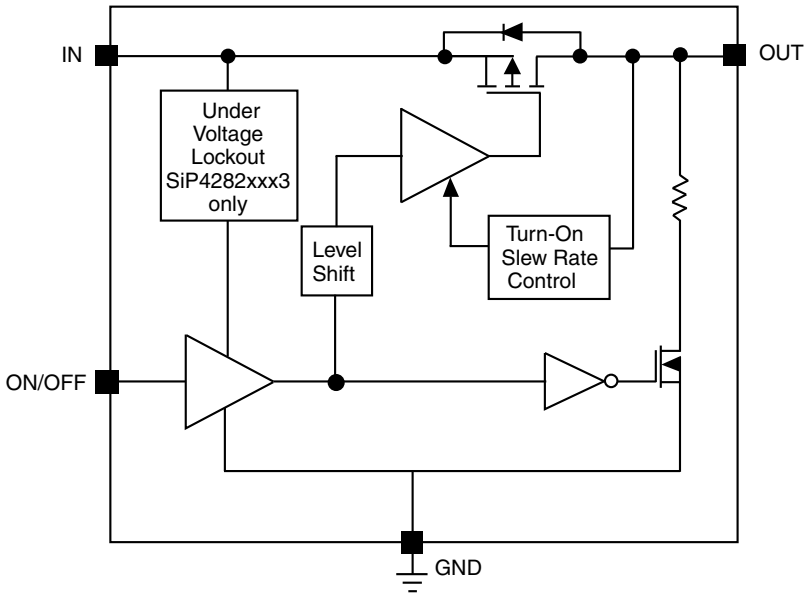


Fig. 14 - SiP4282 Functional Block Diagram

PCB LAYOUT

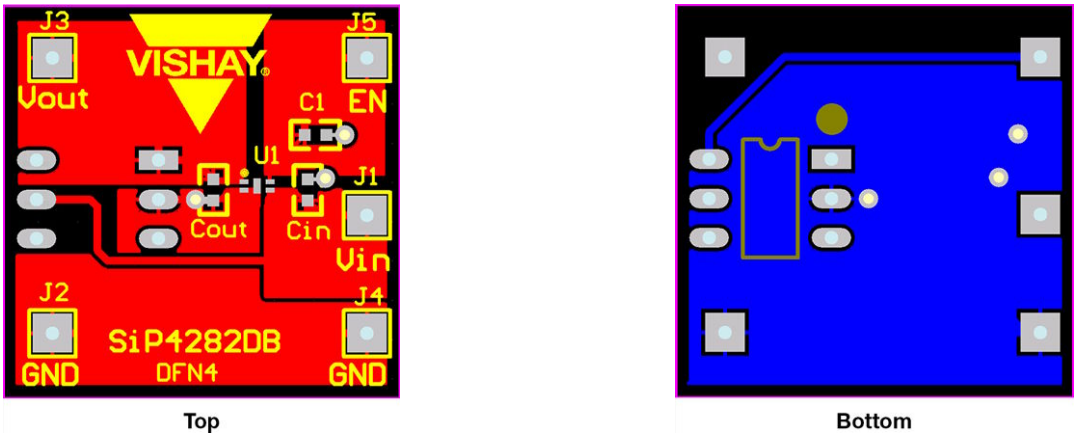


Fig. 15 - TDFN4 1.2 mm x 1.6 mm PCB Layout

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DETAILED DESCRIPTION

The SiP4282 is a p-channel MOSFET power switches designed for high-side slew rate controlled load-switching applications. Once turned on, the slew-rate control circuitry is activated and current is ramped in a linear fashion until it reaches the level required for the output load condition. This is accomplished by first elevating the gate voltage of the MOSFET up to its threshold voltage and then by linearly increasing the gate voltage until the MOSFET becomes fully enhanced. At this point, the gate voltage is then quickly increased to the full input voltage to reduce $R_{DS(on)}$ of the MOSFET switch and minimize any associated power losses.

All versions features a shutdown output discharge circuit which is activated at shutdown (when the part is disabled through the on / off pin) and discharges the output pin through a small internal resistor hence, turning off the load. For SiP4282-3, in instances where the input voltage falls below 1.4 V (typically) the under voltage lock-out circuitry protects the MOSFET switch from entering the saturation region or operation by shutting down the chip.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 1 µF or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the SiP4282 to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 µF capacitor or larger across V_{OUT} and GND is recommended to insure proper slew operation. C_{OUT} may be increased without limit to accommodate any load transient condition with only minimal affect on the SiP4282 turn on slew rate time. There are no ESR or capacitor type requirement.

Enable

The on / off pin is compatible with both TTL and CMOS logic voltage levels.

Protection Against Reverse Voltage Condition

The p-channel MOSFET pass transistor has an intrinsic diode that is reversed biased when the input voltage is greater than the output voltage. Should V_{OUT} exceed V_{IN}, this intrinsic diode will become forward biased and allow excessive current to flow into the IC thru the V_{OUT} pin and potentially damage the IC device. Therefore extreme care should be taken to prevent V_{OUT} from exceeding V_{IN}.

In conditions where V_{OUT} exceeds V_{IN} a Schottky diode in parallel with the internal intrinsic diode is recommended to protect the SiP4282.

Thermal Considerations

The SiP4282 is designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 1.2 A, as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 90 °C/W) the power pad of the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependent on the maximum junction temperature, T_J (max.) = 125 °C, the junction-to-ambient thermal resistance for the SC-75 PPAK package, θ_{J-A} = 90 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\ (max.) = \frac{T_J\ (max.) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{90}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 610 mW.

So long as the load current is below the 1.2 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(on)}$ at 25 °C occurs at an input voltage of 1.8 V and is equal to 480 mΩ. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 3300 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 480 mΩ x (1 + 0.0033 x (70 °C - 25 °C)) = 551 mΩ

The maximum current limit is then determined by

$$I_{LOAD}\ (max.) < \sqrt{\frac{P\ (max.)}{R_{DS(on)}}}$$

which in case is 1.05 A. Under the stated input voltage condition, if the 1.05 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

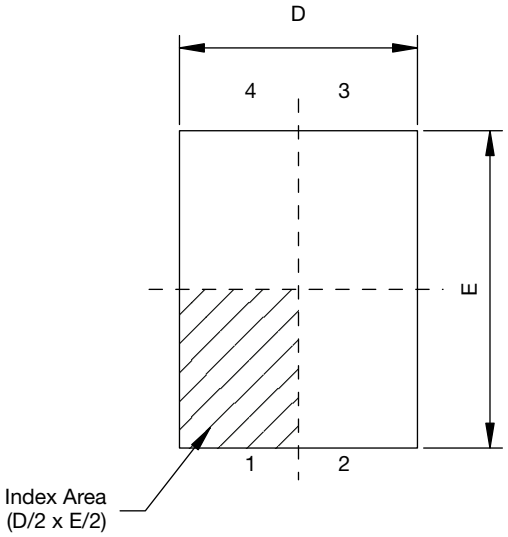
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PRODUCT SUMMARY				
Part number	SiP4282	SiP4282	SiP4282A	SiP4282A
Description	1.8 V to 5.5 V, 105 mΩ, 100 µs rise time, with UVLO	1.8 V to 5.5 V, 105 mΩ, 100 µs rise time, with UVLO	1.5 V to 5.5 V, 105 mΩ, 100 µs rise time	1.5 V to 5.5 V, 105 mΩ, 100 µs rise time
Configuration	Single	Single	Single	Single
Slew rate time (µs)	140	140	140	140
On delay time (µs)	20	20	20	20
Input voltage min. (V)	1.8	1.8	1.5	1.5
Input voltage max. (V)	5.5	5.5	5.5	5.5
On-resistance at input voltage min. (mΩ)	230	230	350	350
On-resistance at input voltage max. (mΩ)	105	105	105	105
Quiescent current at input voltage min. (µA)	1	1	0.00001	0.00001
Quiescent current at input voltage max. (µA)	2.5	2.5	0.00005	0.00005
Output discharge (yes / no)	Yes	Yes	Yes	Yes
Reverse blocking (yes / no)	No	No	No	No
Continuous current (A)	1.2	1.2	1.2	1.2
Package type	TDFN4	PowerPAK SC-75-6	TDFN4	PowerPAK SC-75-6
Package size (W, L, H) (mm)	1.2 x 1.6 x 0.5	0.75 x 1.6 x 0.5	1.2 x 1.6 x 0.5	0.75 x 1.6 x 0.5
Status code	2	2	2	2
Product type	Slew rate	Slew rate	Slew rate	Slew rate
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

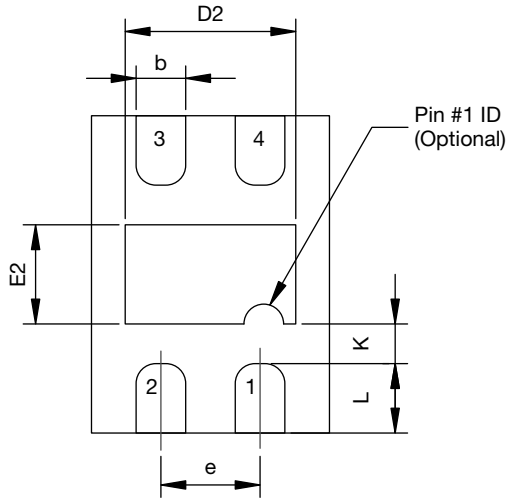
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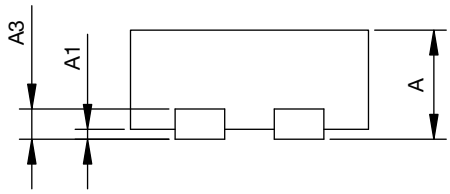
TDFN4 1.2 x 1.6 Case Outline



Top View



Bottom View



Side View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.45	0.55	0.60	0.017	0.022	0.024
A1	0.00	-	0.05	0.00	-	0.002
A3	0.15 REF. or 0.127 REF. (1)			0.006 or 0.005 (1)		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.15	1.20	1.25	0.045	0.047	0.049
D2	0.81	0.86	0.91	0.032	0.034	0.036
e	0.50 BSC			0.020		
E	1.55	1.60	1.65	0.061	0.063	0.065
E2	0.45	0.50	0.55	0.018	0.020	0.022
K	0.25 typ.			0.010 typ.		
L	0.25	0.30	0.35	0.010	0.012	0.014
ECN: T16-0143-Rev. C, 18-Apr-16 DWG: 5995						

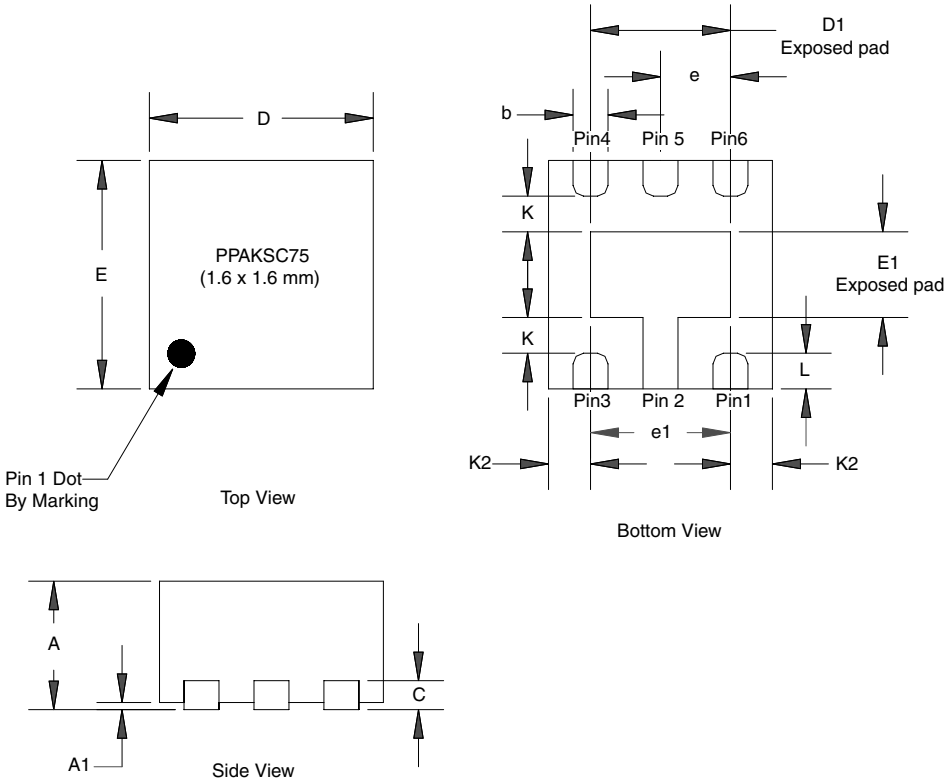
Note

(1) The dimension depends on the leadframe that assembly house used.

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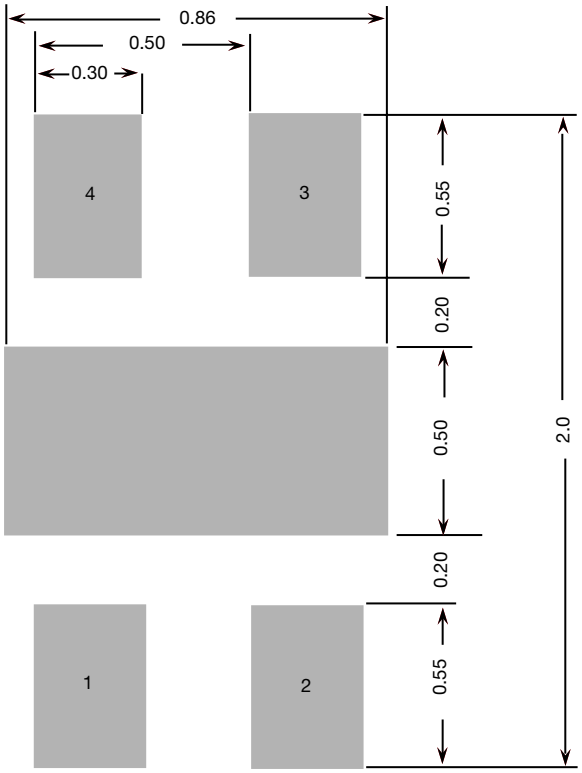
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PowerPAK® SC75-6L (Power IC only)



DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0	-	0.05	0	-	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.15	0.20	0.25	0.006	0.008	0.010
D	1.55	1.60	1.65	0.0061	0.063	0.065
D1	0.95	1.00	1.05	0.037	0.039	0.041
E	1.55	1.60	1.65	0.061	0.063	0.065
E1	0.55	0.60	0.65	0.022	0.024	0.026
e	0.50 BSC			0.020 BSC		
e1	1.00 BSC			0.039 BSC		
K	0.15	-	-	0.006	-	-
K2	0.20	-	-	0.008		
L	0.20	0.25	0.30	0.008	0.010	0.012
ECN: S-60845-Rev. B, 22-May-06 DWG: 5953						

RECOMMENDED MINIMUM PADS FOR TDFN4 1.2 x 1.6



Recommended Minimum Pads
Dimensions in mm

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