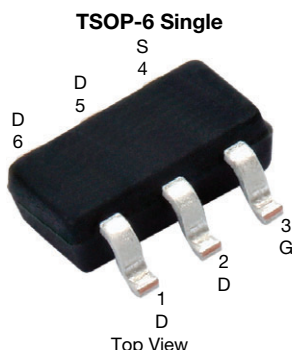


# Automotive P-Channel 40 V (D-S) 175 °C MOSFET

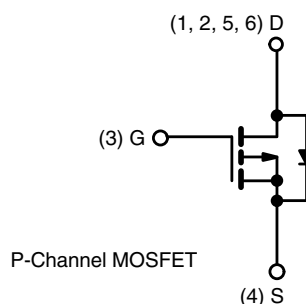


Marking Code: 8V

PRODUCT SUMMARY	
$V_{DS}$ (V)	-40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.058
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.092
$I_D$ (A)	-6.9
Configuration	Single

## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free and halogen-free	SQ3419EV (for detailed order number please see <a href="http://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	-40	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current	$T_C = 25$ °C	$I_D$	-6.9	A
	$T_C = 125$ °C		-4	
Continuous source current (diode conduction)		$I_S$	-6.3	
Pulsed drain current		$I_{DM}$	-27	
Single pulse avalanche current		$I_{AS}$	-16.5	
Single pulse avalanche energy		$E_{AS}$	13.6	mJ
Maximum power dissipation <sup>a</sup>	$T_C = 25$ °C	$P_D$	5	
	$T_C = 125$ °C		1.6	W
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	$R_{thJA}$	110	°C/W
		$R_{thJF}$	30	

## Notes

- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)

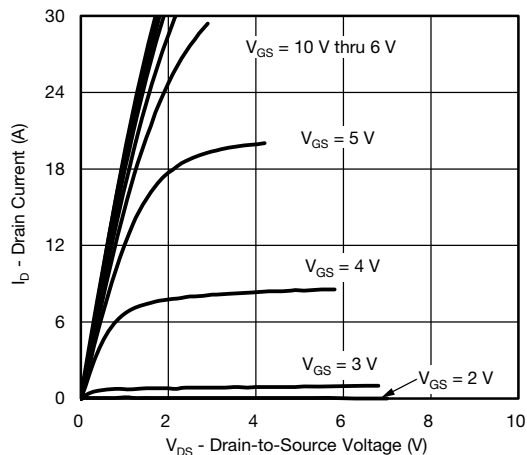
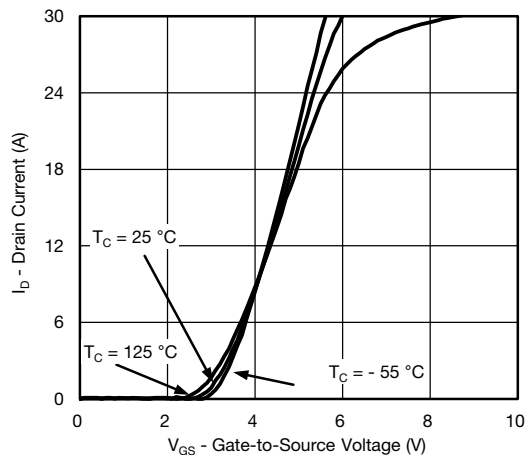
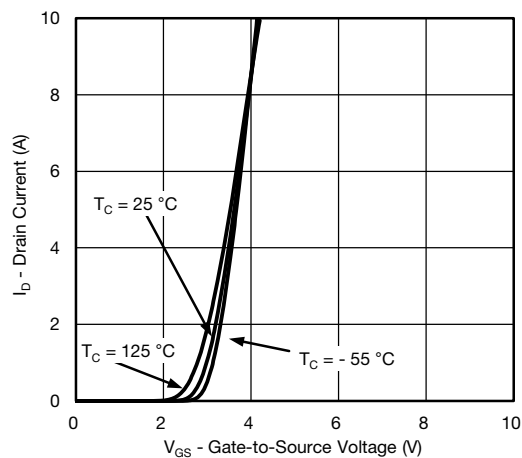
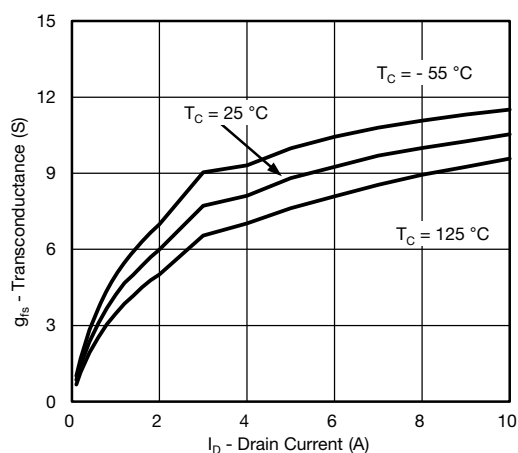
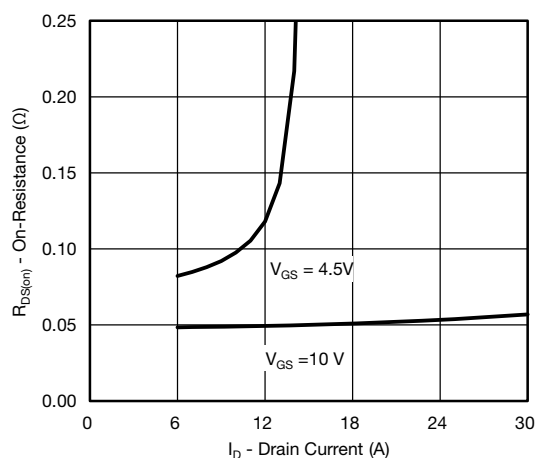
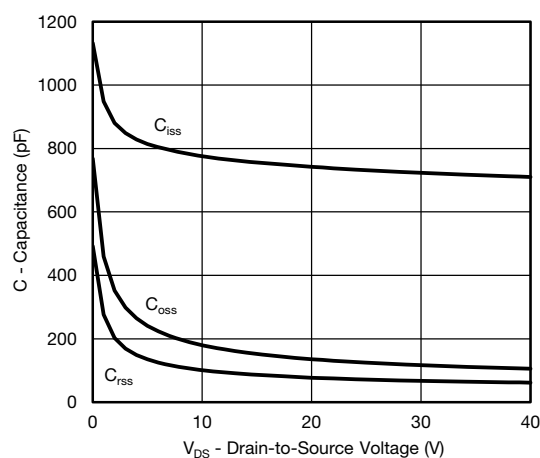


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA		-40	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-1.5	-2.0	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V	-	-	-1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -5 V	-10	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -2.5 A	-	0.048	0.058	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -2.5 A, T <sub>J</sub> = 125 °C	-	0.075	-	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -2.5 A, T <sub>J</sub> = 175 °C	-	0.086	-	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2 A	-	0.076	0.092	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -20 V, I <sub>D</sub> = -4 A		-	8	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -20 V, f = 1 MHz	-	742	990	pF
Output capacitance	C <sub>oss</sub>			-	136	180	
Reverse transfer capacitance	C <sub>rss</sub>			-	77	100	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -4.5 V	V <sub>DS</sub> = -20 V, I <sub>D</sub> = -4 A	-	7.5	11.3	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	2.5	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	3.9	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		2.6	5.3	7.9	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -20 V, R <sub>L</sub> = 5 Ω I <sub>D</sub> ≅ -4 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		-	8	12	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	24	36	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	26	39	
Fall time <sup>c</sup>	t <sub>f</sub>			-	31	47	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-27	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -1.6 A, V <sub>GS</sub> = 0 V		-	-0.8	-1.2	V

**Notes**

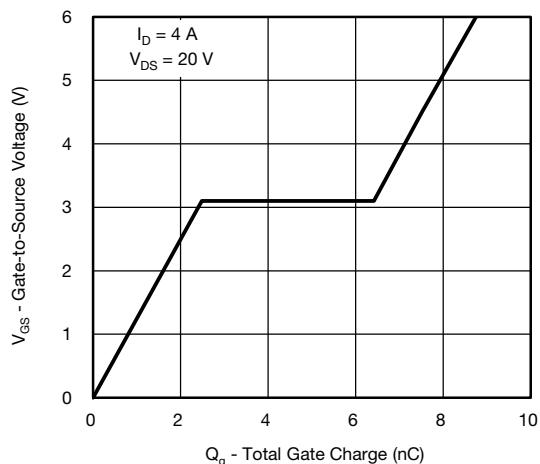
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

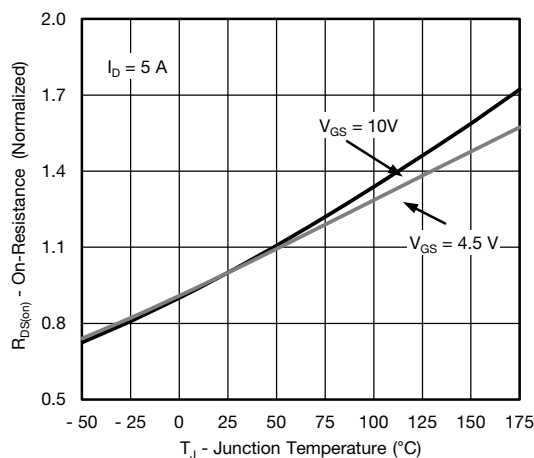
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**



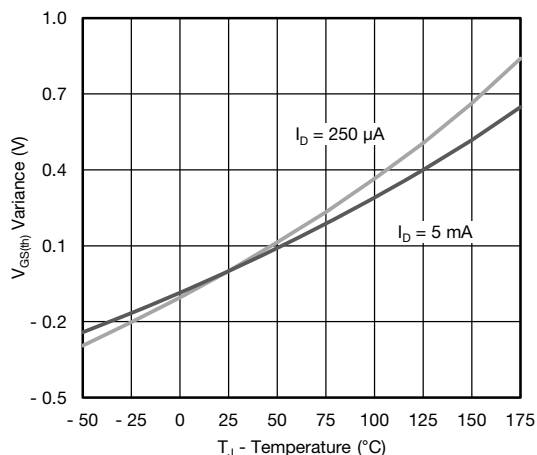
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



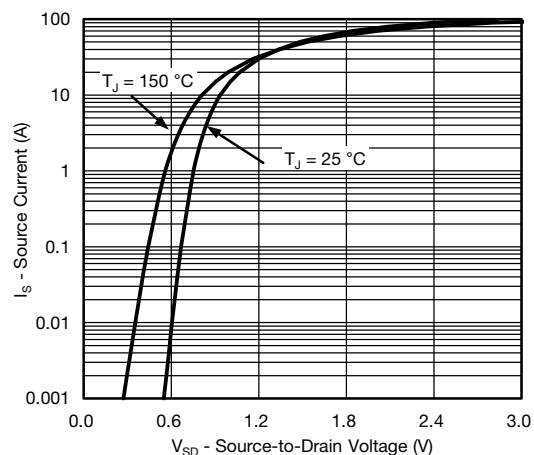
**Gate Charge**



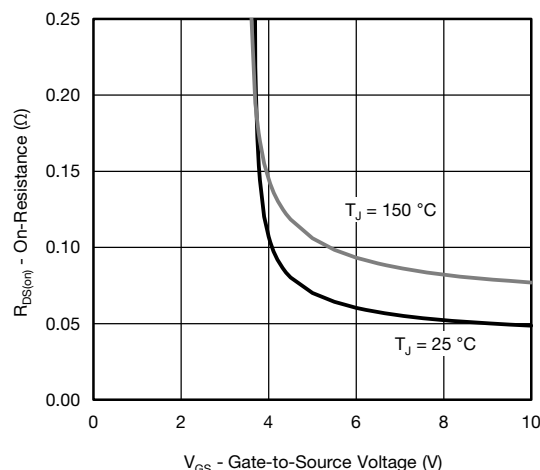
**On-Resistance vs. Junction Temperature**



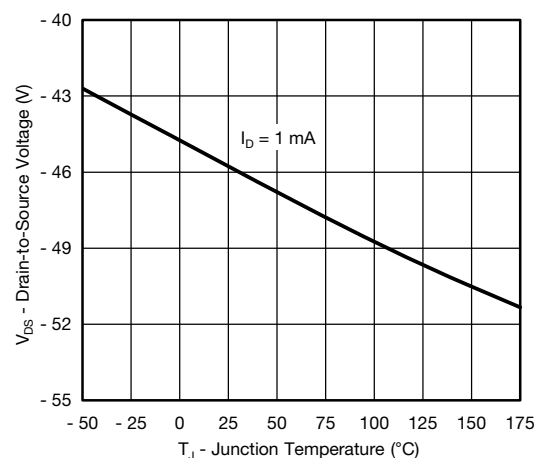
**Threshold Voltage**



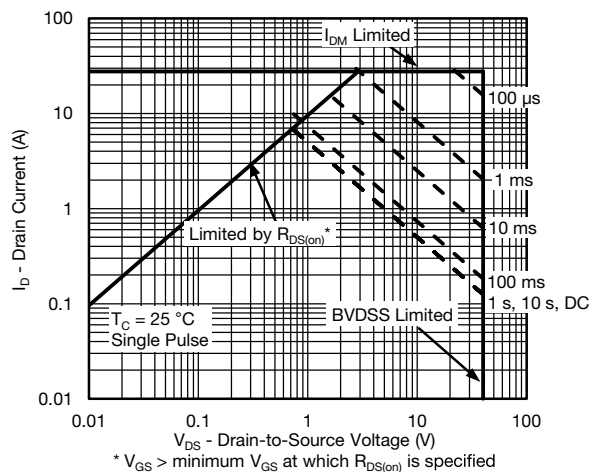
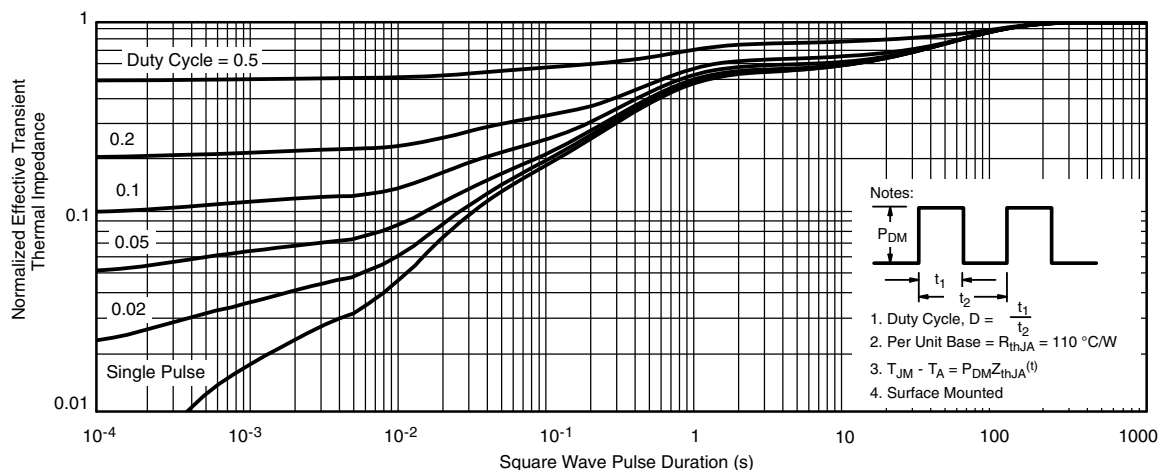
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

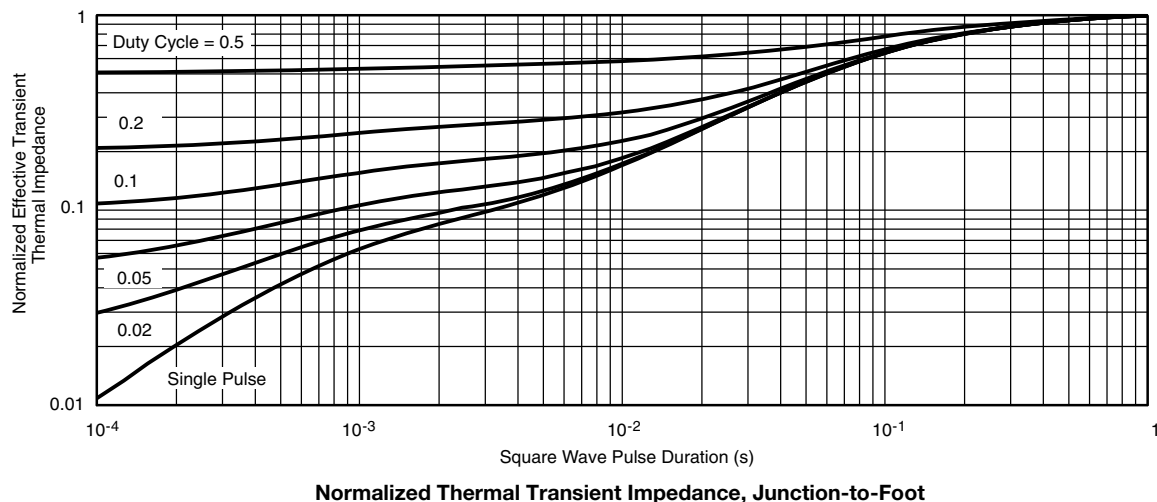


**Drain Source Breakdown vs. Junction Temperature**

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Safe Operating Area**

**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



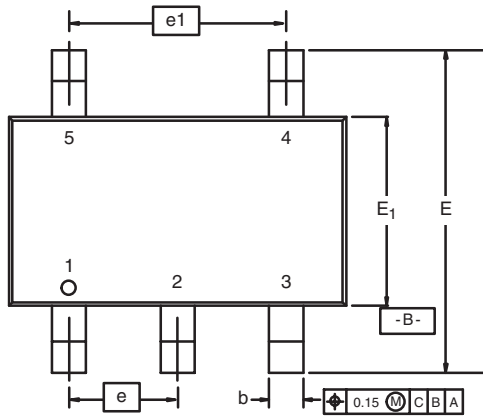
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

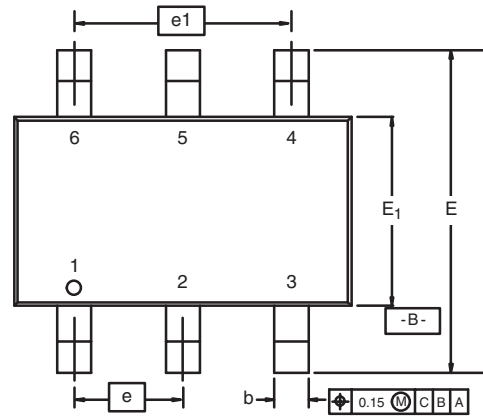
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## TSOP: 5/6-LEAD

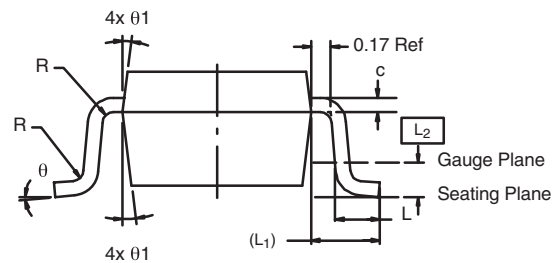
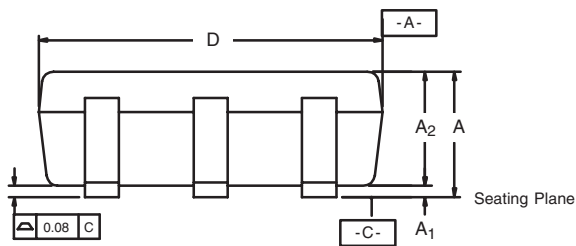
JEDEC Part Number: MO-193C



5-LEAD TSOP

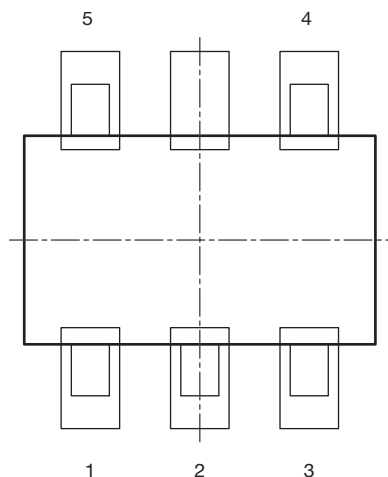


6-LEAD TSOP

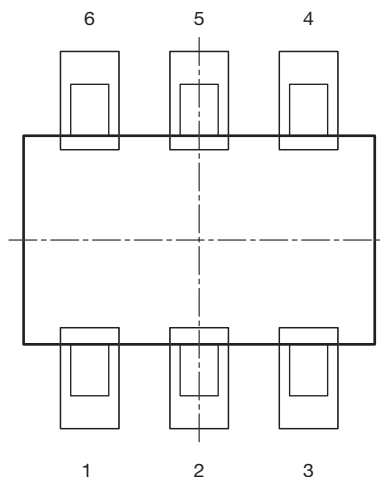


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A <sub>1</sub>	0.01	-	0.10	0.0004	-	0.004
A <sub>2</sub>	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e <sub>1</sub>	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L <sub>1</sub>	0.60 Ref			0.024 Ref		
L <sub>2</sub>	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ <sub>1</sub>	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

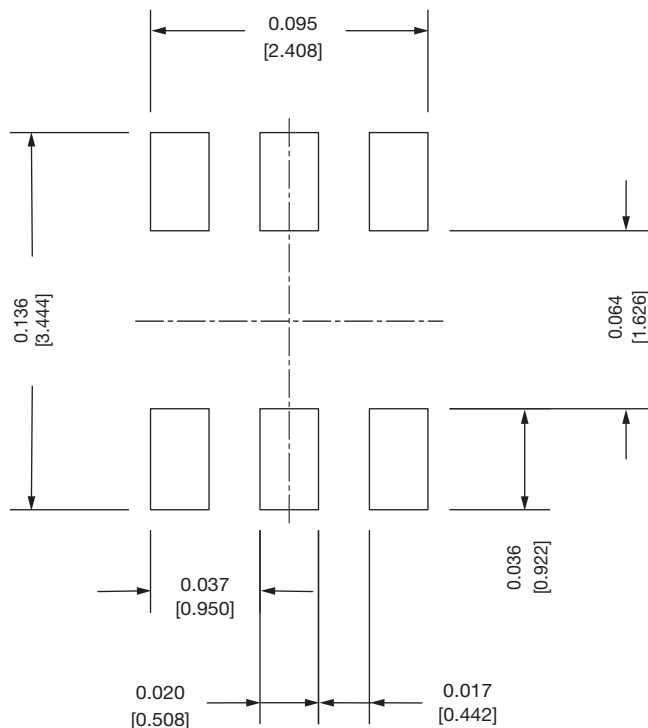
## Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


**Note**

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022  
DWG: 3010





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