Half-Bridge Controller with Primary MOSFET Drivers for Intermediate Bus Converters

DESCRIPTION

SiP11206 is a controller for the primary side of a half-bridge intermediate bus converter (IBC). It is ideally suited for isolated applications such as telecom, data communications and other products requiring an IBC architecture and conversion of standard bus voltages such as 48 V to a lower intermediate voltage, where high efficiency is required at low output voltages (24 V, 12 V, 9 V or 5 V).

Designed to operate within the telecom voltage range of 36 V to 75 V and withstand 100 V transients for a period of 100 ms, the IC is designed for controlling and driving both the low- and high-side switching devices of a half-bridge converter.

The SiP11206 operates with a fixed duty cycle to provide the highest efficiency over a wide input voltage range. SiP11206 has advanced current monitoring and control circuitry, which allows the user to set the maximum current in the primary circuit. This feature acts as protection against overcurrent, output short circuit. Current sensing is by means of a sense resistor connected in series with the primary low-side MOSFET.

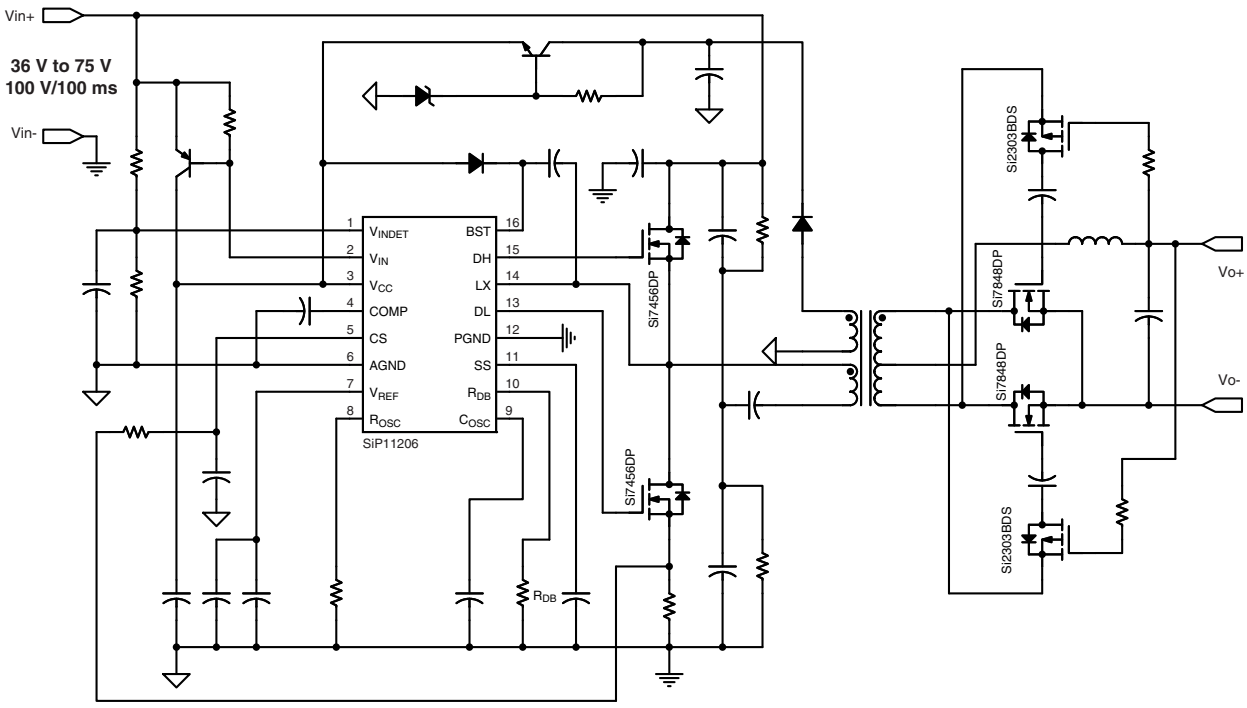
FEATURES

- 36 V to 75 V input voltage range
- Withstand 100 V, 100 ms transient capability
- Integrated ± 1.6 A typical high- and low-side MOSFET drivers
- Oscillator frequency is programmable from 200 kHz to 1 MHz and can be externally synchronized
- High voltage pre-regulator operates during start-up
- Current sensing on primary low-side switch
- Hiccup mode
- System low input voltage detection
- Chip UVLO function
- Programmable soft-start function
- Over temperature protection (160 °C)
- Greater than 95 % efficiency

APPLICATIONS

- Intermediate bus architectures
- Telecom and Datacom
- Routers and servers
- Storage area network
- Base station
- 1/8 and 1/4 bricks

TYPICAL APPLICATION CIRCUIT



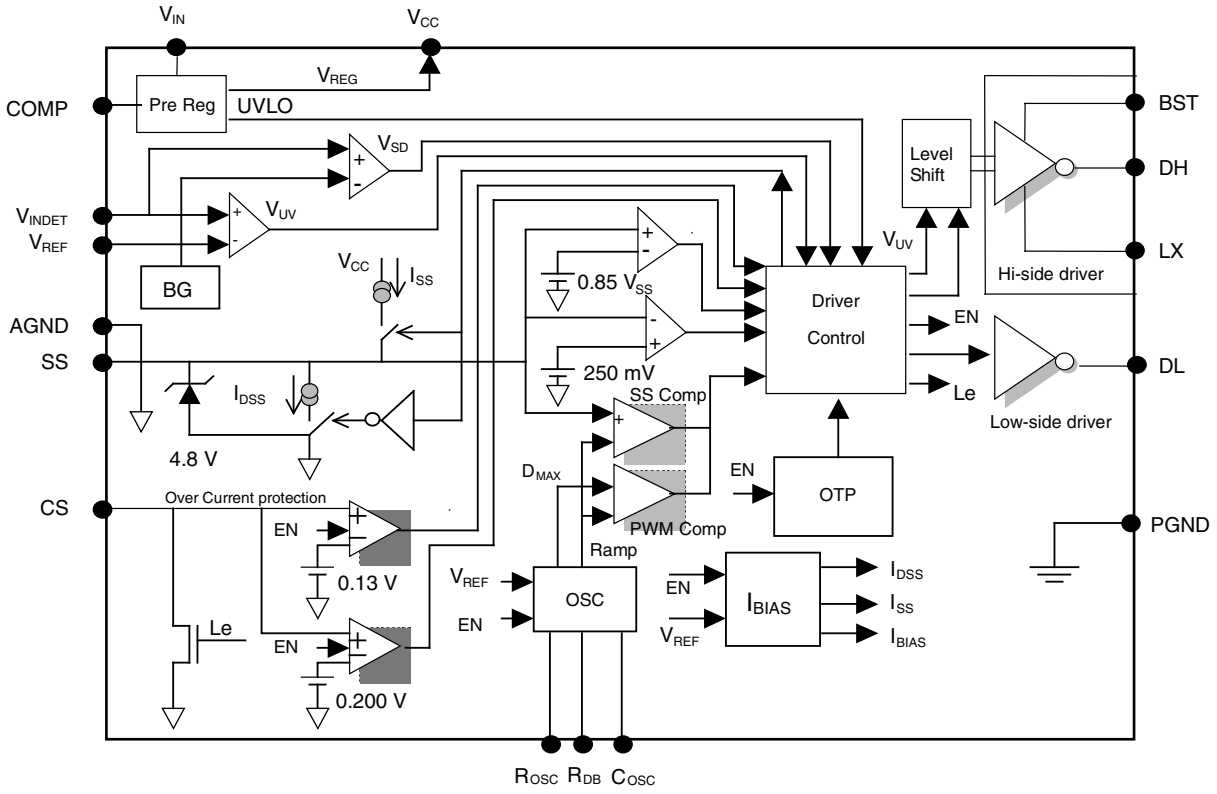
TECHNICAL DESCRIPTION

SiP11206 is a switching controller on the primary side of a half-bridge intermediate bus converter. With 100 V depletion mode MOSFET in the chip, the SiP11206 is capable of being powered directly from the high voltage bus to V_{CC} through an external PNP pass transistor, or may be powered by an external supply directly to the V_{CC} pin.

Without the use of an external pass transistor, failure of the converter output to power V_{CC} above the V_{REG} level will result in over temperature protection activating hiccup operation whenever the pre-regulator power dissipation becomes excessive. The external high- and low-side N-Channel power MOSFETs are driven by a built in driver with ± 1.6 A peak current capability.

SiP11206 is available in the MLP44-16 PowerPAK® package and TSSOP-16 PowerPAK® package and is specified over the ambient temperature range of - 40 °C to + 85 °C

SIP11206 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS all voltages referenced to GND = 0 V			
Parameter		**Limit**	**Unit**
V_{IN}, V_{LX}	Continuous	80	V
	100 ms	100	
V_{CC}		14.5	
V_{BST}	Continuous	95	
	100 ms	112	
V_{BST} - V_{LX}		15	
Logic Inputs		- 0.3 to V_{CC} + 0.3	
Linear Inputs		- 0.3 to V_{CC} + 0.3	
HV Pre-Regulator Input Current (continuous)		10	mA
Storage Temperature		- 65 to 150	°C
Maximum Junction Temperature		150	
Power Dissipation	PowerPAK MLP44-16[a, b]	2564	mW
	PowerPAK TSSOP-16[a, c]	2630	
Thermal Impedance (Θ_{JA})	PowerPAK MLP44-16[a, b]	39	°C/W
	PowerPAK TSSOP-16[a, c]	38	

Notes:
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 25.6 mW/°C above 25 °C.
c. Derate 26.3 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE all voltages referenced to GND = 0 V			
Parameter		**Limit**	**Unit**
V_{IN}	Continuous	36 to 75	V
	100 ms	100	
V_{BST}		V_{IN} + 10.5 to V_{IN} + 13.2	
V_{BST} - V_{LX}		10.5 to 13.2	
V_{CC}		10.5 to 13.2	
Logic Inputs		- 0.3 to V_{CC} + 0.3	
Linear Inputs		- 0.3 to V_{CC} + 0.3	
F_{OSC}		200 to 1000	kHz
R_{OSC}		40 to 200	kΩ
C_{OSC}		100 to 220	pF
C_{SS}		10 to 100	nF
C_{COMP}		2.2	
V_{REF} Capacitor to GND		1	µF
C_{BOOST}		0.1	
V_{CC} Capacitor to GND		4.7	

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified T_A = - 40 °C to + 85 °C, F_{OSC} = 800 kHz, 10.5 V ≤ V_{CC} ≤ 13.2 V, V_{INDET} = 4.8 V, V_{IN} = 48 V, R_{DB} = 47.5 kΩ, R_{OSC} = 47.5 kΩ, C_{OSC} = 100 pF	Limits Min.	Typ.	Max.	Unit
Pre-Regulator						
V_{IN} Range	V_{IN}		36	48	75	V
Pre-Reg Current (cut-off)	I_{VINLKG}	V_{IN} = 75 V, V_{CC} > 10.5 V			10	µA
Pre-Reg Current (standby)	I_{VINSD}	V_{IN} = 75 V, V_{INDET} = 0 V		90	200	
Pre-Reg Current (switching)	I_{VINSW}	V_{IN} = 75 V, V_{INDET} = 7.5 V	3.3	6.0	8.7	mA
Pre-Reg Output Voltage	V_{REG}	V_{CC} Voltage with V_{IN} = 48 V	7.8	9.3	10.4	V
Pre-Reg Drive Current	I_{START}	V_{CC} < V_{REG}	20			mA
Pre-Reg Load Regulation	LDR	I_{LOAD}: 0 to 20 mA		100		mV
Pre-Reg Line Regulation	LNR			0.05		%/V
Regulator Compensation	I_{SRC}	V_{CC} = 12 V	- 35	- 20	- 10	µA
	I_{SNK}		40	87	130	
V_{CC} Supply Voltage						
V_{CC} Range	V_{CC}		10.5	12	13.2	V
Shut Down Current	I_{SD}	V_{INDET} = 0 V	50	150	350	µA
Quiescent Current	I_Q	V_{INDET} < V_{REF}	4.0	5.0	6.2	mA
Supply Current	I_{CC}	V_{INDET} > V_{REF}	5.5	7.2	9.5	
UVLO Off-Threshold	$UVLO_H$	V_{CC} rising	7.6	9.0	10	V
Hysteresis	H_{UVLO}			1.2		
V_{CC} Clamp Voltage	V_{CLAMP}	Force 20 mA into V_{CC}	14	15.3	16.2	
Current Sense						
Current Limit Threshold 1 (MOC)[a]	V_{MOC}	I_{SS} = 20 µA, C_{SS}= 1 nF	105	130	160	mV
Current Limit Threshold 2 (SOC)[b]	V_{SOC}	I_{SS} = 400 nA, C_{SS}= 1 nF	165	200	235	
CS to DL Delay	T_D			150		ns
Leading Edge Blanking Period	T_{BL}	$DL_{(ON)}$ blanking time		20		
Pulse Width Modulator						
Maximum Duty Cycle[c]	D_{MAX}			47	50	%
Maximum Duty Cycle Asymmetry				1		
R_{DB} Voltage	V_{RDB}			3.18		V
Oscillator						
Oscillator Frequency[d]	F_{OSC}	R_{OSC} = 47 kΩ, C_{OSC} = 100 pF	680	800	920	kHz
Oscillator Bias Voltage	V_{ROSC}			3.24		V
Soft Start						
Soft Start Charging Current	I_{SS}	V_{SS} = 0 V	- 26	- 20	- 14	µA
SS Ramp Completion Voltage	V_{SS}			5.4		V
MOC Discharge Current	I_{DSS1}	CS = V_{MOC}	14	20	26	µA
SOC Discharge Current	I_{DSS2}	CS = V_{SOC}		400		nA
Reset Voltage	V_{SSL}	CS < V_{MOC}		0.25		V
Reference						
Output Voltage	V_{REF}	V_{CC} = 12 V	3.2	3.3	3.4	V
Short Circuit Current	I_{REFSC}	V_{REF} = 0 V	- 50	- 42		mA
Load Regulation	$\Delta V_R/\Delta I_R$	(0 mA ≤ I_{LOAD} ≤ 2.5 mA)	- 33	- 16		mV

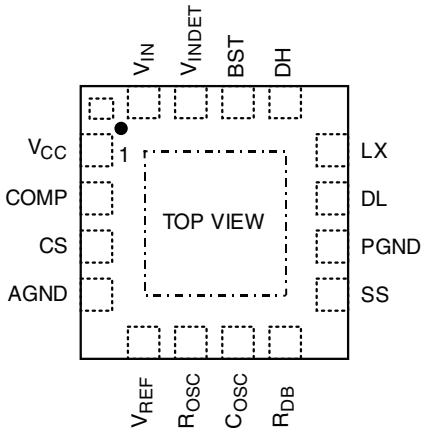
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified T_A = - 40 °C to 85 °C, F_{OSC} = 800 kHz, 10.5 V ≤ V_{CC} ≤ 13.2 V, V_{INDET} = 4.8 V, V_{IN} = 48 V, R_{DB} = 47.5 kΩ, R_{OSC} = 47.5 kΩ, C_{OSC} = 100 pF	Limits Min.	Typ.	Max.	Unit
V_{INDET} Function						
V_{Indet} Pin Input Impedance	R_{INDET}		30	46	70	kΩ
Shutdown Threshold High Voltage	V_{SDH}	V_{INDET} rising	0.33	0.58	0.76	V
Shutdown Hysteresis Voltage	H_{SD}			0.15		
Under Voltage OFF Voltage	V_{UVH}	V_{INDET} rising at I_{CC}	3.14	3.30	3.46	
Under Voltage Hysteresis Voltage	H_{UV}			0.26		
Over Temperature Protection (OTP)						
Activating Temperature	OTP_{ON}	T_J rising		160		°C
De-activating Temperature	OTP_{OFF}	T_J falling		145		
High-Side MOSFET Driver (DH Output)						
Output High Voltage (differential)	V_{DHH}	Sourcing 10 mA, V_{DH} - V_{BST}	- 0.3			V
Output Low Voltage (differential)	V_{DHL}	Sinking 10 mA, V_{DH} -V_{LX}			0.3	
Peak Output Sourcing Current	I_{DHH}	V_{CC} = 10.5 V, C_{LOAD} = 3 nF		- 2.2		A
Peak Output Sinking Current	I_{DHL}			1.6		
Driver Frequency	F_{DH}		340	400	460	kHz
Rise Time	t_{HR}	C_{LOAD} = 3 nF		20		ns
Fall Time	t_{HF}	C_{LOAD} = 3 nF		20		
Boost Pin Current (switching)	I_{BST}	V_{LX} = 75 V, V_{BST} = V_{LX} + V_{CC}	1.3	2.6	3.9	mA
LX Pin Current (switching)	I_{LX}		- 2.1	- 1.4	- 0.7	
LX Pin Leakage Current	I_{LX-LKG}	V_{INDET} = 0 V, V_{LX} = 40 V			10	µA
Low-Side MOSFET Driver (DL Output)						
Output High Voltage (differential)	V_{DLH}	Sourcing 10 mA, V_{DL} - V_{CC}	- 0.3			V
Output Low Voltage (differential)	V_{DLL}	Sinking 10 mA, V_{DL} - V_{AGND}			0.3	
Peak Output Sourcing Current	I_{DLH}	V_{CC} = 10.5 V, C_{LOAD} = 3 nF		- 1.6		A
Peak Output Sinking Current	I_{DLL}			1.6		
Driver Frequency	F_{DL}		340	400	460	kHz
Rise Time	t_{LR}	C_{LOAD} = 3 nF		20		ns
Fall Time	t_{LF}	C_{LOAD} = 3 nF		20		

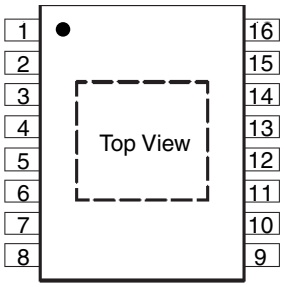
Notes:
a. MOC stands for moderate overcurrent voltage at CS pin.
b. SOC stands for severe overcurrent voltage at CS pin.
c. R_{DB} should be chosen for each application to provide adequate dead time. For production testing R_{DB} is chosen to test at 47 % target duty.
d. Not tested. Guaranteed by driver frequency test. The driver frequency is half of the oscillator frequency.

PACKAGE AND PIN CONFIGURATION

MLP44-16 PowerPAK Package



TSSOP-16 PowerPAK Package



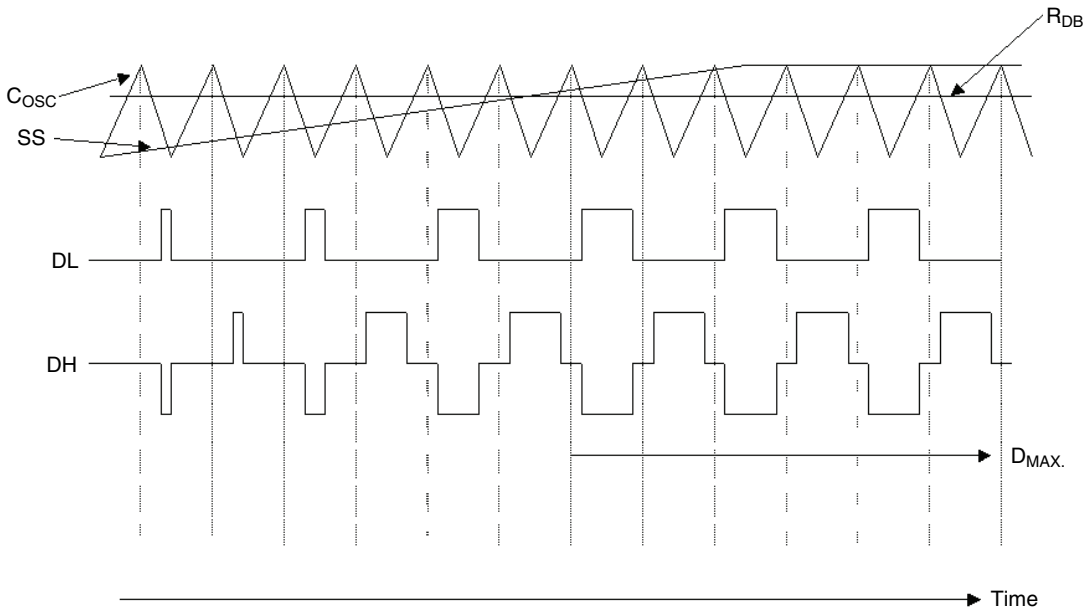
Notes:
For MLP44-16 package the bottom pin 1 indicator is connected to EPAD or AGND.

TSSOP-16	MLP44-16	Symbol	Description
3	1	V_{CC}	Pre-regulator output and supply voltage for internal circuitry
4	2	COMP	Pre-regulator compensation pin
5	3	CS	Current sense comparator input
6	4	AGND	Analog ground (connected to package's exposed pad)
7	5	V_{REF}	3.3 V reference output and bypass capacitor connection pin
8	6	R_{OSC}	Oscillator resistor connection
9	7	C_{OSC}	Oscillator capacitor connection and external frequency sync. connection
10	8	R_{DB}	Dead time setting resistor connection
11	9	SS	Soft start capacitor connection
12	10	PGND	Power ground
13	11	DL	Primary low-side MOSFET drive signal
14	12	LX	High-side MOSFET source and transformer connection node
15	13	DH	Primary high-side MOSFET drive signal
16	14	BST	Bootstrap voltage pin for the high-side driver
1	15	V_{INDET}	Shut down/under voltage/enable control pin
2	16	V_{IN}	High voltage pre-regulator input

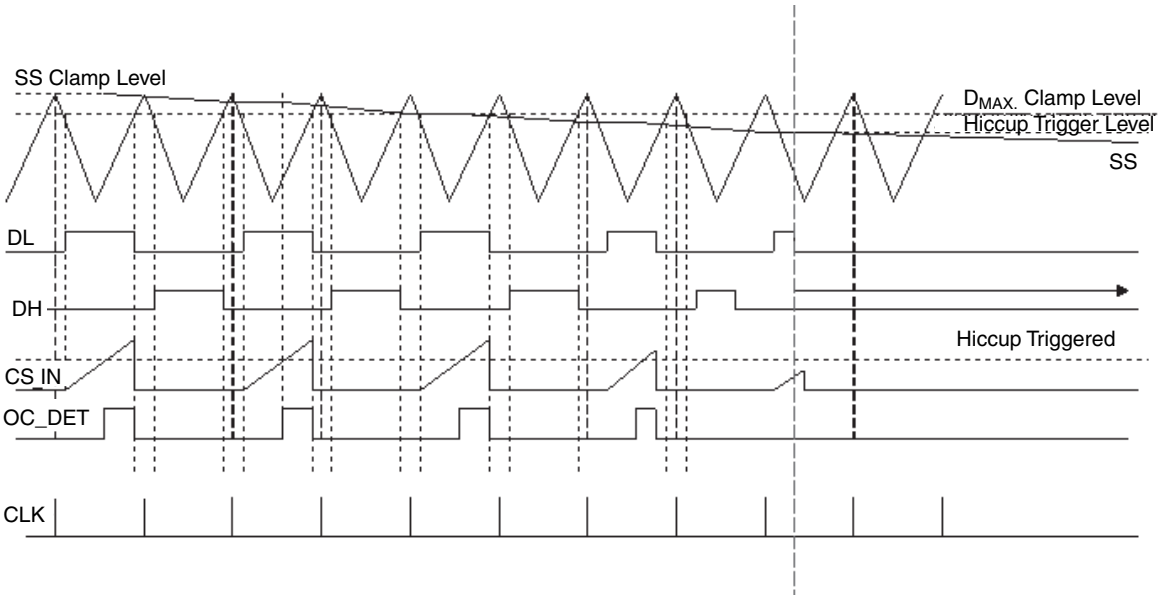
ORDERING INFORMATION

Part Number	Package	Marking	Temperature
SiP11206DQP-T1-E3	TSSOP-16	11206	- 40 °C to + 85 °C
SiP11206DLP-T1-E3	MLP44-16		

TIMING DIAGRAM AND SOFT START DUTY CYCLE CONTROL

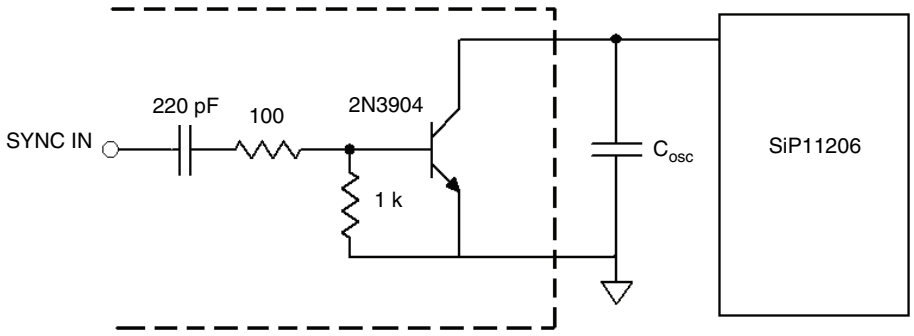


HICCUP RESPONSE TO MODERATE OVERCURRENT FAULTS



Over current protection operation showing reduction in duty cycle down to the hiccup trigger point. SS continues to discharge down to 250 mV (400 nA $I_{DISCHARGE}$), and then will recharge at 20 µA.

CIRCUIT FOR FREQUENCY SYNCHRONIZATION



DETAILED OPERATIONAL DESCRIPTION

Start Up

The controller supply (V_{CC}) is linearly regulated up to its target voltage V_{REG} by the on chip pre-regulator circuit. During power up with V_{INDET} ramping up from 0, the V_{CC} capacitor minimum charge current is 20 mA and the pre-regulator voltage is typically 9.3 V. As V_{INDET} exceeds V_{REF}, the DL/DH outputs are capable of driving 3 nF MOSFET gate capacitances and hence the pre-regulator load regulation can easily handle 120 µA to 20 mA load step with a typical load regulation of 1 %. Current into the external V_{CC} capacitor is limited to typically 20 mA by the internal pre-regulator unless an external power source is connected to V_{CC} pin. This source may be a DC supply or from V_{IN} by connecting a PNP pass transistor between V_{IN} and V_{CC}. The V_{CC} pin is protected by a 20 mA clamp when this pin exceeds 14.5 V. The clamp turns on when V_{CC} is between 14.5 V and 16 V. When V_{CC} exceeds the UVLO voltage ($UVLO_H$) a soft start cycle of the switch mode supply is initiated. The V_{CC} supply continues to be charged by the pre-regulator until V_{CC} equals V_{REG}. During this period, between $UVLO_H$ and V_{REG}, excessive load may result in V_{CC} falling below $UVLO_H$ and stopping switch mode operation. This situation is avoided by the hysteresis between V_{REG} and UVLO Off-Threshold level $UVLO_L$.

PWM Operation

During startup, DL always turns on before DH and both switch on and off at half the oscillator frequency. The driver duty cycle increases as SS voltage increases, since the SS comparator sets the ON pulse width by comparing the SS ramp voltage with the oscillator ramp voltage. When SS ramp reaches a voltage that equals to R_{DB} voltage, the PWM comparator, which compares R_{DB} voltage to the oscillator ramp, takes over and the maximum duty cycle is now set by the oscillator ramp and R_{DB} voltage. Mathematically, the total duty cycle is determined by the following formula:

$$D_{TOTAL} = R_{DB}/R_{OSC}$$

And the duty cycle on DL or DH will be approximately half of D_{TOTAL}. Please note that due to oscillator comparator overshoot the exact duty cycle calculated using above formula may be slightly different. The PWM operation during start up can be better understood by referring to "Timing diagram and soft start duty cycle control" graph. The soft start completion voltage at SS pin is clamped above the internal ramp waveform's upper turning point.

Soft Start

The soft start circuit plays an important role in protecting the controller. At startup it prevents high in-rush current. During a normal start-up sequence ($V_{CS} < V_{MOC}$. V_{CS} is the voltage at CS pin), or following any event that would cause a hiccup-and-soft-start sequence, C_{SS} will be charged from about 0 V to a final voltage of 4.8 V at a 20 µA rate. As the voltage on the C_{SS} rises towards the final voltage, the maximum permitted DL and DH duty cycles will increase from 0 % to a maximum defined by the R_{DB} resistor.

When a mild fault condition is detected ($V_{CS} = V_{MOC}$), C_{SS} goes into a hiccup mode until fault condition is removed. The hiccup is activated when C_{SS} discharges to 0.85 V_{SS} at 20 µA and subsequently at 0.4 µA until the fault condition is removed. Refer to "Fault Conditions and Responses" for details.

Fault Conditions and Responses

The faults that can cause a hiccup-and-retry cycle are moderate over-current (MOC), severe over-current (SOC), chip level UVLO, system level UVLO, and over temperature protection (OTP).

Prior to detailing the various fault conditions and responses, some definitions are given:

1. A complete switching period, T, consists of two oscillator cycles, T_{DL} and T_{DH}.
2. T_{DL} (T_{DH}) is the oscillator cycle during which the DL (DH) output is in the high state.
3. T is defined as starting at the beginning of T_{DL}, and terminating at the end of T_{DH}.

Response to MOC Faults ($V_{MOC} < V_{CS} < V_{SOC}$):

Once SiP11206 has completed a normal soft-start cycle, V_{SS} will be clamped at 4.5 V, allowing the maximum possible duty cycle on DL and DH.

If an MOC fault occurs following the start-up (due to a condition such as an excessive load on the converter's output), SiP11206 will respond by gradually reducing the available maximum duty cycle of its DL and DH outputs each to be equal to approximately 42 % of their possible 47 % maximum values. This is before any effects of deadtime introduced by R_{DB} are added in. This reduction in available maximum duty cycle is achieved by reducing the voltage on the SS pin to 4 V, as follows:

1. If $V_{MOC} < V_{CS} < V_{SOC}$ at any time during T_{DL}, a current of 20 µA will be drawn out of the SS pin until the beginning of the next T_{DL}.
2. If the voltage on the SS pin remains above the value that would allow an available maximum DL and DH duty cycle of 42 %, SiP11206 will continue operating.
3. If the voltage on the SS pin goes below the value that would allow an available maximum DL and DH duty cycle of 42 %, a hiccup interval is started, during which both DL and DH are held in their low states.
4. The SS pin is discharged towards 0 V by a 400 nA sink current.
5. The hiccup interval is terminated when the SS pin is discharged to 0.25 V.

After the above actions have been taken switching on the DL and DH outputs will then resume with a normal soft-start cycle.
Response to MOC faults is enabled after the successful completion of any normal soft-start cycle.

Response to SOC Faults ($V_{CS} > V_{SOC}$):

This is an immediate, single-cycle response over current shutdown, followed by a hiccup delay and a normal soft-start cycle. Since this is a gross fault protection mechanism, its triggering mechanism is asynchronous to the timing of T_{DL} and T_{DH}.

1. If $V_{CS} > V_{SOC}$, a hiccup interval is started, during which both DL and DH are held in their low states.
2. The SS pin is discharged towards 0 V by a 400 nA sink current.
3. The hiccup interval is terminated when the SS pin is discharged to 0.25 V.
4. Switching on the DL and DH outputs will then resume with a normal soft-start cycle.

Severe over current response is enabled at all times, including the initial ramp-up period of the soft-start pin. This allows SiP11206 to provide rapid fault protection for the converter's power train.

Immediate Response to UVLO Faults:
The under voltage protection conditions at converter-level (V_{INDET} pin UVLO) and chip-level (V_{CC} UVLO) will immediately trigger a shutdown-and-retry SS response, with the restart requirements being that:

1. The SS pin has been discharged at a 20 µA rate to the 0.25 V level.
2. The affected supply has recovered to its turn-on threshold.

Once these conditions are met, switching will resume with a normal soft-start cycle. Response to UVLO faults is enabled at all times, including the initial ramp-up period of the soft-start pin.

Immediate Response to an OTP Condition:
Failure of the application circuit to provide an external voltage to the V_{CC} pin above the V_{REG} level may result in an OTP condition ($T_J > OTP_{ON}$). Other conditions, such as excessive ambient temperature or, where applicable, failure of airflow over the DC-DC converter circuit, can also trigger an OTP condition. An OTP condition will immediately trigger a shutdown-and-retry soft start response, with the restart requirements being that:

1. The SS pin has been discharged at a 20 µA rate to the 0.25 V level.
2. The chip junction temperature has fallen below the lower OTP threshold.

Once these conditions are met, switching will resume with a normal soft-start cycle. Response to the OTP condition is enabled at all times, including the initial ramp-up period of the soft-start pin.

Reference

The reference voltage of SiP11206 is set at 3.3 V at V_{REF} pin. This pin should be decoupled externally with a 0.1 µF to 1 µF capacitor to GND. Up to 5 mA may be drawn internally from this reference to power external circuits. Note that if the V_{INDET} pin is pulled below 0.55 V (typical), the reference will be turned off, and SiP11206 will enter a low-power "standby" mode. During startup or when V_{REF} is accidentally shorted to ground, this pin has internal short circuit protection limiting the source current to 50 mA. V_{REF} load regulation for 5 mA step is typically 0.45 %.

Oscillator

The oscillator is designed to operate from 200 kHz to 1 MHz with temperature stability within 15 %. This operating frequency range allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator frequency, and therefore the switching frequency, is programmable by the value of resistor and capacitor connected to the R_{OSC} and C_{OSC} pins respectively. Note that the switching frequency at pins DL and DH is half of the oscillator frequency, i.e., the DL output will be active during one oscillator cycle, and the DH during the next oscillator cycle.

V_{INDET}

The V_{INDET} pin controls several modes of operation and the modes of operation are controlled by shutdown (V_{SD}) and under voltage (V_{UV}) comparators (see block diagram). When the IC is powered solely by V_{IN} and V_{INDET} is less than V_{SDH}

due to some external reset condition the pre-regulator is in low power standby mode and the internal bias network is powered down. When V_{INDET} is greater than V_{SDH} but less than V_{REF} and V_{CC} is forced to 12 V the pre-regulator shuts off drawing only leakage current from V_{IN} and quiescent current from V_{CC}. In this mode the controller output drivers remains static (non-switching). When V_{INDET} is above V_{REF} the controller is enabled and both drivers are switching at half the oscillator frequency. If SiP11206 is shut down via this pin, its restart will be by means of a soft-start cycle, as described under "Soft Start" and "Hiccup-Mode Operation" above.

The input impedance to ground of this pin is typically 46K ± 30 % and must be taken into account at application design. An external 10:1 resistor divider ratio of supply voltage to V_{INDET} pin is required in a typical application.

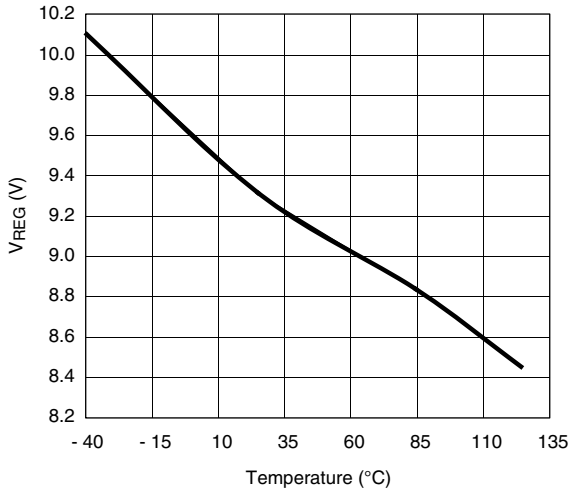
Primary High and Low Side MOSFET Drivers

The low-side MOSFET driver is powered directly from V_{CC} of the chip. The high-side MOSFET however requires the gate voltage to be higher than V_{IN}. This is achieved with a charge pump capacitor C_{BST} between BST and LX, and an external diode to charge and bootstrap the initial charge up voltage across C_{BST} to V_{CC} level. On the alternate oscillator cycle the boost diode isolates BST from V_{IN} and hence BST and LX steps up to V_{IN} + V_{CC} and V_{IN}, respectively. This sequencing insures that DL will always turn on before DH during start-up. The boost capacitor value must be chosen to meet the application droop rate requirement.

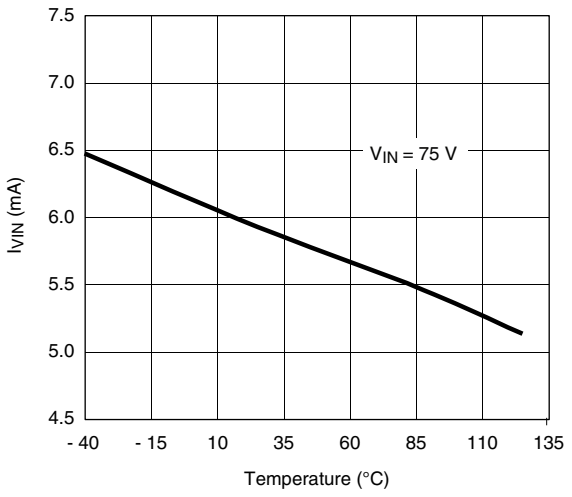
External Frequency Synchronization

The oscillator frequency of this IC can be synchronized to an external source with a simple circuit shown in "Circuit for Frequency Synchronization" diagram. The synchronized frequency should not exceed 1.4 times the set frequency, and the synchronized frequency range should not exceed the IC frequency range.

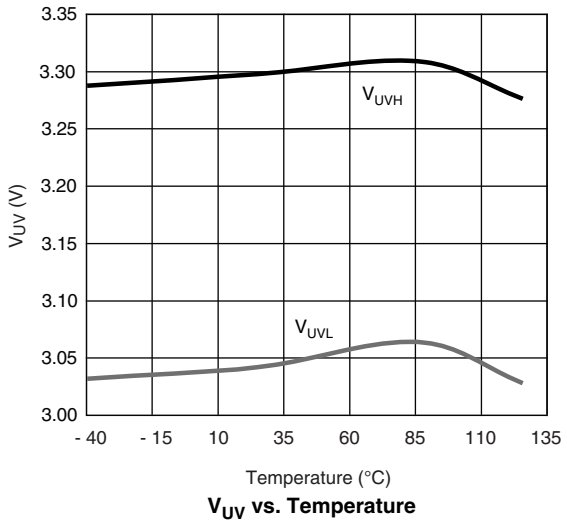
TYPICAL CHARACTERISTICS



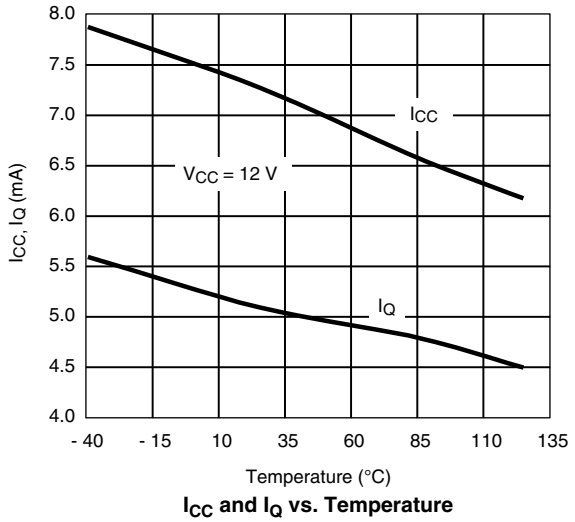
V_{REG} vs. Temperature



I_{VIN} vs. Temperature

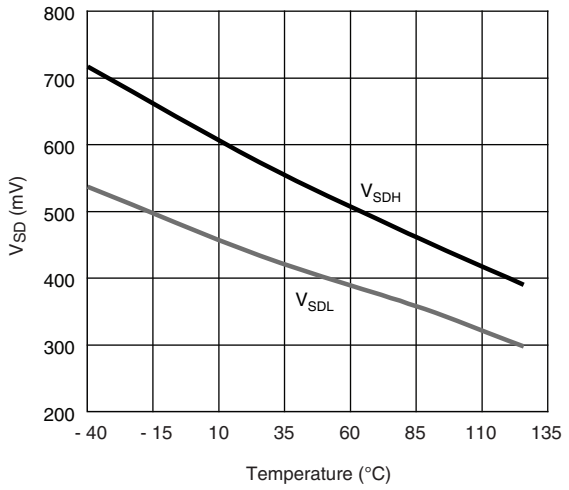


V_{UV} vs. Temperature

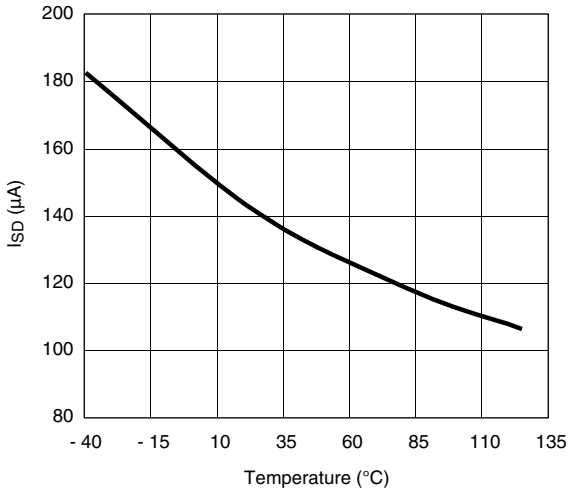


I_{CC} and I_Q vs. Temperature

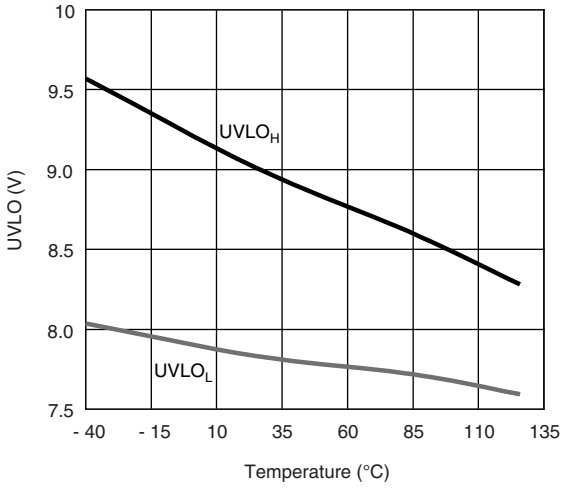
TYPICAL CHARACTERISTICS



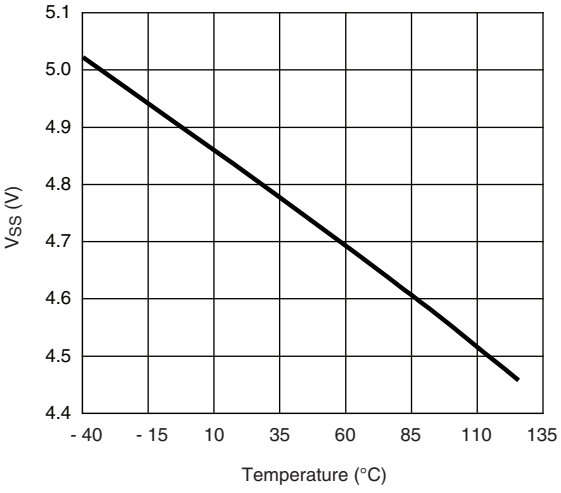
V_{SD} vs. Temperature



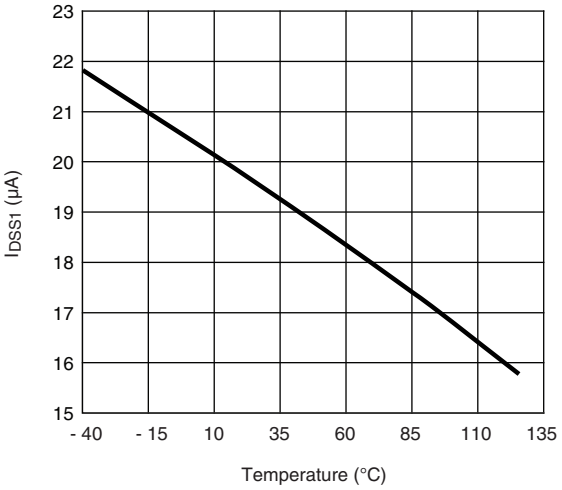
I_{SD} vs. Temperature



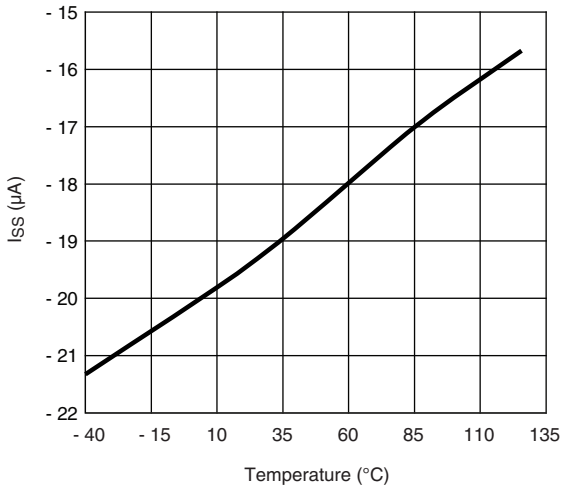
UVLO vs. Temperature



V_{SS} vs. Temperature

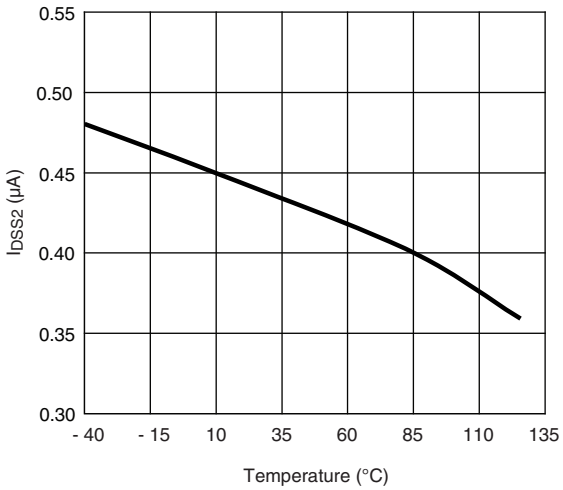


I_{DSS1} vs. Temperature

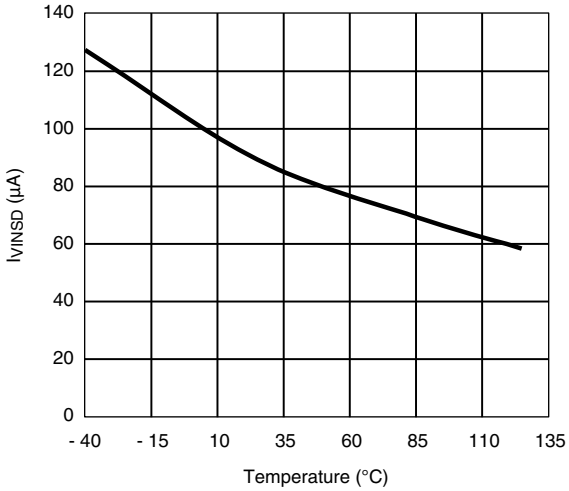


I_{SS} vs. Temperature

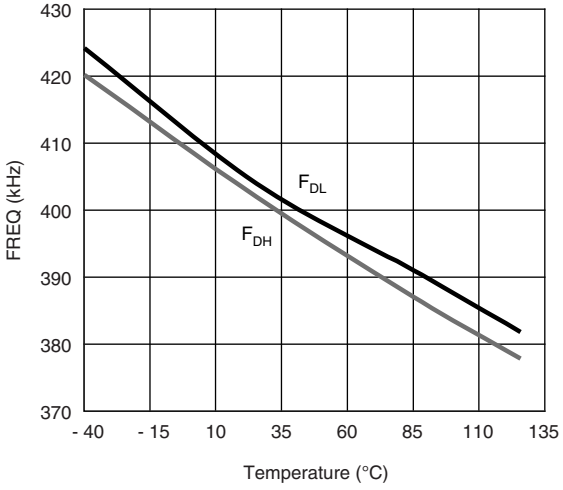
TYPICAL CHARACTERISTICS



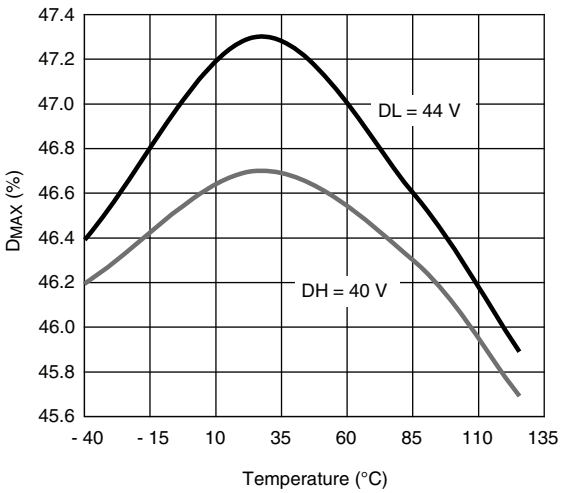
I_{DSS2} vs. Temperature



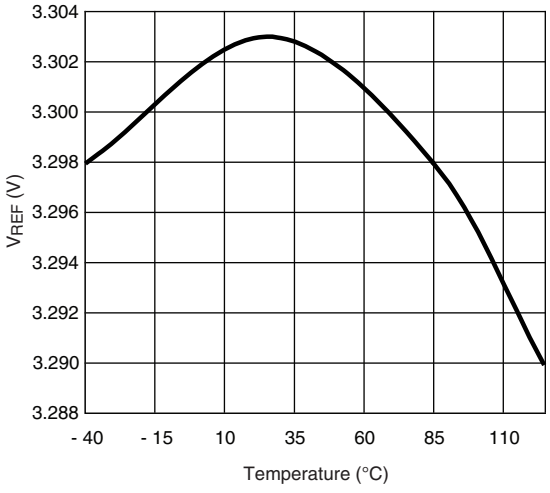
I_{VINSD} vs. Temperature



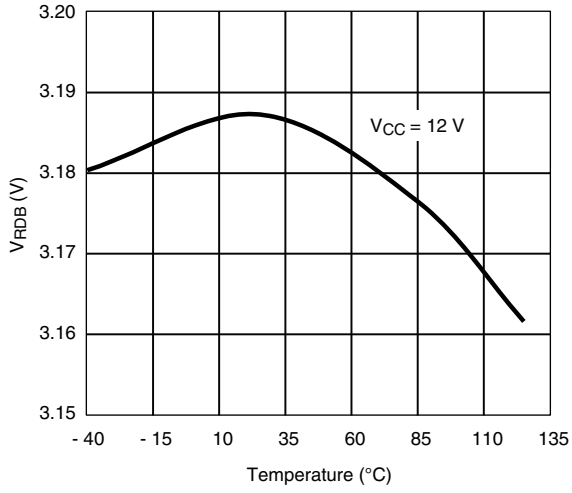
F_{DL}/F_{DH} vs. Temperature



$D_{MAX.}$ vs. Temperature

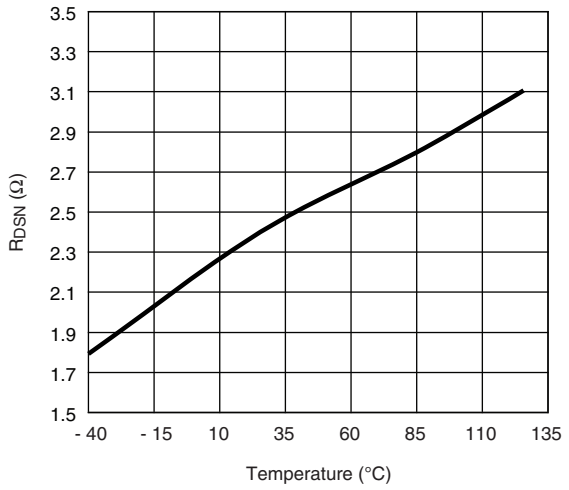


V_{REF} vs. Temperature

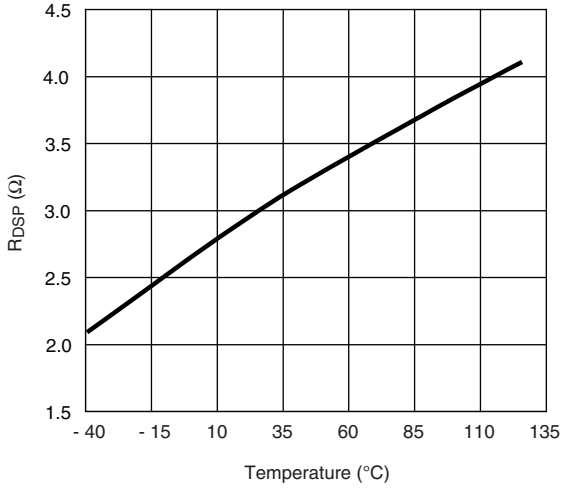


V_{RDB} vs. Temperature

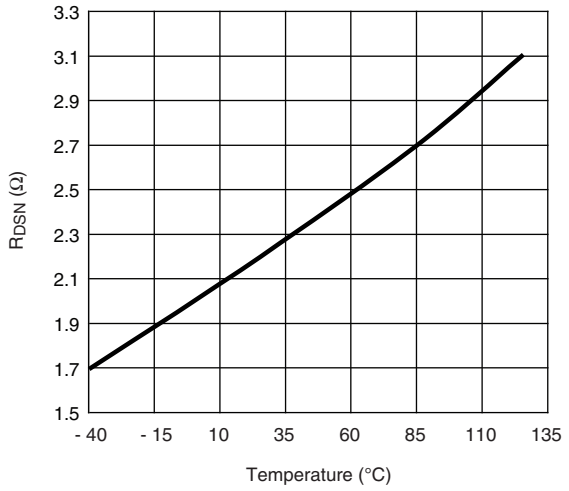
TYPICAL CHARACTERISTICS



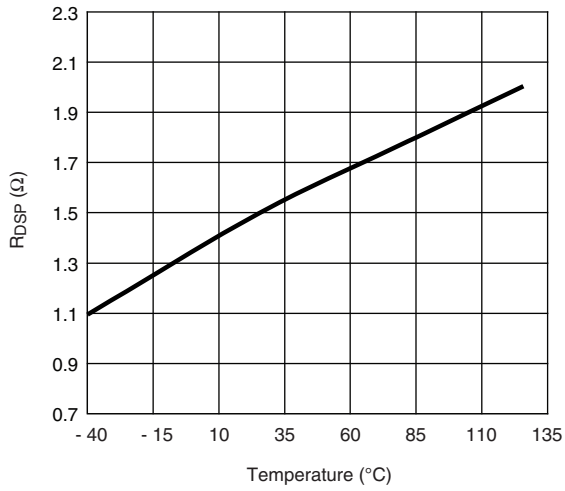
DL R_{DSN} vs. Temperature



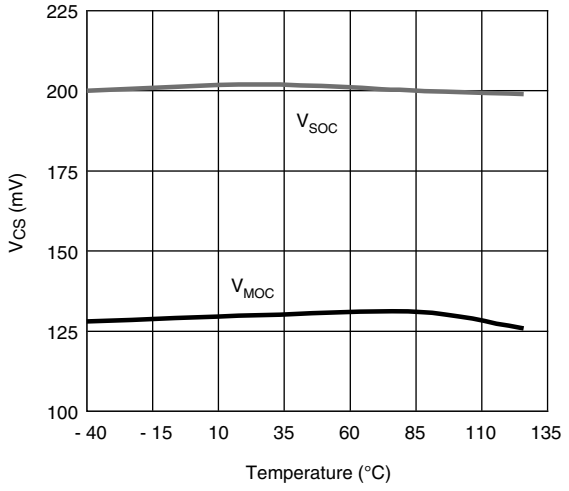
DL R_{DSP} vs. Temperature



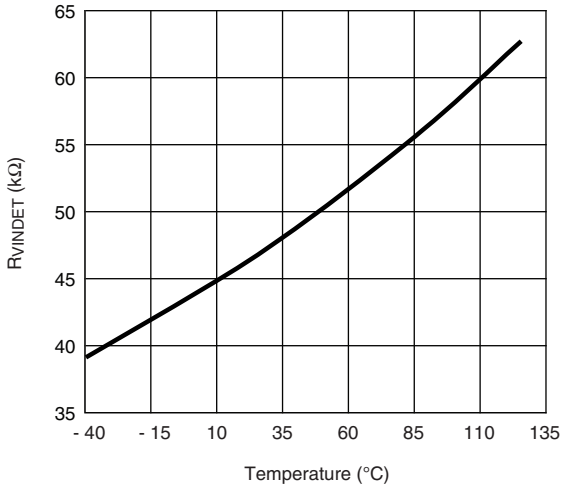
DH R_{DSN} vs. Temperature



DH R_{DSP} vs. Temperature

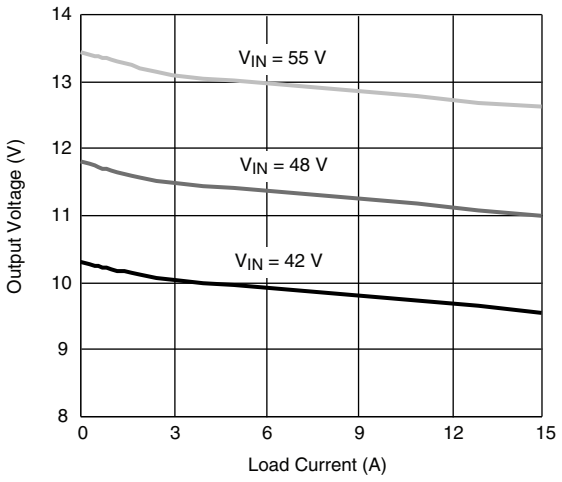


V_{CS} vs. Temperature

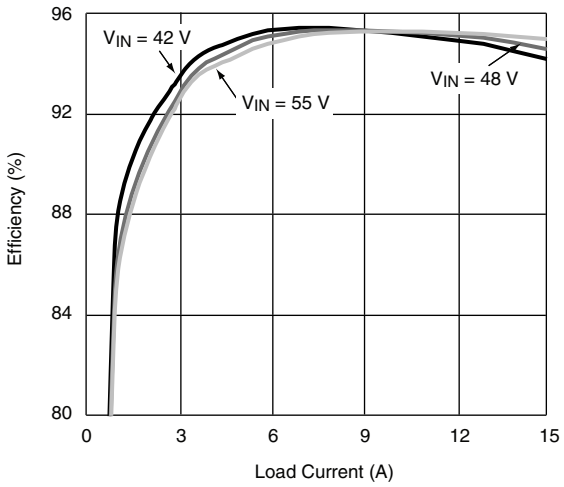


R_{VINDET} vs. Temperature

TYPICAL CHARACTERISTICS

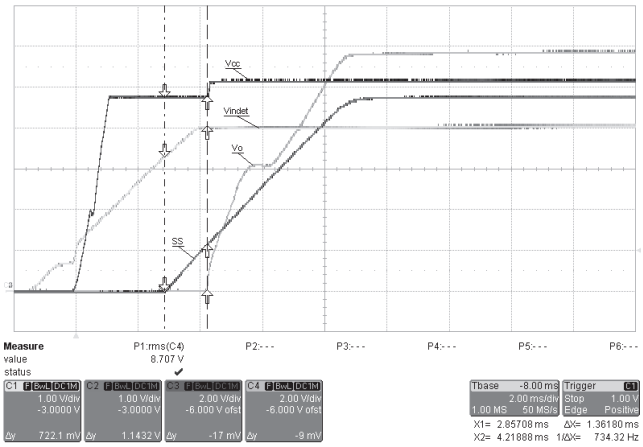


Line and Load Regulation

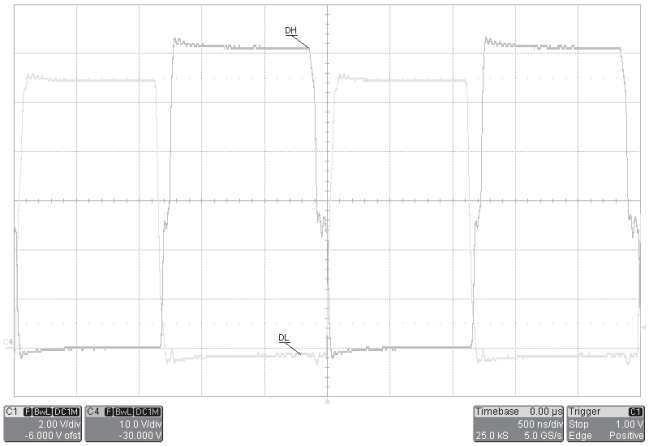


Efficiency vs. Current

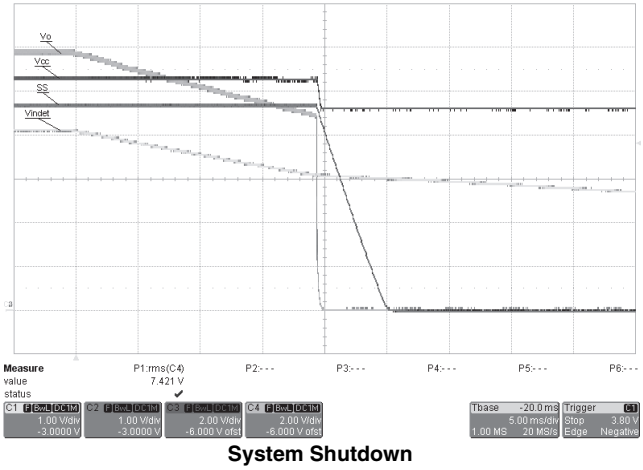
TYPICAL WAVEFORMS



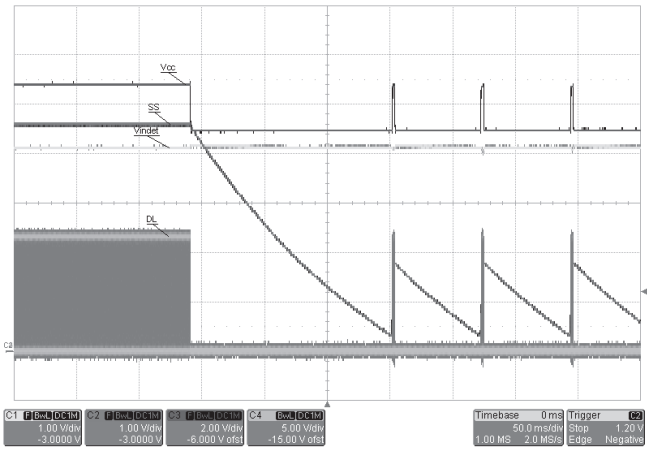
System Startup



Primary Driving Signals DL and DH



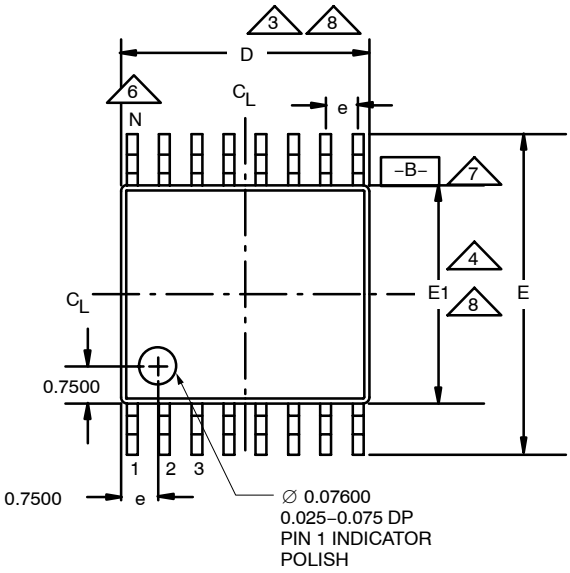
System Shutdown



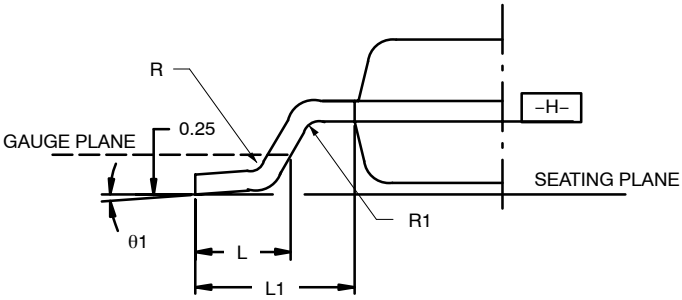
Hiccup Mode when Output Shorted

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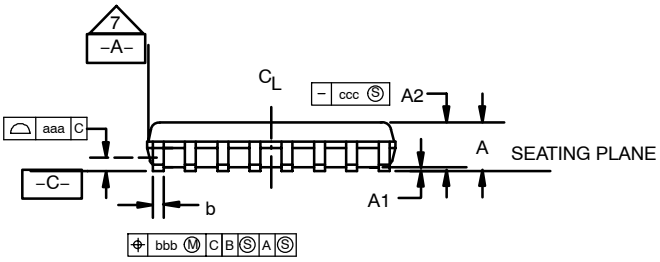
POWER IC THERMALLY ENHANCED PowerPAK® TSSOP: 14/16-LEAD

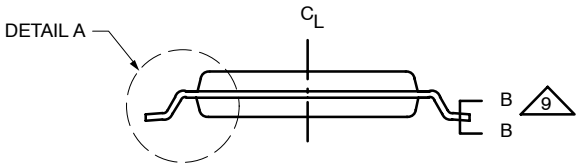


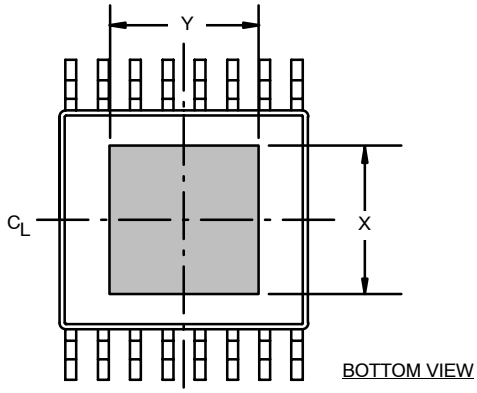
TOP VIEW



DETAIL A

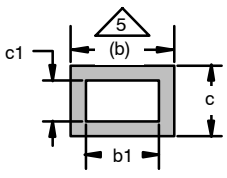






BOTTOM VIEW

EXPOSED PAD



DETAIL B-B

POWER IC THERMALLY ENHANCED PowerPAK® TSSOP: 14/16-LEAD

Dim	MILLIMETERS			INCHES*		
	Min	Nom	Max	Min	Nom	Max
A	–	–	1.20	–	–	0.0472
A_1	0.025	–	0.100	0.001	–	0.0039
A_2	0.80	0.90	1.05	0.0315	0.0354	0.0413
b	0.19	–	0.30	0.0075	–	0.0118
b1	0.19	0.22	0.25	0.0075	0.0087	0.0098
c	0.09	–	0.20	0.0035	–	0.0079
c1	0.09	–	0.16	0.0035	–	0.0063
D	4.9	5.0	5.1	0.1929	0.1968	0.2008
e		0.65 BSC			0.0256 BSC	
E	6.2	6.4	6.6	0.2441	0.2520	0.2598
E_1	4.3	4.4	4.5	0.1693	0.1732	0.1772
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.0 REF			0.0394 REF	
R	0.09	–	–	0.0035	–	–
R1	0.09	–	–	0.0035	–	–
θ1	0	–	0	0	–	0
N (14)		14			14	
N (16)		16			16	
X	2.95	3.0	3.05	0.116	0.118	0.120
Y (14)	3.15	3.2	3.25	0.124	0.126	0.128
Y (16)	2.95	3.0	3.05	0.116	0.118	0.120
aaa		0.10			0.0039	
bbb		0.10			0.0039	
ccc		0.05			0.0020	
ddd		0.20			0.0079	

ECN: S-50568—Rev. B, 04-Apr-05
DWG: 5913

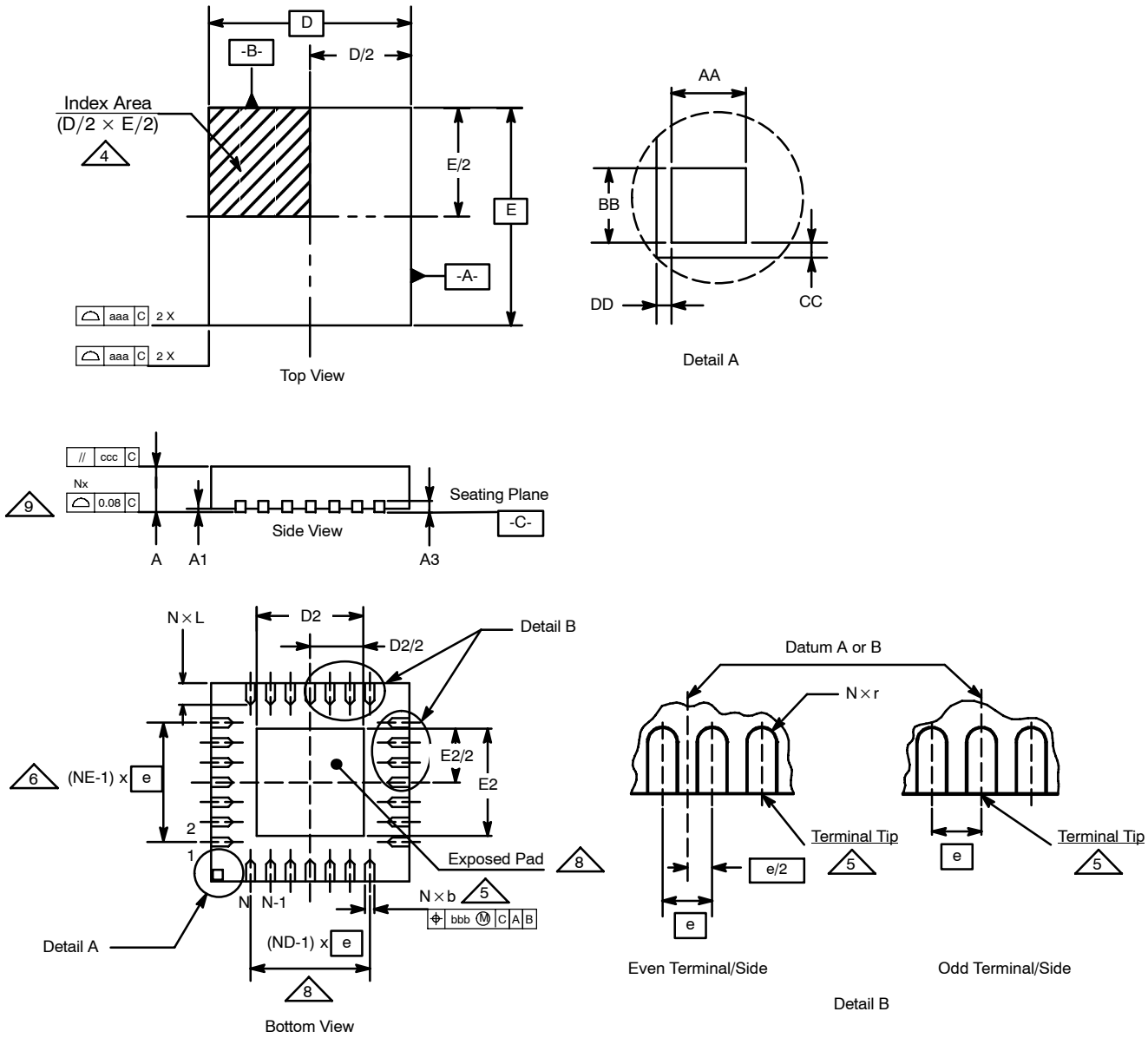
*Dimensions are in mm converted to inches.

NOTES:

1. All dimensions are in millimeters (angles in degrees).
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs.
4. Dimension “E1” does not include internal flash or protrusion.
5. Dimension “b” does not include Dambar protrusion.
6. “N” is the maximum number of lead terminal positions for the specified package length.
7. Datums -A- and -B- to be determined at datum plane -H- .
8. Dimensions “D” and “E1” are to be determined at datum plane -H- .
9. Cross section B-B to be determined at 0.10 to 0.25 mm from the lead tip.
10. Refer to JEDEC MO-153, Issue C., Variation ABT.
11. Exposed pad will depend on the pad size of the L/F.

PowerPAK® MLP44-16 (POWER IC ONLY)

JEDEC Part Number: MO-220



PowerPAK® MLP44-16 (Power IC Only)

JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	–	0.20 Ref	–	–	0.0079	–	
AA	–	0.345	–	–	0.0136	–	
aaa	–	0.15	–	–	0.0059	–	
BB	–	0.345	–	–	0.0136	–	
b	0.25	0.30	0.35	0.0098	0.0118	0.138	5
bbb	–	0.10	–	–	0.0039	–	
CC	–	0.18	–	–	0.0071	–	
ccc	–	0.10	–	–	0.0039	–	
D		4.00 BSC			0.1575 BSC		
D2	2.55	2.7	2.8	0.1004	0.1063	0.1102	
DD	–	0.18	–	–	0.0071	–	
E		4.00 BSC			0.1575 BSC		
E2	2.55	2.7	2.8	0.1004	0.1063	0.1102	
e		0.65 BSC			0.0256 BSC		
L	0.3	0.4	0.5	0.0118	0.0157	0.0197	
N		16			16		3, 7
ND	–	4	–	–	4	–	6
NE	–	4	–	–	4	–	6
r	b(min)/2	–	–	b(min)/2	–	–	

* Use millimeters as the primary measurement.

ECN: S-50794—Rev. B, 16-May-05
DWG: 5905

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

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