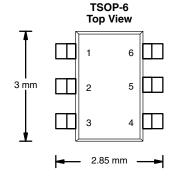




P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
- 20	0.0240 at $V_{GS} = -4.5 \text{ V}$	- 8 ^a	21 nC			
	0.0372 at V _{GS} = - 2.5 V	- 8 ^a	21110			



Ordering Information:

Si3407DV-T1-E3 (Lead (Pb)-free) Si3407DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

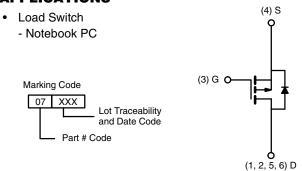
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- PWM Optimized
- 100 % R_q Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free Pb-free



APPLICATIONS



P-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	- 20 ± 12			
Gate-Source Voltage				V_{GS}	
	T _C = 25 °C		- 8 ^a		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C	I_	- 8 ^a		
Continuous Diain Current (1) = 130 G)	T _A = 25 °C	I _D	- 7.5 ^{b, c}		
	T _A = 70 °C		- 6 ^{b, c}	Α .	
Pulsed Drain Current		I _{DM}	- 25	^	
Continuous Source-Drain Diode Current	T _C = 25 °C	1	- 3.5		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 1.7 ^{b, c}		
Avalanche Current	L = 0.1 mH	I _{AS}	- 8		
Single Pulse Avalanche Energy	L = 0.111111	E _{AS}	3.2	mJ	
	T _C = 25 °C		4.2		
Maximum Power Dissipation	T _C = 70 °C		2.7	w	
Maximum Fower Dissipation	T _A = 25 °C	P _D	2 ^{b, c}	VV	
	T _A = 70 °C		1.3 ^{b, c}		
Operating Junction and Storage Temperature	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS								
Parameter	Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 s	R _{thJA}	45	62.5	°C/W			
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	30	7 0,00			

Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. Maximum under steady state conditions is 110 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static				, ,, <u> </u>		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			-18.7		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		3.7		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = -250 \mu A$	- 0.65		- 1.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
		V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 25			Α
	, ,	V _{GS} = - 4.5 V, I _D = - 7.5 A		0.0200	0.0240	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 6.4 A		0.0310	0.0327	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 7.5 A		25		S
Dynamic ^b						
Input Capacitance	C _{iss}			1670		
Output Capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		335		рF
Reverse Transfer Capacitance	C _{rss}			284		
	Q _g	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -7.5 \text{ A}$		42	63	nC
Total Gate Charge				21	32	
Gate-Source Charge	Q _{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -7.5 \text{ A}$		6		
Gate-Drain Charge	Q _{gd}			5		
Gate Resistance	R _g	f = 1 MHz	1.3	6.5	13	Ω
Turn-on Delay Time	t _{d(on)}			8	16	
Rise Time	t _r	V_{DD} = - 10 V, R_L = 1.7 Ω		11	17	ns
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -6 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		65	98	
Fall Time	t _f			39	59	
Turn-on Delay Time	t _{d(on)}			32	48	
Rise Time	t _r	V_{DD} = - 10 V, R_L = 1.7 Ω		62	93	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 6 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		53	80	
Fall Time	t _f			38	57	
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 3.5	
Pulse Diode Forward Current ^a	I _{SM}				- 25	Α
Body Diode Voltage	V_{SD}	I _S = - 6 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}			37	56	ns
Body Diode Reverse Recovery Charge	Q _{rr}	L CA 41/4t 100 A/v. T 05 00		22	33	nC
Reverse Recovery Fall Time	t _a	$I_F = 6 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		12		
Reverse Recovery Rise Time	t _b			25		- ns

Notes:

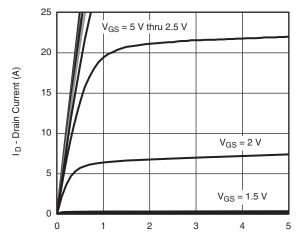
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.

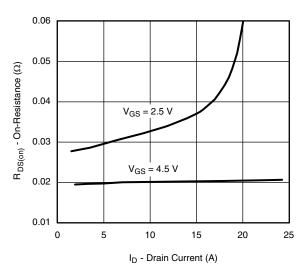


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

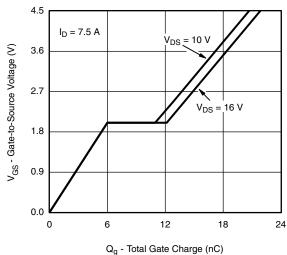


V_{DS} - Drain-to-Source Voltage (V)

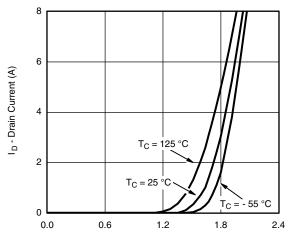
Output Characteristics



On-Resistance vs. Drain Current and Gate Voltage

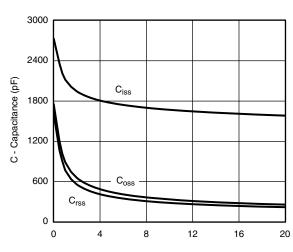


Gate Charge



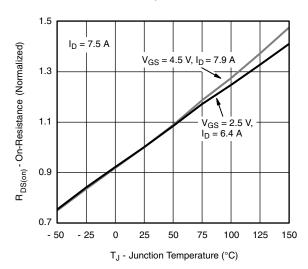
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



V_{DS} - Drain-to-Source Voltage (V)

Capacitance

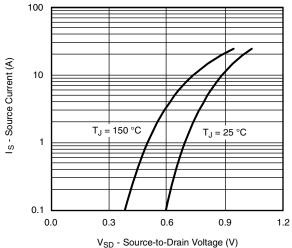


On-Resistance vs. Junction Temperature

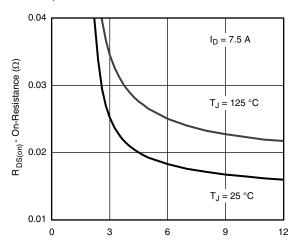
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

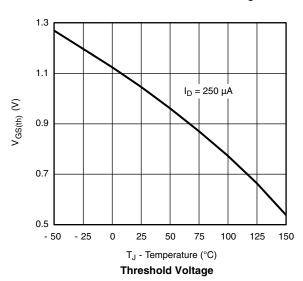


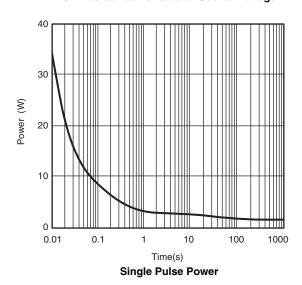
Source-Drain Diode Forward Voltage

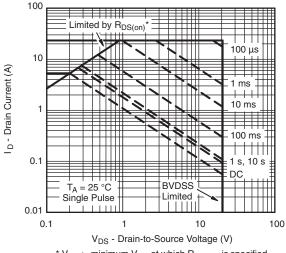


V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage





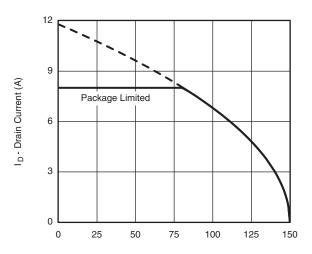


 * V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified **Safe Operating Area, Junction-to-Ambient**



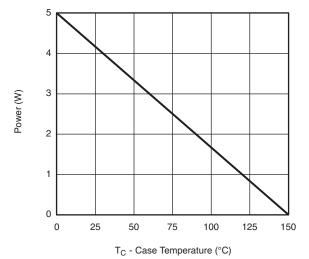


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

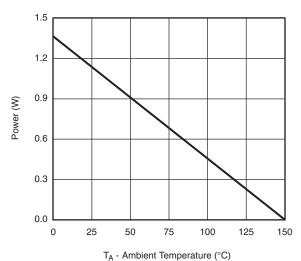


T_C - Case Temperature (°C)

Current Derating*



Power Derating, Junction-to-Foot



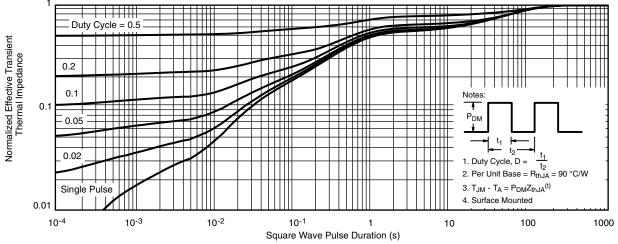
Power Derating, Junction-to-Ambient

 $^{^*}$ The power dissipation P_D is based on $T_{J(max.)}$ = 150 $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package

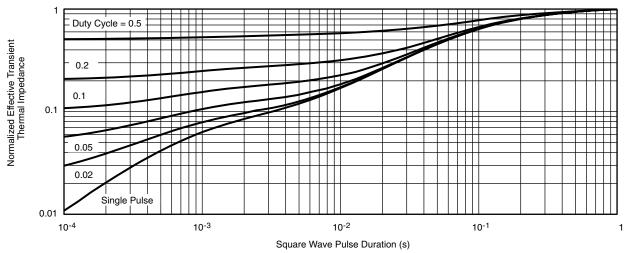
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

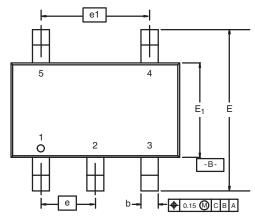
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?69987.

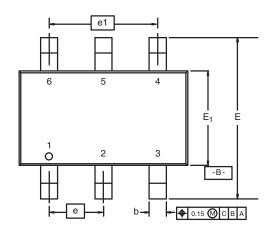




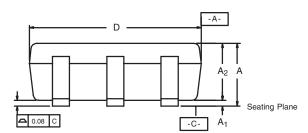
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C

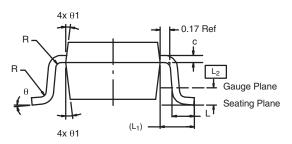




5-LEAD TSOP





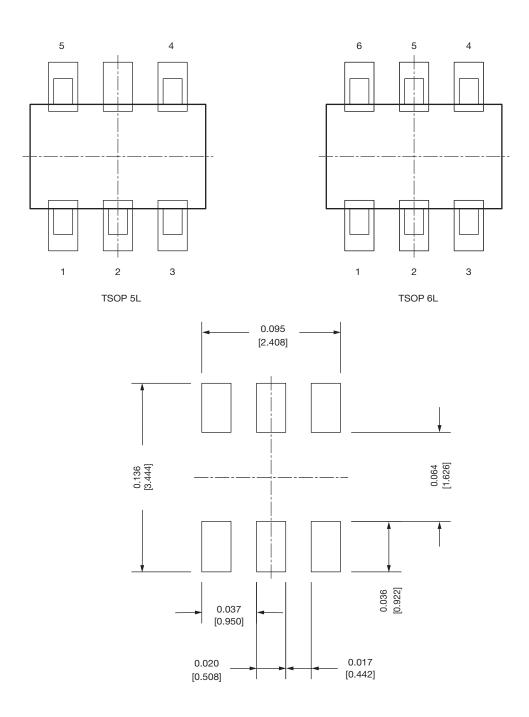


	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116 0.120		0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е		0.95 BSC		0.0374 BSC			
e ₁	1.80 1.90 2.00			0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L ₁	0.60 Ref			0.024 Ref			
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

Document Number: 71200 18-Dec-06



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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