Battery Disconnect Switch

FEATURES

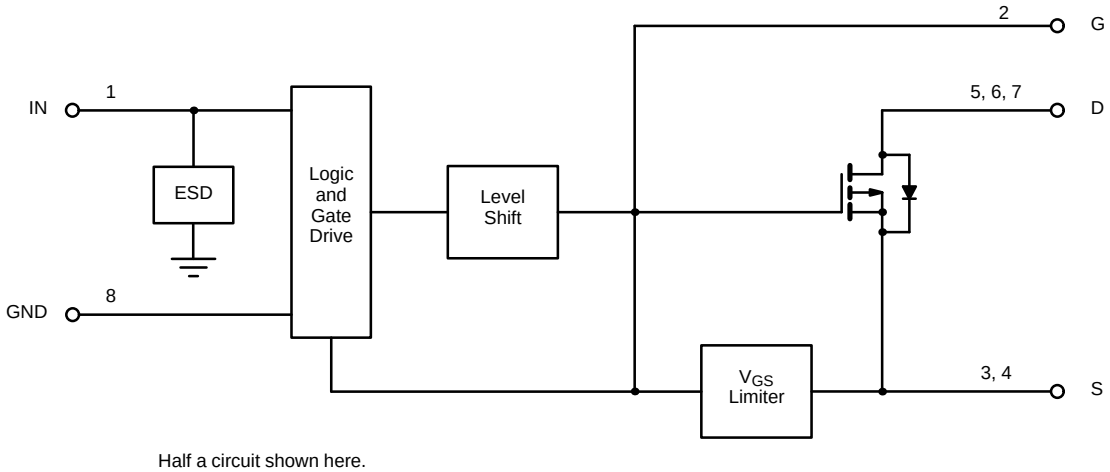
- Solution for Bi-Directional Blocking Bi-Directional Conduction Switch
- 6- to 30-V Operation
- Ground Referenced Logic Level Inputs
- Integrated Low $r_{DS(on)}$ MOSFET
- Level-Shifted Gate Drive with Internal MOSFET
- Ultra Low Power Consumption in Off State (Leakage Current Only)
- Logic Supply Voltage is Not Required

DESCRIPTION

The Si4710CY is a level-shifted p-channel MOSFET. Operating two in a series, these MOSFETs can be used as a reverse blocking switch for battery disconnect applications. It is a solution for multiple battery technology designs or designs that require isolation from the power bus during charging.

The Si4710CY is available in a 8-pin SOIC package and is rated for the commercial temperature range of –25 to 85°C.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Half a circuit shown here.

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND
V_S, V_D[a] ..... –0.3 V to 30 V
V_{SD} ..... –0.3 V to 30 V
V_{IN1}, V_{IN2} ..... –0.3 V to 15 V
V_{GS} ..... 20 V
Storage Temperature ..... –55 to 150°C
Power Dissipation[b] (t = 10 sec) ..... 2.3 W
(t = steady state) ..... 1.4 W

Thermal Resistance
Max Junction-Ambient[b] (t = 10 sec) ..... 55 C/W
(t = steady state) ..... 90 C/W
Max Junction-Foot (t = steady state) ..... 27 C/W

Notes
a. $V_{SD} \leq 30\ V_{DC}$
b. Device mounted with all leads soldered to 1" x 1" FR4 with laminated copper PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

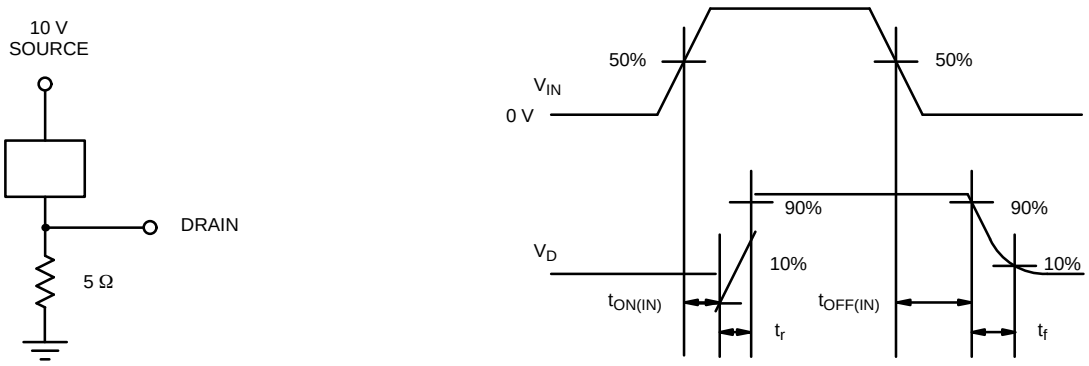
V_S, V_D ..... 6 V to 30 V
V_{IN1}, V_{IN2} ..... 0 V to 13.2 V
I_{DS} ..... 0 A to 6 A
Operating Temperature Range ..... –25 to 85°C
Junction Temperature ..... –25 to 150°C

SPECIFICATIONS

Parameter		Symbol	Specific Test Conditions	Limits Temp[a]	Min[b]	Typ[c]	Max[b]	Unit
On-Resistance		r_{DS}	V_S = 10 V, I_D = 1 A, V_{IN} = H	Room		0.014	0.018	Ω
Leakage Current		$I_{DS(off)}$	V_{DS} = 10 V	Room			1	µA
Power Consumption		I_S $GND_{(off)}$	V_S = 17 V	Room			1	µA
		I_S $GND_{(on)}$		Room		1.1	6	µA
Input Voltage Low		V_{INL}	V_S = 10 V	Full			0.8	V
Input Voltage High		V_{INH}		Full	2.5			V
Input Leakage Current		I_{INH}	V_{IN} = 5.0 V	Full			5	µA
Turn-On Delay	IN to D or S	$t_{ON(IN)}$	V_S = 10 V, R_L = 5 Ω, Test Circuit 1	Room		3.0	6	µs
Turn-Off Delay	IN to D or S	$t_{OFF(IN)}$		Room		1.5	3	µs
Rise Time		t_{RISE}		Room		1.25	3	µs
Fall Time		t_{FALL}		Room		50	150	ns
Voltage Across Pin 6 and 7		V_{GS}	V_S = 30 V	Room		10.2	18	V
Forward Diode		V_{SD}	I_D = –1 A	Room			1.1	V

Notes
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

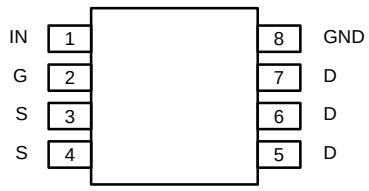
TIMING DIAGRAMS



TEST CIRCUIT 1

PIN CONFIGURATION

SO-8



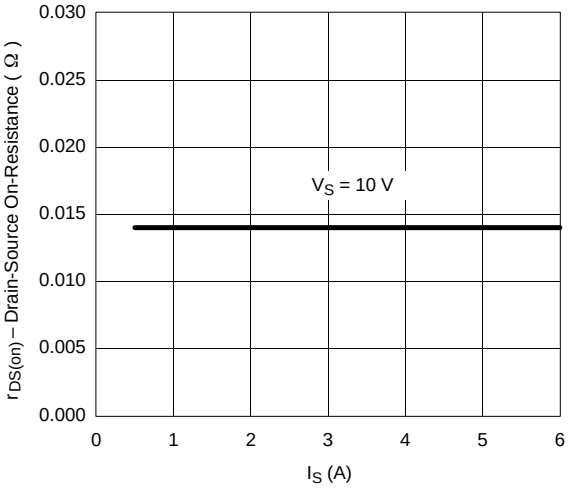
Order Number: Si4710CY

TRUTH TABLE	
V_{IN}	Switch
0	Off
0	Off
1	On
1	On

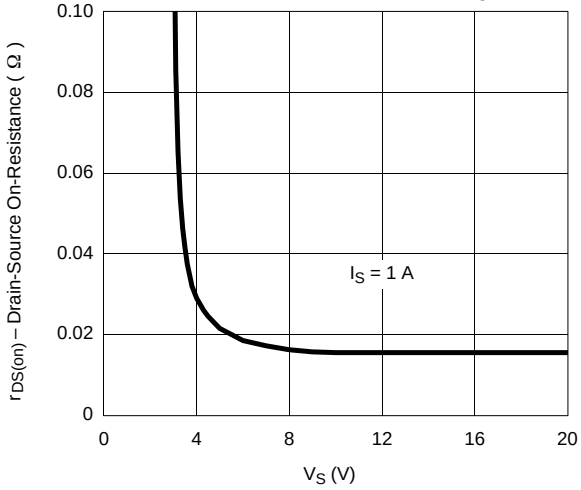
PIN DESCRIPTION		
Pin Number	Symbol	Description
5, 6	D	Drain connection for MOSFET.
8	GND	Ground
1	IN	Logic input, IN. High level turns on the switch.
2	G	Gate output to MOSFET.
3, 4	S	Source connection for MOSFET.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

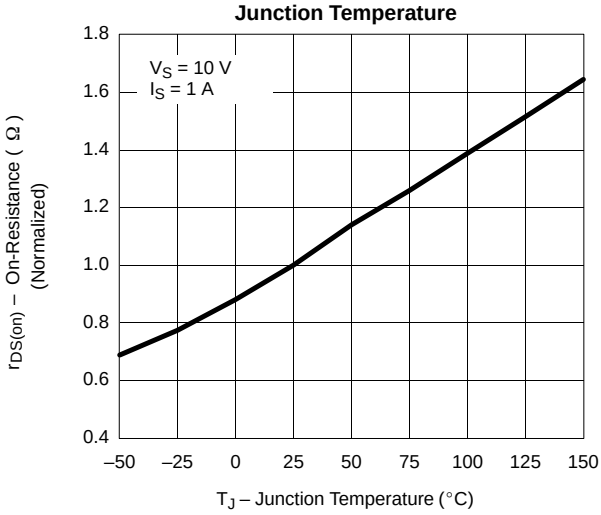
On-Resistance vs. Drain Current



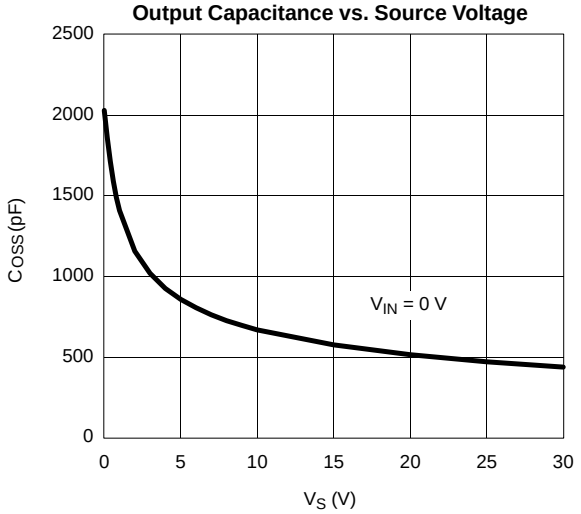
On-Resistance vs. Source Voltage



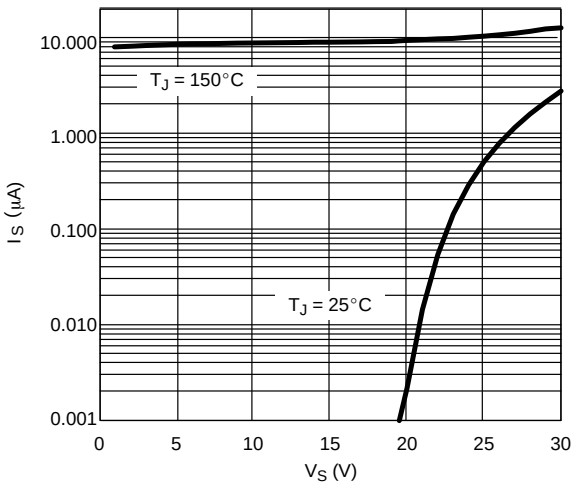
Normalized On-Resistance vs. Junction Temperature



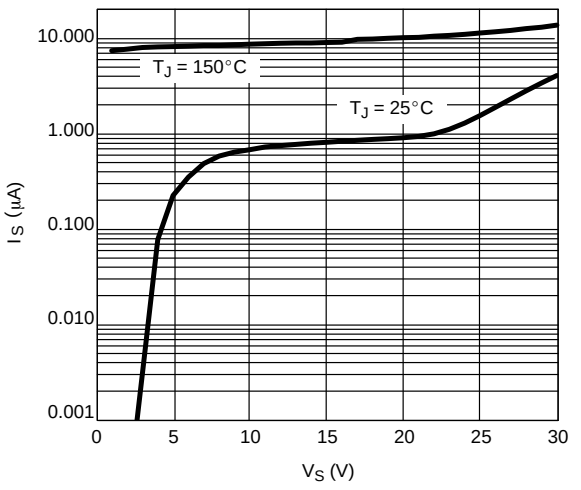
Output Capacitance vs. Source Voltage



Off-Supply Current vs. Source Voltage

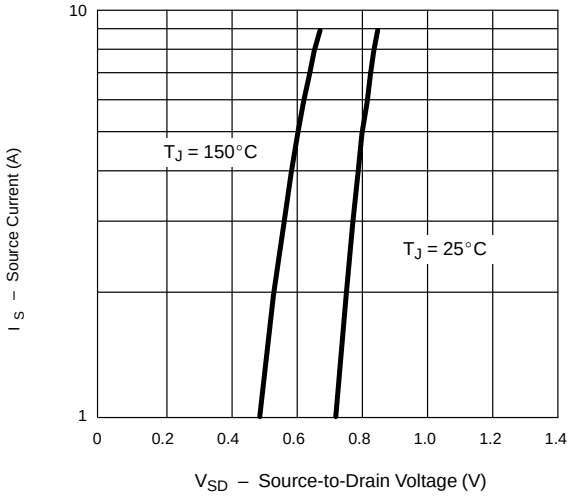


On-Supply Current vs. Source Voltage

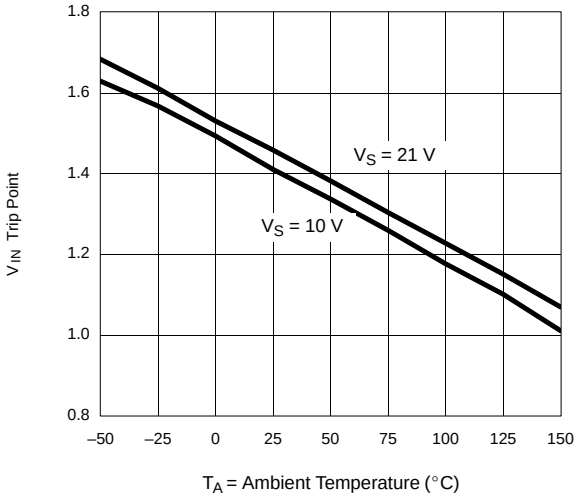


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

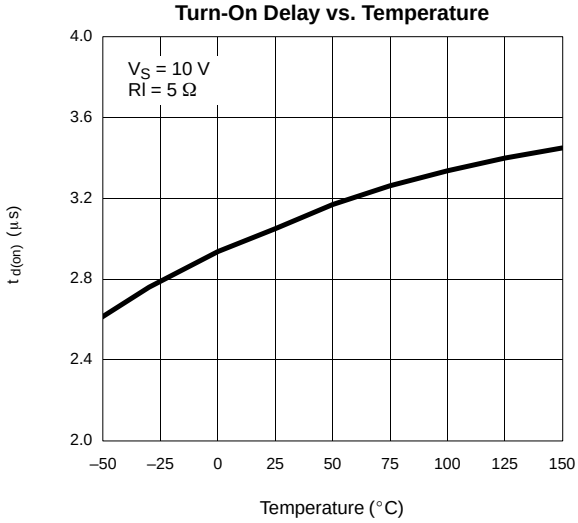
Drain-Source Diode Forward Voltage



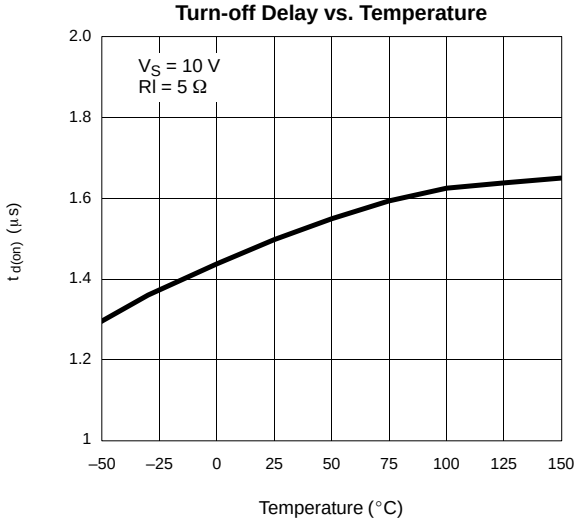
Input Voltage Trip Point vs. Temperature



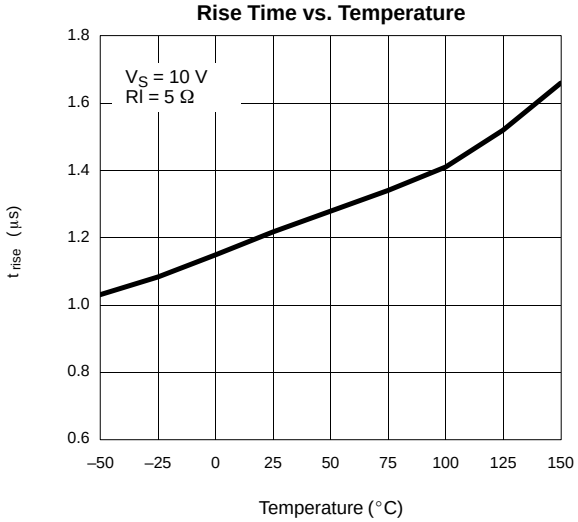
Turn-On Delay vs. Temperature



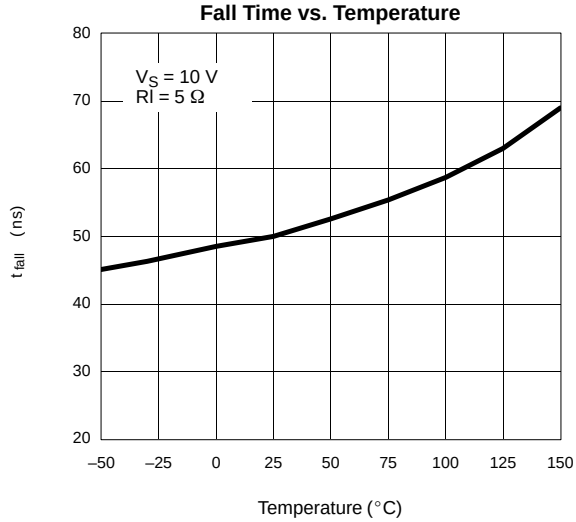
Turn-off Delay vs. Temperature



Rise Time vs. Temperature

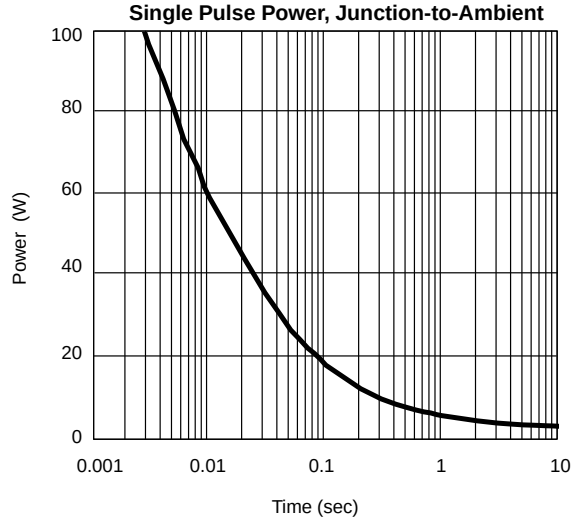


Fall Time vs. Temperature

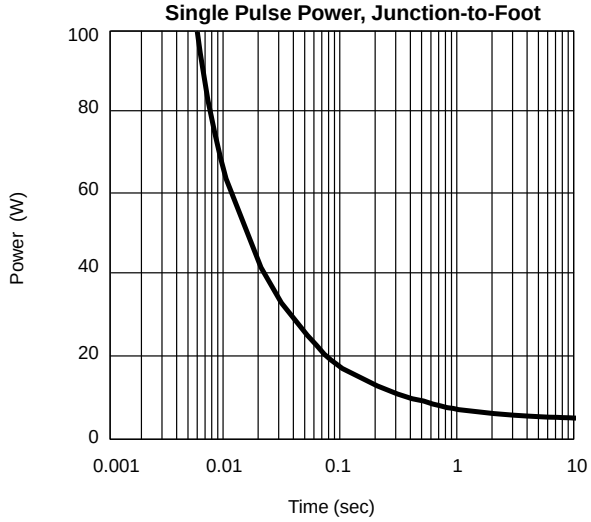


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

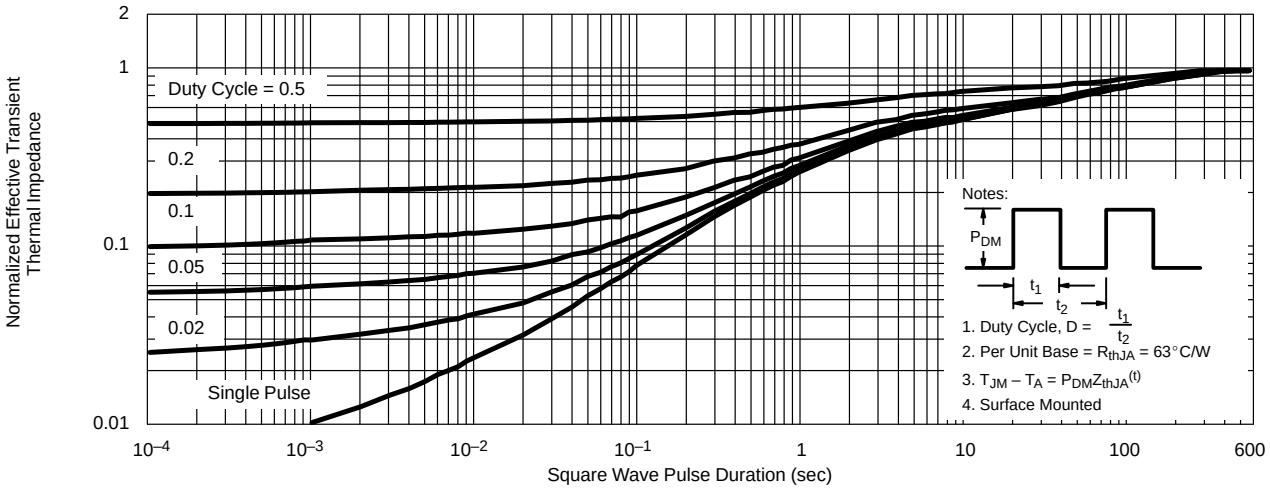
Single Pulse Power, Junction-to-Ambient



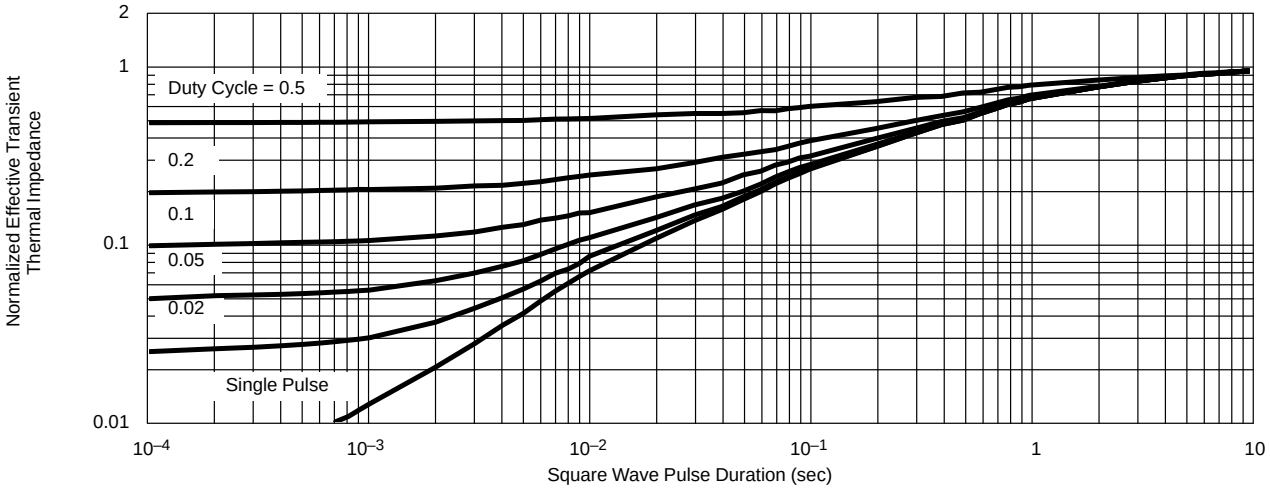
Single Pulse Power, Junction-to-Foot



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



APPLICATION DRAWINGS

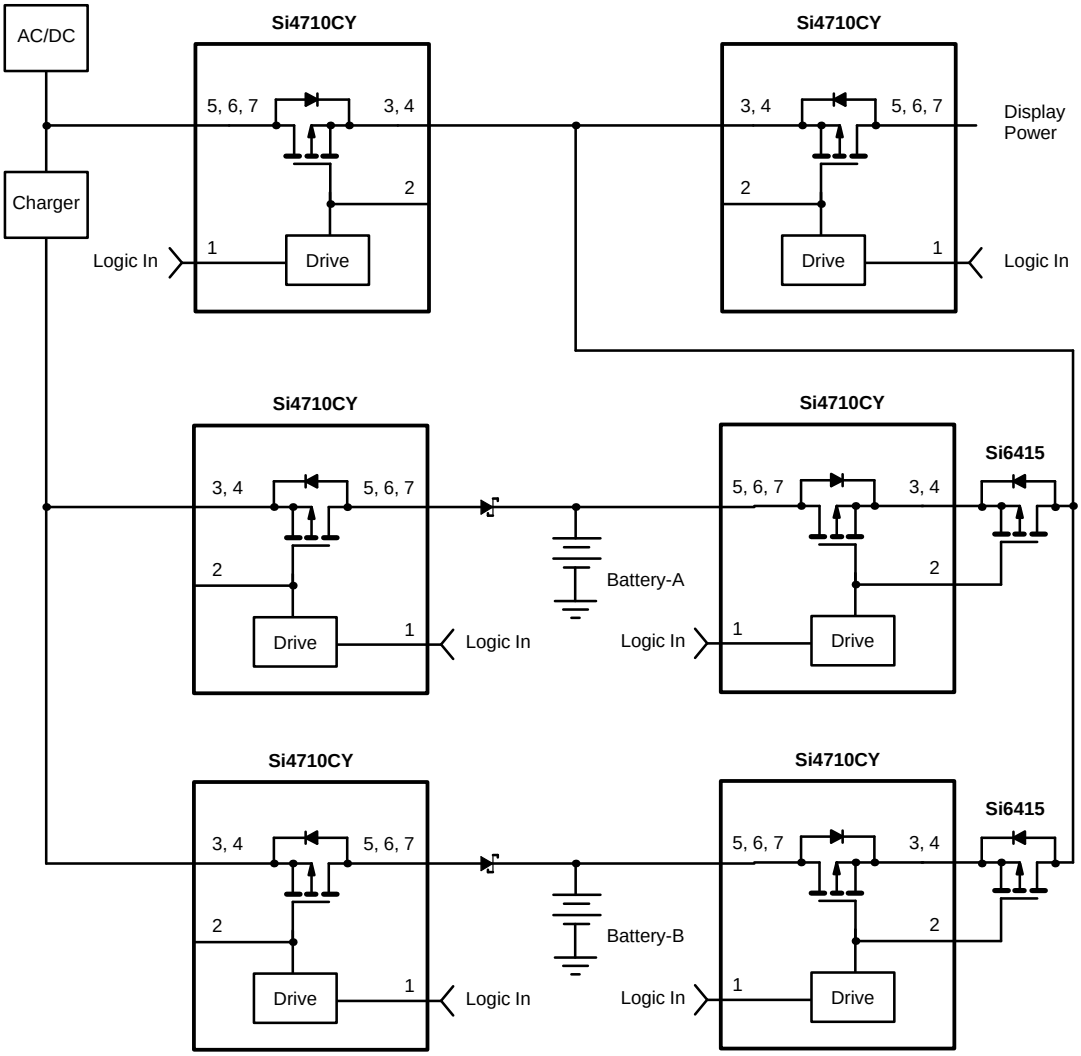


Figure 1: High-Performance Laptop PC

APPLICATION DRAWINGS

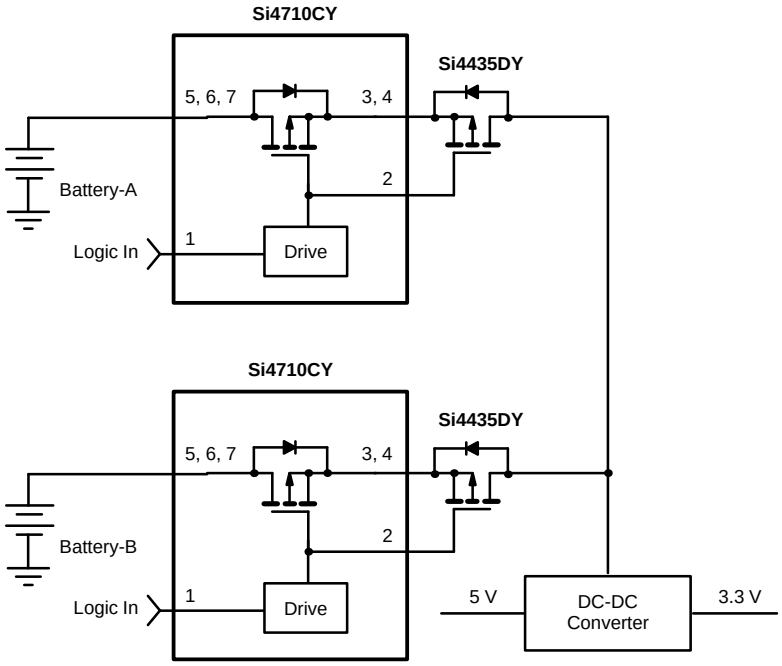


Figure 2:

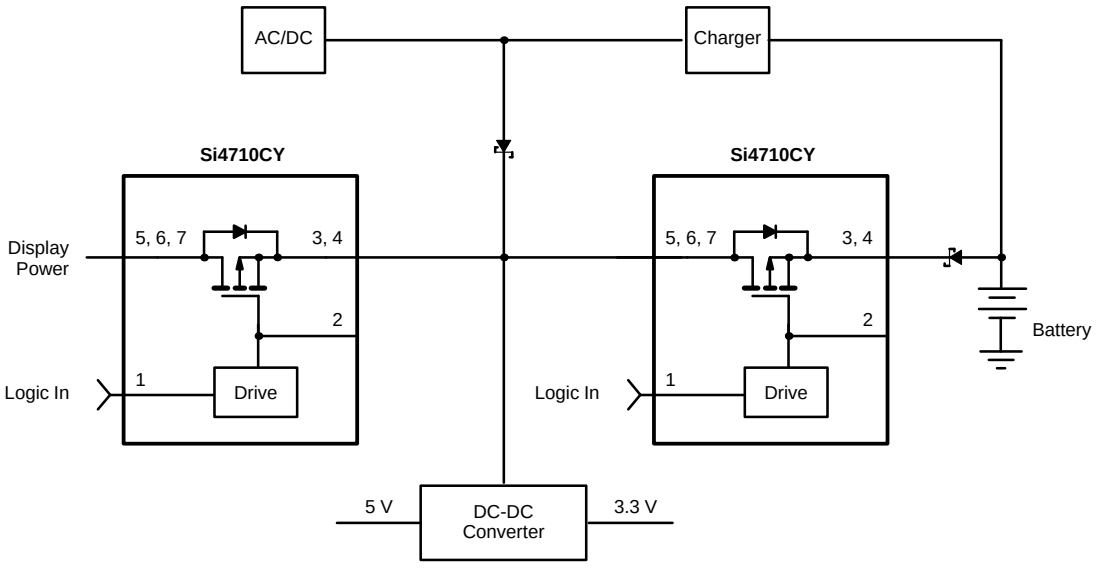


Figure 3: Low-Cost Laptop PC

APPLICATION DRAWINGS

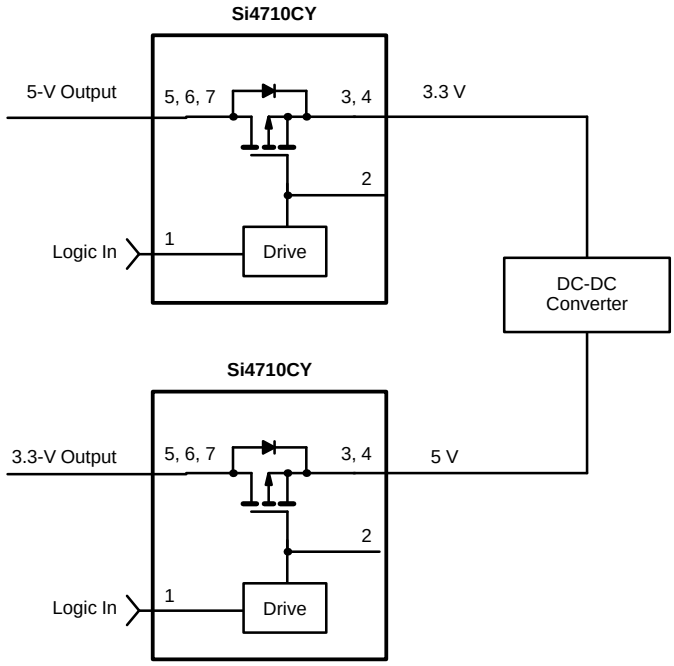


Figure 4: ACPI Power Saving Switcher

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