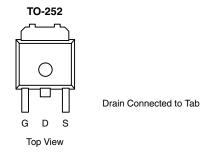




# N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	
20	0.0060 at V <sub>GS</sub> = 10 V	26	
20	0.0095 at V <sub>GS</sub> = 4.5 V	21	



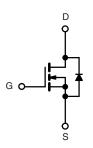
Ordering Information: SUD50N02-06P-E3 (Lead (Pb) free)

## **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- 100 % R<sub>q</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

### **APPLICATIONS**

- Synchronous Buck DC/DC Conversion
  - Desktop
  - Server



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $(T_A =$	: 25 °C, unless othe	rwise noted)		
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	20	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	1 V
	T <sub>A</sub> = 25 °C	I-	26 <sup>a</sup>	
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> = 25 °C	l <sub>D</sub>	50 <sup>b</sup>	
Pulsed Drain Current		I <sub>DM</sub>	100	Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	26	
Avalanche Current	che Current L = 0.1 mH		45	
Single Pulse Avalanche Energy	L = 0.1 IIII1	E <sub>AS</sub>	101	mJ
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	6.8 <sup>a</sup>	w
Maximum Fower Dissipation	T <sub>C</sub> = 25 °C	1 ' <sup>D</sup>	65	T vv
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Marrian con location to Ambient	t ≤ 10 s	- R <sub>thJA</sub>	18	22	°C/W
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		40	50	
Maximum Junction-to-Case	•	R <sub>thJC</sub>	1.9	2.3	

- a. Surface mounted on FR4 board,  $t \le 10 \text{ s.}$
- b. Limited by package.

# Vishay Siliconix



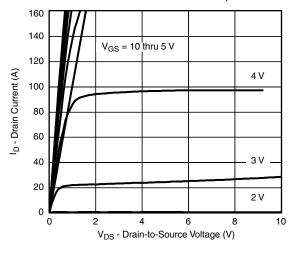
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	20			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.8		3	V
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zana Cata Valta da Duain Comuna	l	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μΑ
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	50			Α
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0046	0.006	
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125 ^{\circ}\text{C}$			0.0084	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.0073	0.0095	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 20 \text{ A}$	15			S
Dynamic <sup>a</sup>						
Input Capacitance	C <sub>iss</sub>			2550		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 10 \text{ V}, f = 1 \text{ MHz}$		900		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			415		
Total Gate Charge <sup>c</sup>	$Q_g$			19	30	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 50 \text{ A}$		7.5		nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			6		
Gate Resistance	$R_g$		0.5	1.5	2.4	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			11	20	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_{L} = 0.2 \Omega$		10	15	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$		24	35	115
Fall Time <sup>c</sup>	t <sub>f</sub>			9	15	
Source-Drain Diode Ratings and Cha	racteristic (T	<sub>C</sub> = 25 °C)		•		
Pulsed Current	I <sub>SM</sub>				100	Α
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		1.2	1.5	V
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	$I_{\rm F} = 50 \text{ A},  dI/dt = 100  A/\mu s$		35	70	ns

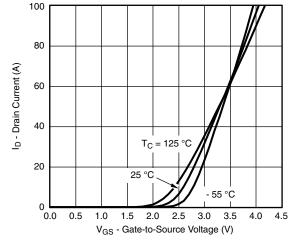
## Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# TYPICAL CHARACTERISTICS (25 °C unless noted)

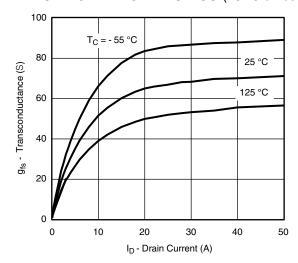




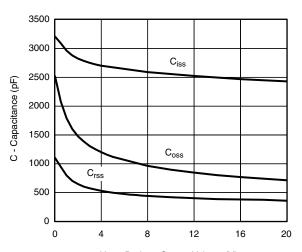
**Output Characteristics Transfer Characteristics** 



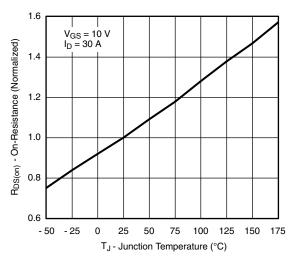
# TYPICAL CHARACTERISTICS (25 °C unless noted)



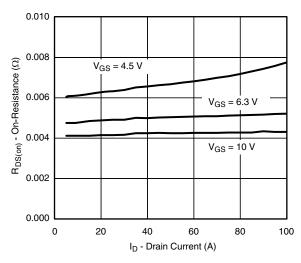
### **Transconductance**



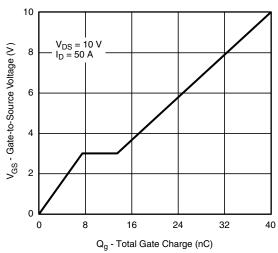
V<sub>DS</sub> - Drain-to-Source Voltage (V) Capacitance



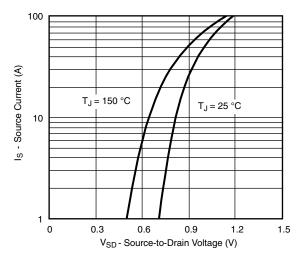
On-Resistance vs. Junction Temperature



On-Resistance vs. Drain Current



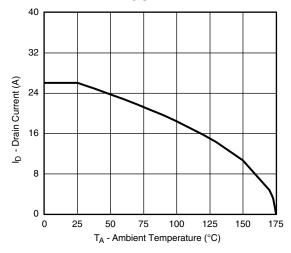
**Gate Charge** 

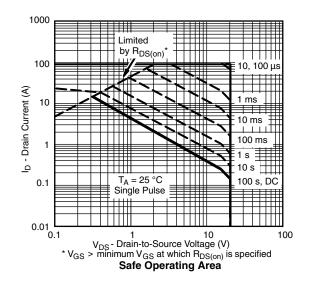


Source-Drain Diode Forward Voltage

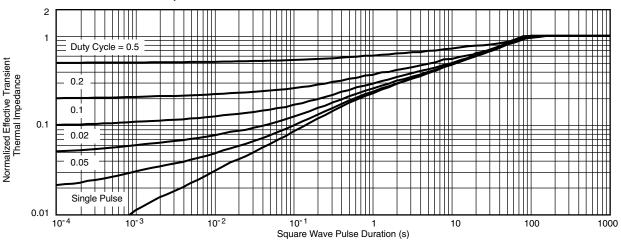
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### THERMAL RATINGS

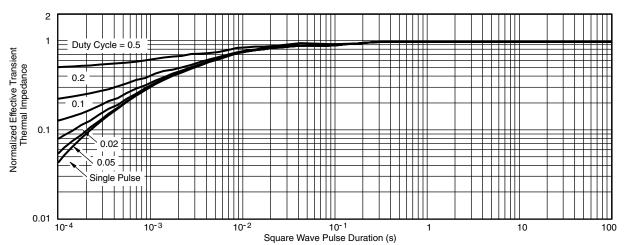












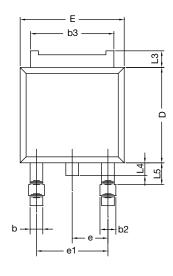
Normalized Thermal Transient Impedance, Junction-to-Case

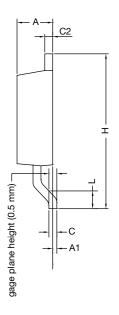
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71931.

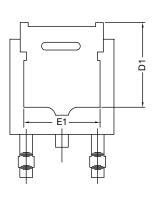


# **TO-252AA Case Outline**

# **VERSION 1: FACILITY CODE = Y**







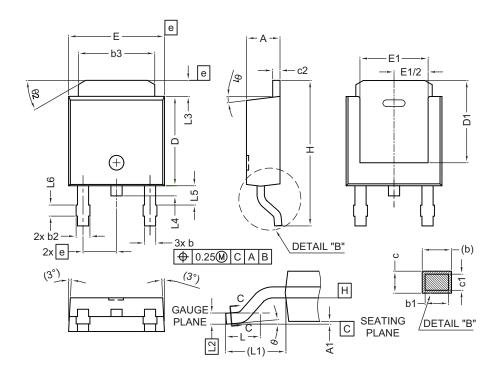
	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	2.18	2.38	
A1	-	0.127	
b	0.64	0.88	
b2	0.76	1.14	
b3	4.95	5.46	
С	0.46	0.61	
C2	0.46	0.89	
D	5.97	6.22	
D1	4.10	-	
Е	6.35	6.73	
E1	4.32	-	
Н	9.40	10.41	
е	2.28 BSC		
e1	4.56 BSC		
L	1.40	1.78	
L3	0.89	1.27	
L4	-	1.02	
L5	1.01	1.52	

### Note

• Dimension L3 is for reference only



## **VERSION 2: FACILITY CODE = N**



	MILLIMETERS		
DIM.	MIN.	MAX.	
А	2.18	2.39	
A1	-	0.13	
b	0.65	0.89	
b1	0.64	0.79	
b2	0.76	1.13	
b3	4.95	5.46	
С	0.46	0.61	
c1	0.41	0.56	
c2	0.46	0.60	
D	5.97	6.22	
D1	5.21	-	
Е	6.35	6.73	
E1	4.32	-	
е	2.29 BSC		
Н	9.94	10.34	

	MILLIMETERS		
DIM.	MIN.	MAX.	
L	1.50	1.78	
L1	2.74	ref.	
L2	0.51 BSC		
L3	0.89	1.27	
L4	-	1.02	
L5	1.14	1.49	
L6	0.65	0.85	
θ	0°	10°	
θ1	0°	15°	
θ2	25°	35°	

## Notes

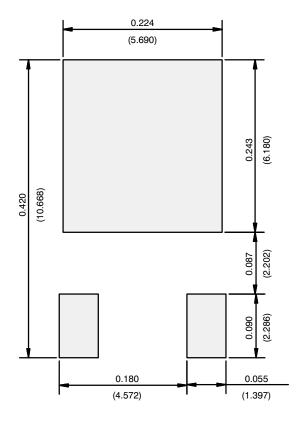
- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022

DWG: 5347



# **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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