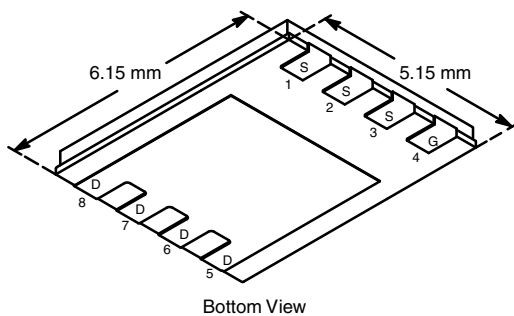


## N-Channel Reduced $Q_g$ , Fast Switching MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.00975 at $V_{GS} = 10$ V	15
	0.01375 at $V_{GS} = 4.5$ V	13

PowerPAK SO-8



Bottom View

Ordering Information: Si7392DP-T1-E3 (Lead (Pb)-free)  
Si7392DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

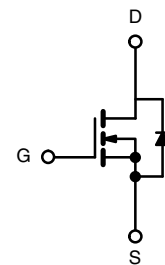
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low  $Q_{gd}$  for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 %  $R_g$  Tested
- 100 % UIS Tested
- Complaint to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

### APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook
  - Server



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	30		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	15	9	A
	T <sub>A</sub> = 70 °C		12	7	
Pulsed Drain Current		I <sub>DM</sub>	± 50		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	4.1	1.5	
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	30		mJ
Single-Pulse Avalanche Energy		E <sub>AS</sub>	45		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5	1.8	W
	T <sub>A</sub> = 70 °C		3.2	1.1	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260		

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) <sup>a</sup>	$R_{thJA}$	20	25	°C/W
		53	70	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	3.5	4.5	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

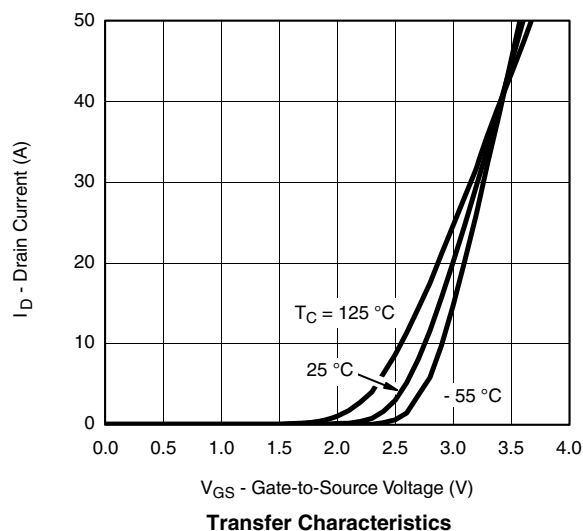
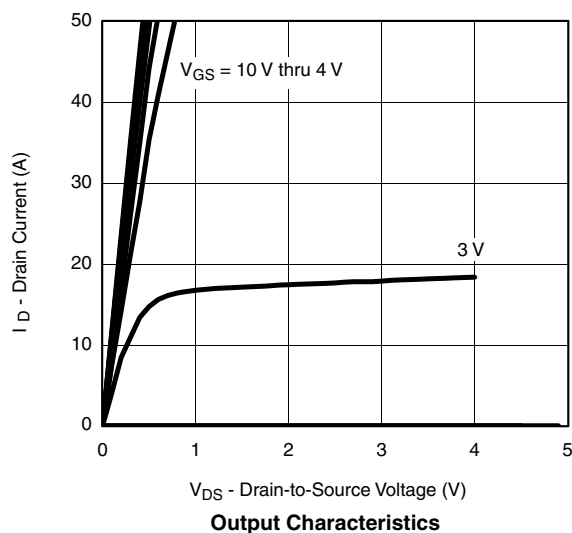
<b>MOSFET SPECIFICATIONS</b> ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^{\circ}\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$		0.008	0.00975	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 13\text{ A}$		0.011	0.01375	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 15\text{ A}$		40		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 4.1\text{ A}$ , $V_{GS} = 0\text{ V}$		0.75	1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 15\text{ A}$		10	15	nC
Gate-Source Charge	$Q_{gs}$			3.5		
Gate-Drain Charge	$Q_{gd}$			2.6		
Gate Resistance	$R_g$			1.6	2.7	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ $I_D \equiv 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 6\text{ }\Omega$		15	25	ns
Rise Time	$t_r$			7	15	
Turn-Off Delay Time	$t_{d(off)}$			46	70	
Fall Time	$t_f$			9	17	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.7\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$		30	60	

Notes:

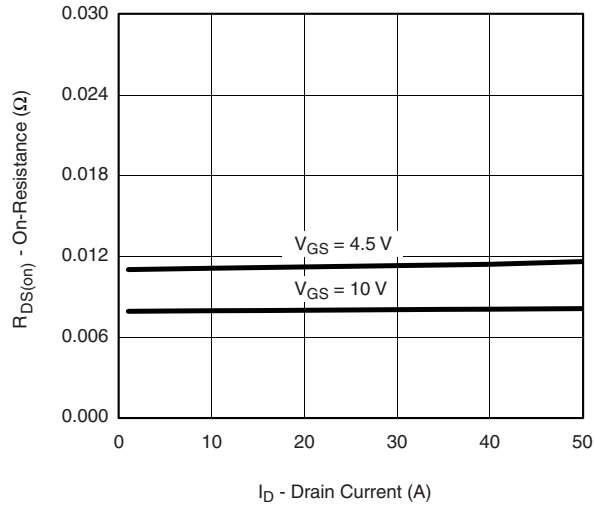
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

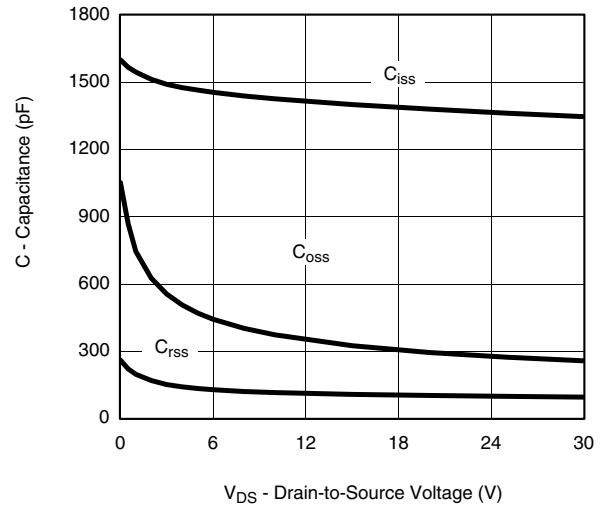
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

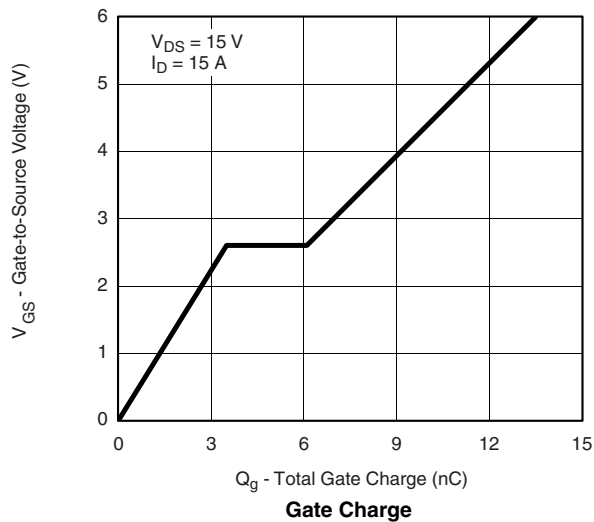
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



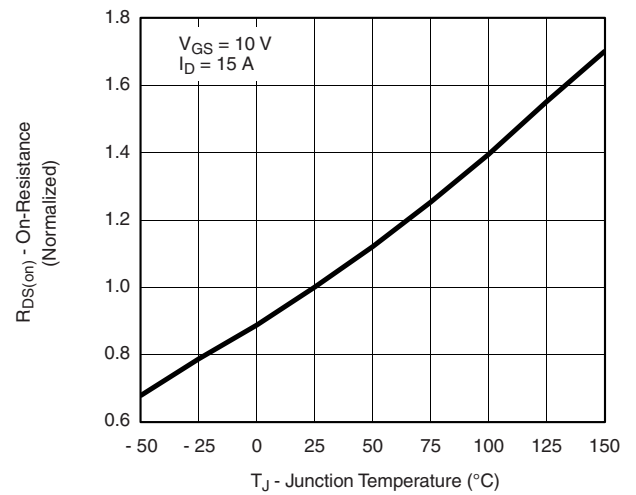
On-Resistance vs. Drain Current



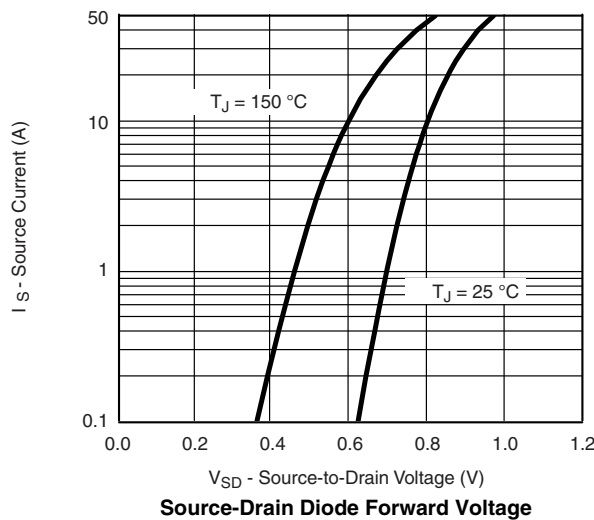
Capacitance



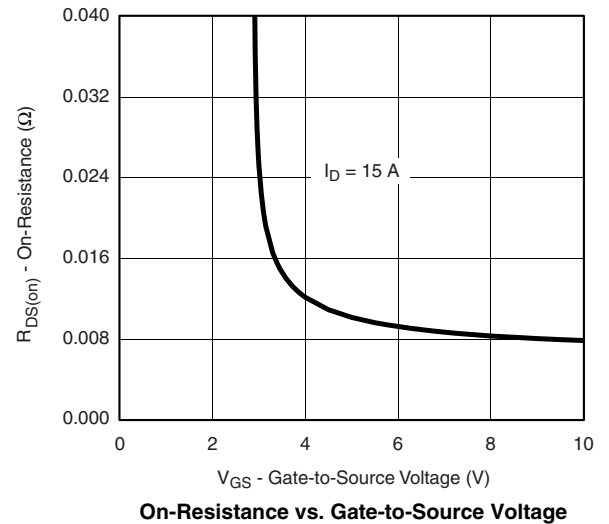
Gate Charge



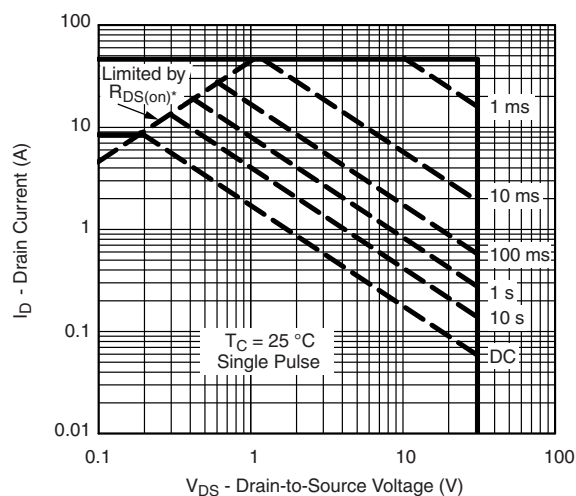
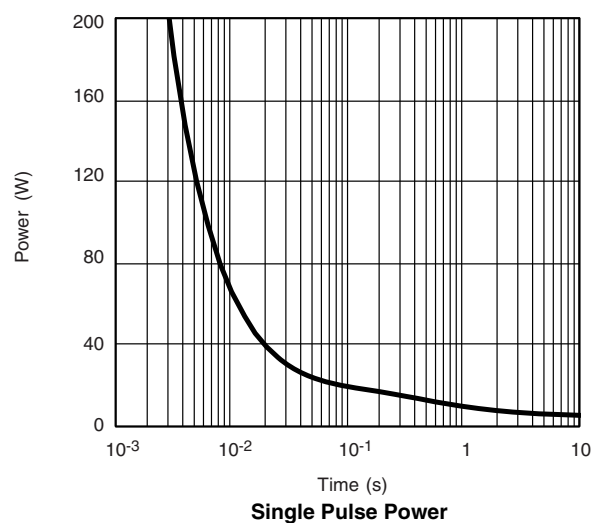
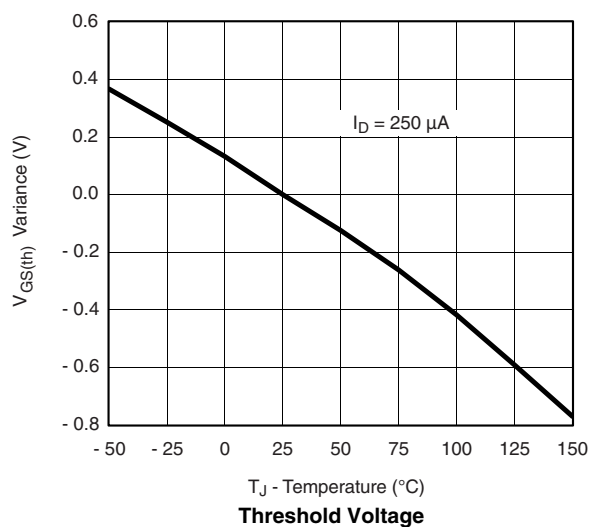
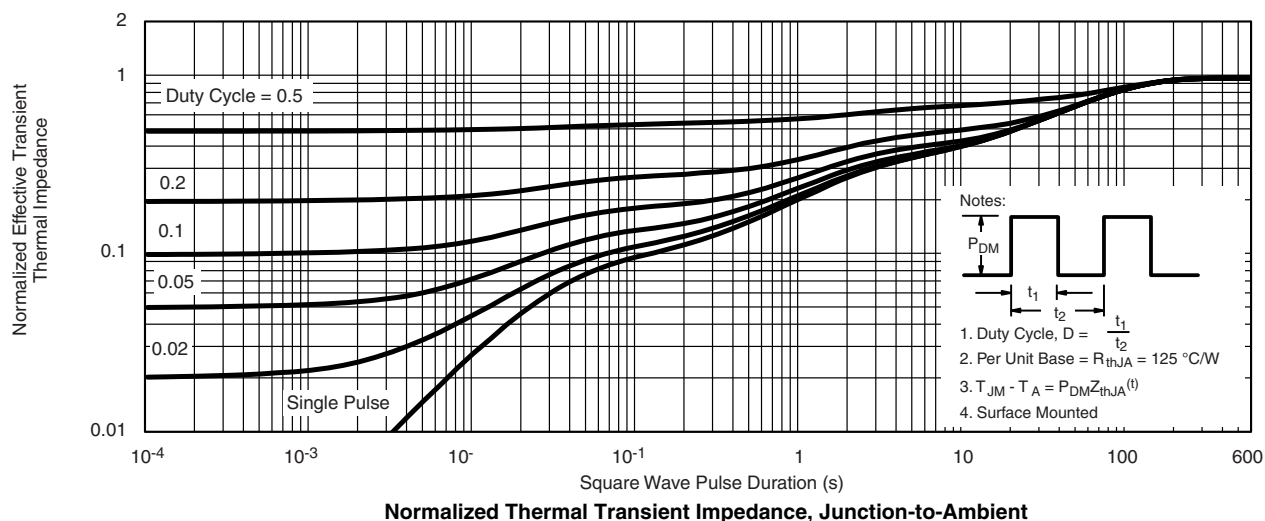
On-Resistance vs. Junction Temperature



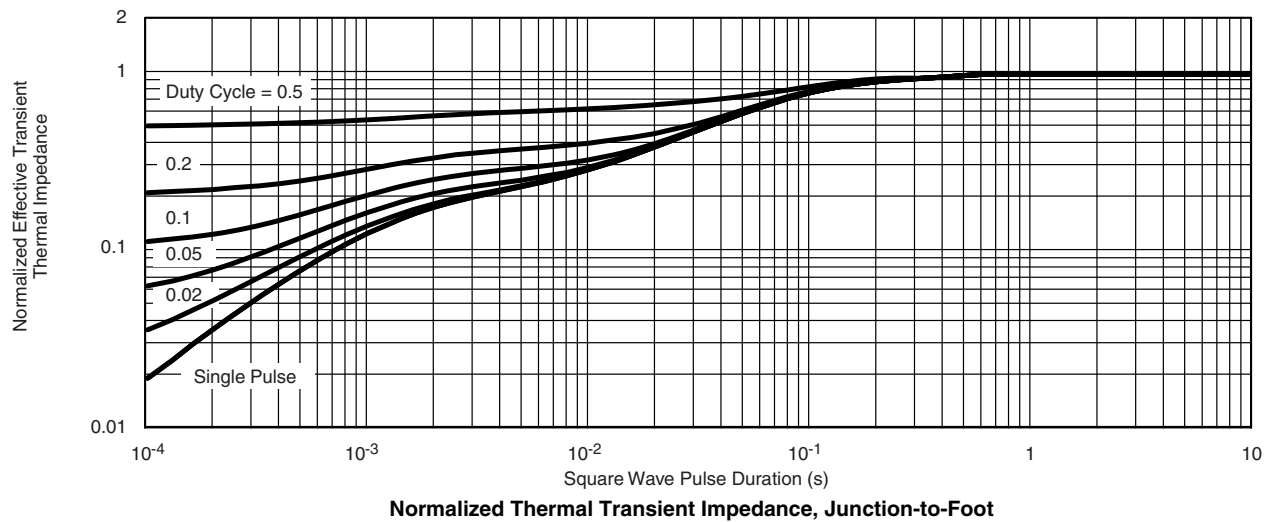
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



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