N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a] Silicon Limit	I_D (A)[a] Package Limit	Q_g (Typ)
30	0.0042 at V_{GS} = 10 V	120	50	33 nC
	0.0048 at V_{GS} = 4.5 V	112	50	

Package Drawing

FEATURES

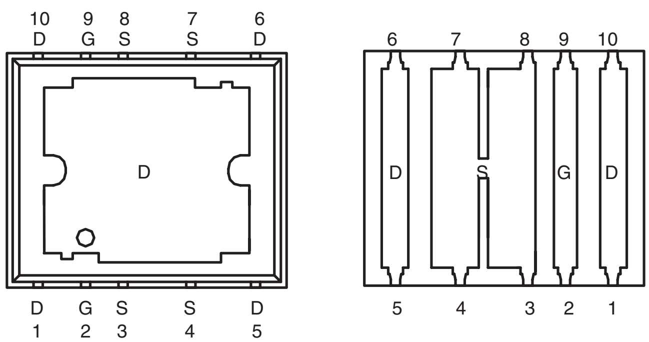
- Extremely Low Q_{gd} WFET® Technology for Low Switching Losses
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
  - Die Not Exposed
  - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested

RoHS COMPLIANT

APPLICATIONS

- VRM
- Point-of-Load
- Synchronous Rectification

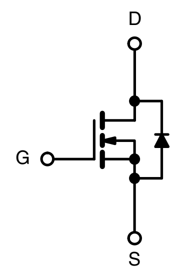
PolarPAK



Top View Bottom View

Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE830DF-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

For Related Documents

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	120 (Silicon Limit)	A
			50[a] (Package Limit)	
	T_C = 70 °C		50[a]	
	T_A = 25 °C		27[b, c]	
	T_A = 70 °C		21.6[b, c]	
Pulsed Drain Current		I_{DM}	80	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	50[a]	
	T_A = 25 °C		4.3[b, c]	
Single Pulse Avalanche Current	T_C = 25 °C	I_{AS}	30	A
Avalanche Energy		E_{AS}	45	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	104	W
	T_C = 70 °C		66	
	T_A = 25 °C		5.2[b, c]	
	T_A = 70 °C		3.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

Notes:
a. Package limited is 50 A.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 sec.
d. See Solder Profile (http://www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	$t \leq 10$ sec	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)[a]	Steady State	R_{thJC} (Drain)	1	1.2	
Maximum Junction-to-Case (Source)[a, c]		R_{thJC} (Source)	2.8	3.4	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Maximum under Steady State conditions is 68 °C/W.
c. Measured at source pin (on the side of the package).

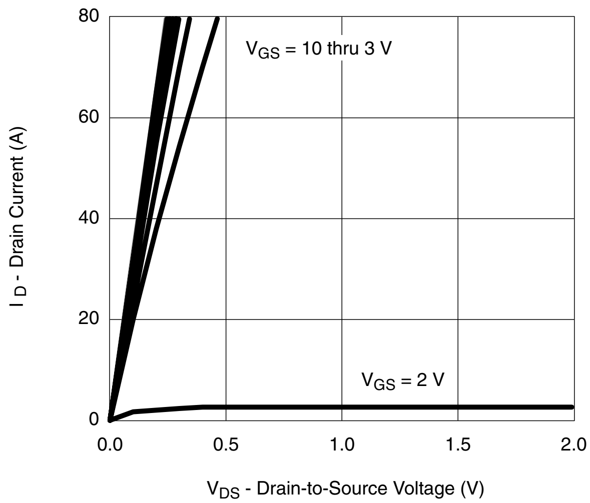
SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		30		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.6	1.4	2	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, V_{GS} = 10 V	25			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 16 A		0.0035	0.0042	Ω
		V_{GS} = 4.5 V, I_D = 15 A		0.0039	0.0048	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 16 A		95		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		3000		pF
Output Capacitance	C_{oss}			650		
Reverse Transfer Capacitance	C_{rss}			220		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A		75	115	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A		33	50	
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			5.1		
Gate Resistance	R_g	f = 1 MHz		1.0	1.5	Ω
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong 10$ A, V_{GEN} = 4.5 V, R_g = 1 Ω		35	55	ns
Rise Time	t_r			105	160	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			95	145	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong 10$ A, V_{GEN} = 10 V, R_g = 1 Ω		15	25	
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			50	A
Pulse Diode Forward Current[a]	I_{SM}				80	
Body Diode Voltage	V_{SD}	I_S = 10 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, di/dt = 100 A/µs, T_J = 25 °C		40	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			40	60	nC
Reverse Recovery Fall Time	t_a			22		ns
Reverse Recovery Rise Time	t_b			18		

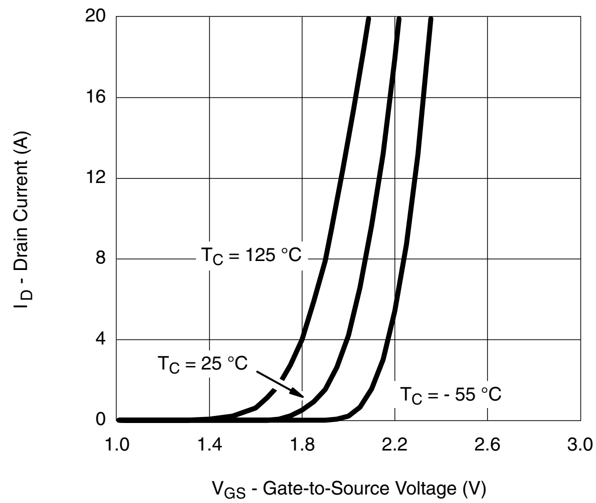
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

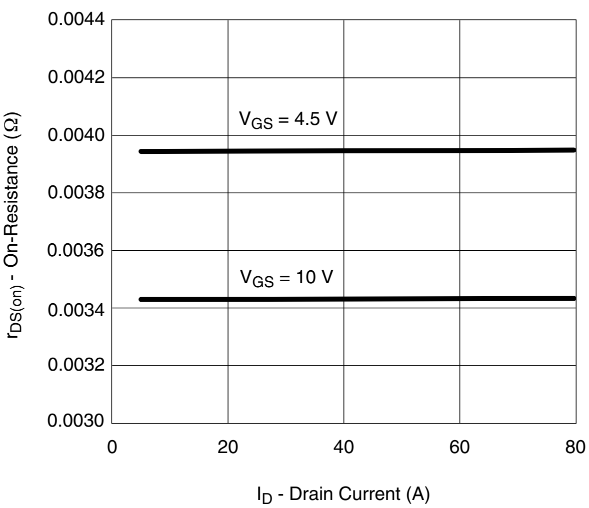
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



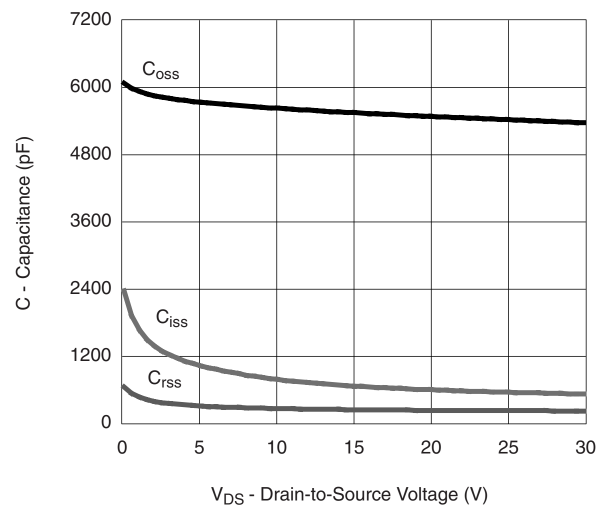
Output Characteristics



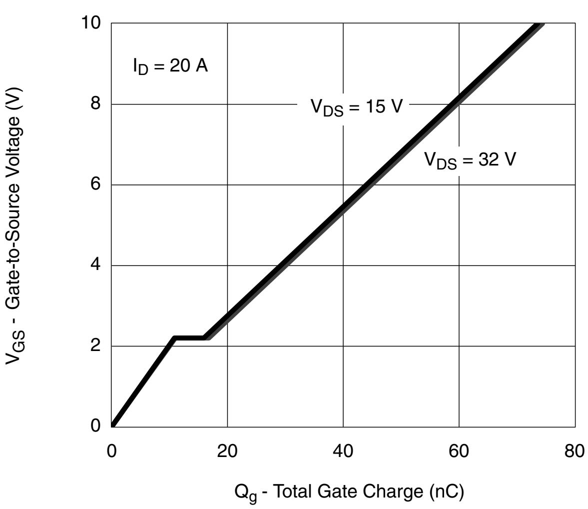
Transfer Characteristics



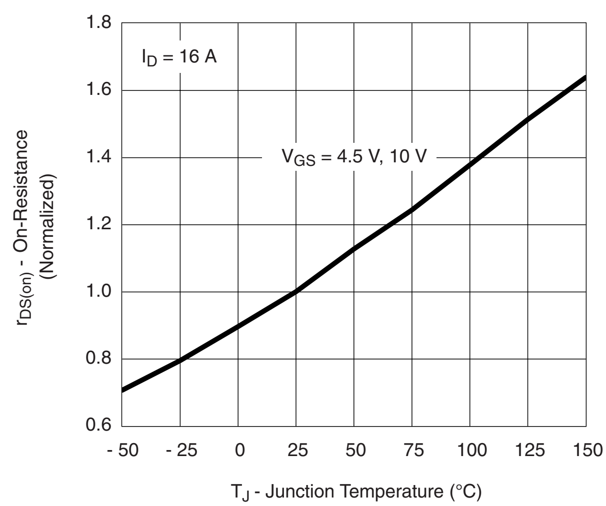
On-Resistance vs. Drain Current



Capacitance

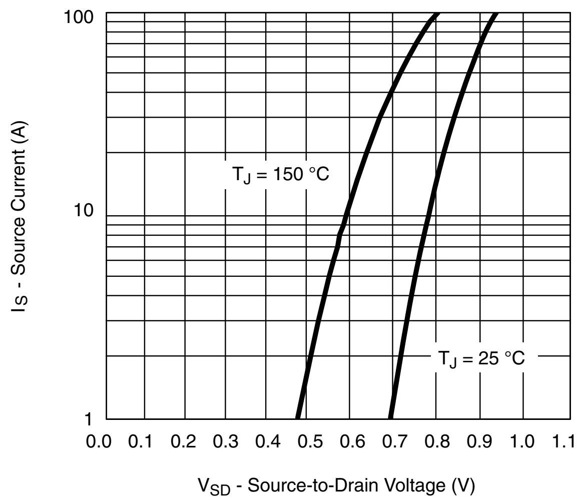


Gate Charge

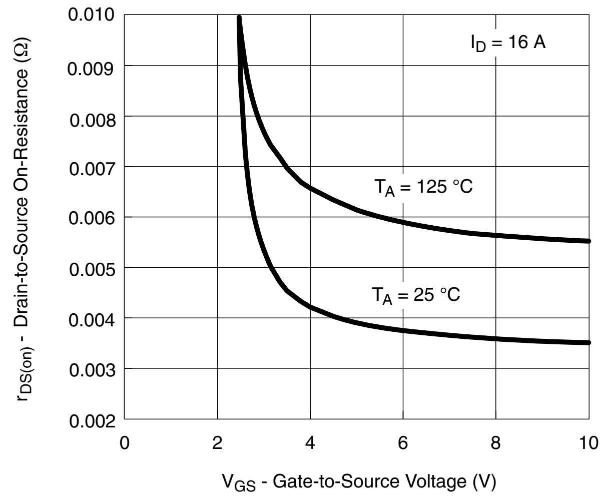


On-Resistance vs. Junction Temperature

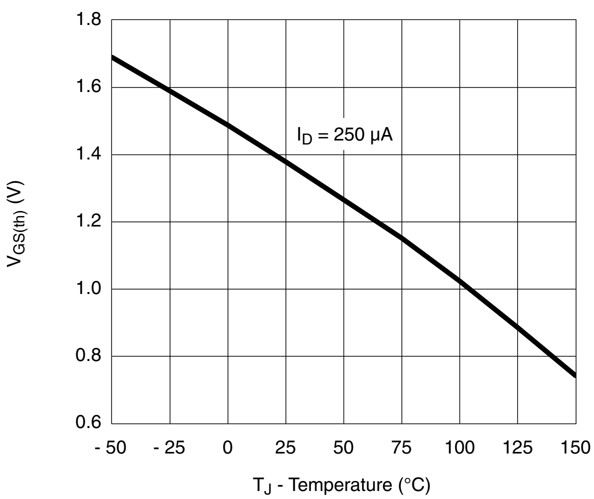
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



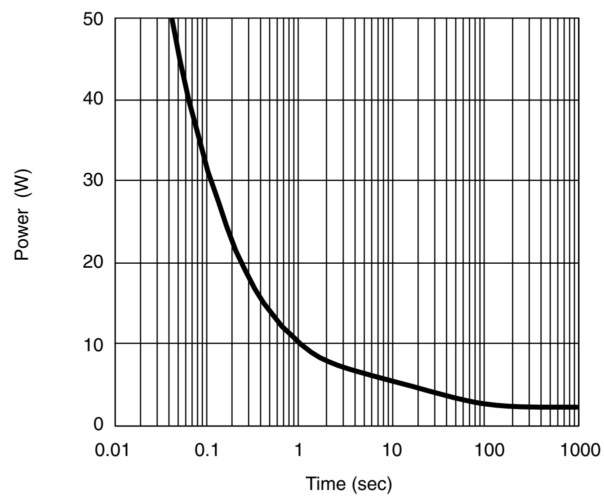
Source-Drain Diode Forward Voltage



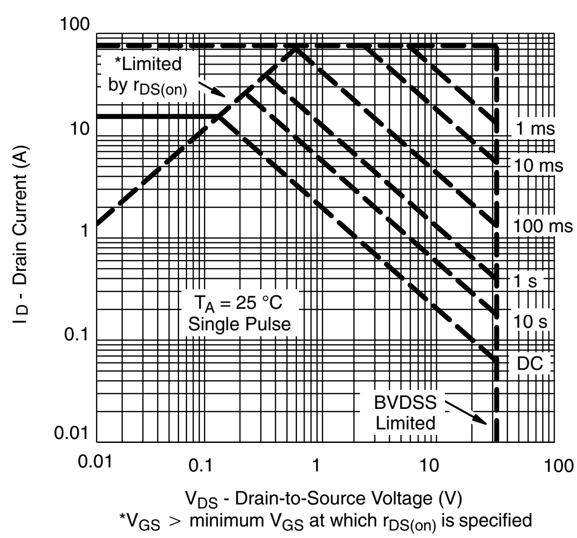
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

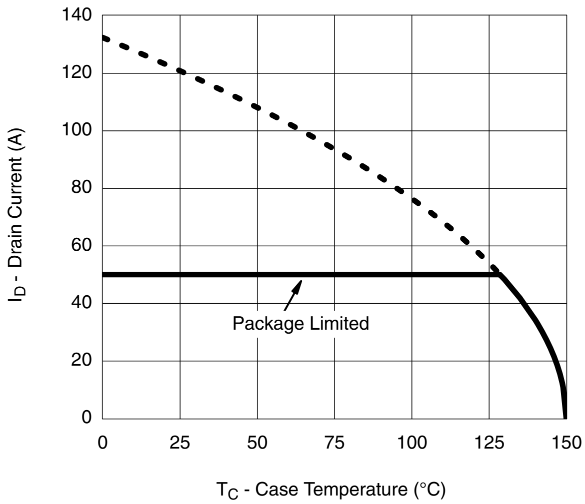


Single Pulse Power, Junction-to-Ambient

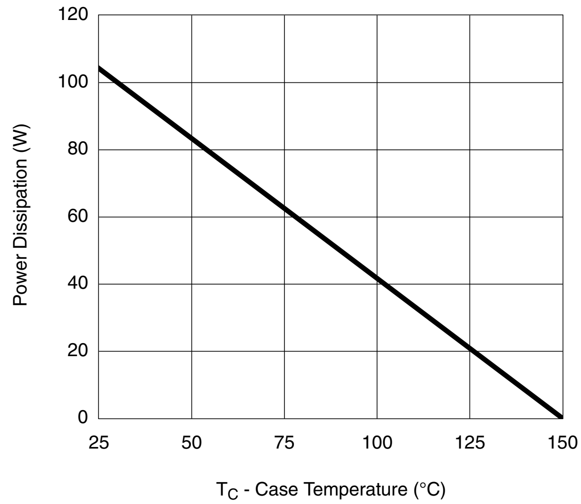


Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



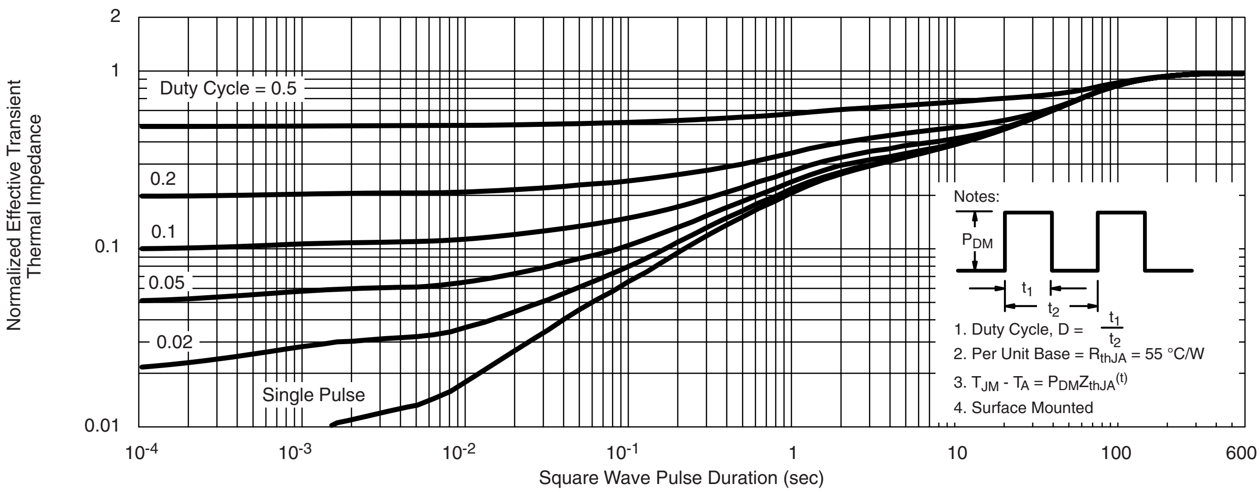
Current Derating*



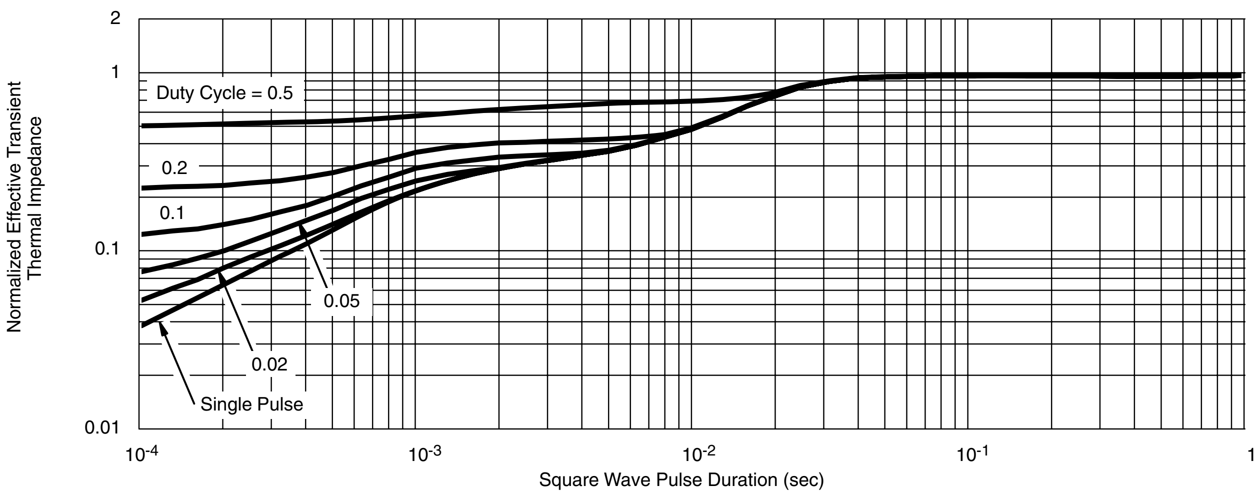
Power Derating, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

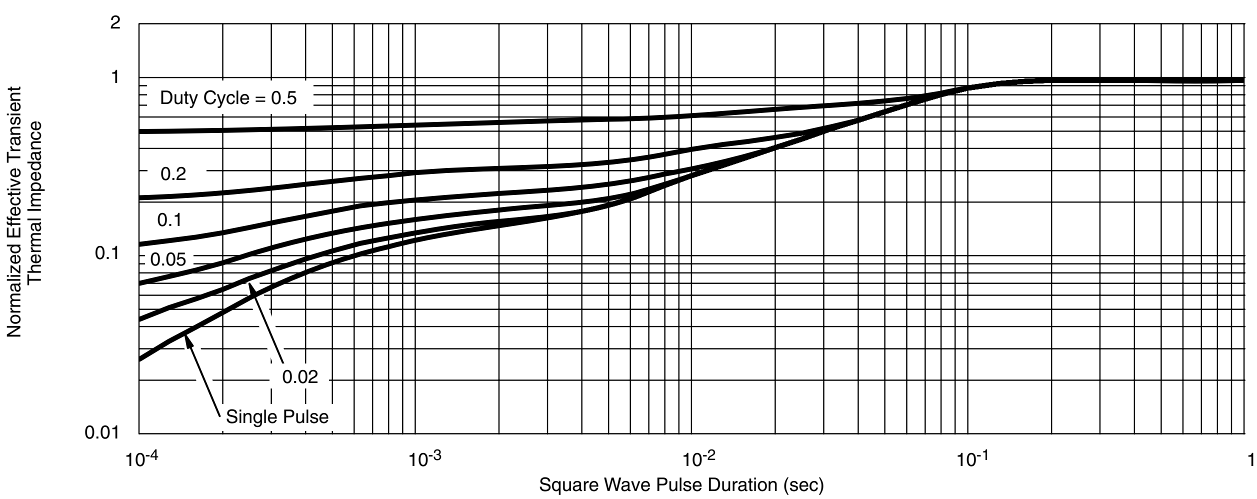
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



Normalized Thermal Transient Impedance, Junction-to-Source

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