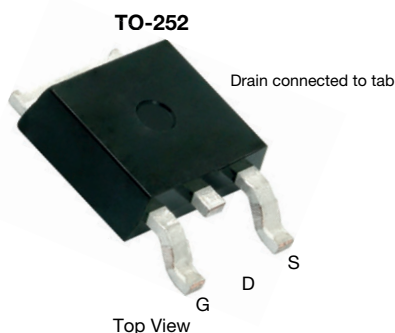


# Automotive P-Channel 40 V (D-S) 175 °C MOSFET

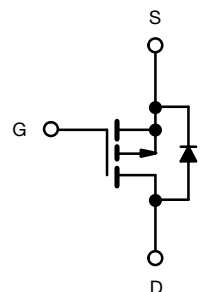


## FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R<sub>g</sub> and UIS tested
- AEC-Q101 qualified
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



P-Channel MOSFET

## PRODUCT SUMMARY

V <sub>DS</sub> (V)	-40
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = -10 V	0.0085
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = -4.5 V	0.0105
I <sub>D</sub> (A)	-50
Configuration	Single
Package	TO-252

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V <sub>DS</sub>	-40	V
Gate-source voltage	V <sub>GS</sub>	± 20	
Continuous drain current <sup>a</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	-50
		T <sub>C</sub> = 125 °C	-38
Continuous source current (diode conduction) <sup>a</sup>	I <sub>S</sub>	-50	A
Pulsed drain current <sup>b</sup>	I <sub>DM</sub>	-200	
Single pulse avalanche current	I <sub>AS</sub>	-35	
Single pulse avalanche energy	E <sub>AS</sub>	61	mJ
Maximum power dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	71
		T <sub>C</sub> = 125 °C	23
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R <sub>thJA</sub>	50	°C/W
Junction-to-case (drain)	R <sub>thJC</sub>	2.1	

### Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA		-40	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-1.5	-2.0	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V	-	-	-1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 175 °C	-	-	-200	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≤ -5 V	-50	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -25 A	-	0.0070	0.0085	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -25 A, T <sub>J</sub> = 125 °C	-	-	0.0110	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -25 A, T <sub>J</sub> = 175 °C	-	-	0.0131	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -20 A	-	0.0086	0.0105	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -25 A		-	92	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -25 V, f = 1 MHz	-	7365	9950	pF
Output capacitance	C <sub>oss</sub>			-	576	800	
Reverse transfer capacitance	C <sub>rss</sub>			-	548	750	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -20 V, I <sub>D</sub> = -50 A	-	138	210	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	21	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	21	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		1.5	3.15	4.8	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -20 V, R <sub>L</sub> = 0.4 Ω I <sub>D</sub> ≅ -50 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		-	13	20	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	81	130	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	103	160	
Fall time <sup>c</sup>	t <sub>f</sub>			-	153	250	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-200	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V		-	-0.96	-1.5	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -30 A, di/dt = 100 A/μs		-	56	120	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	83	170	nC
Reverse recovery fall time	t <sub>a</sub>			-	34	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	22	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-3.8	-	A

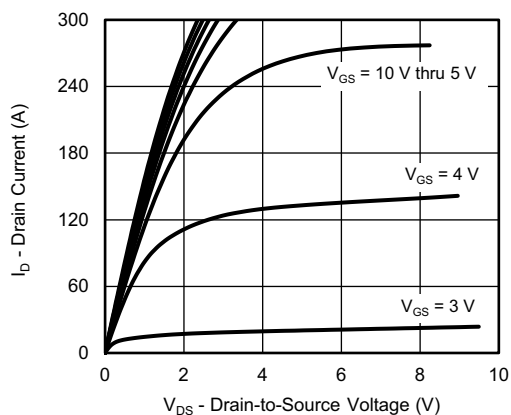
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

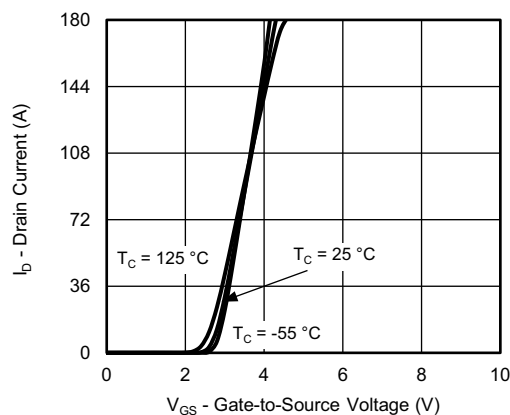
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



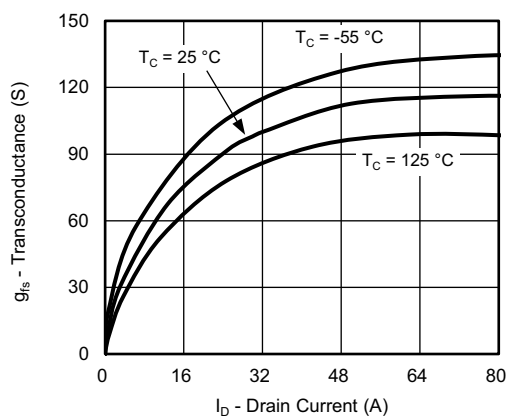
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



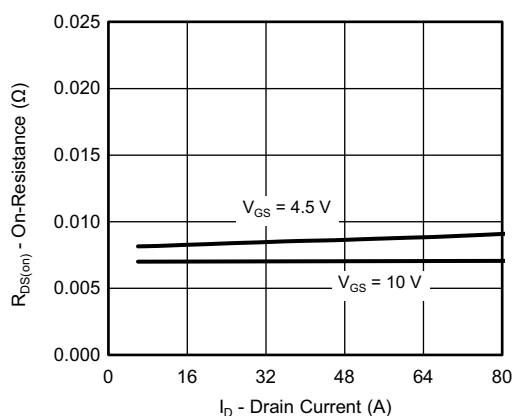
**Output Characteristics**



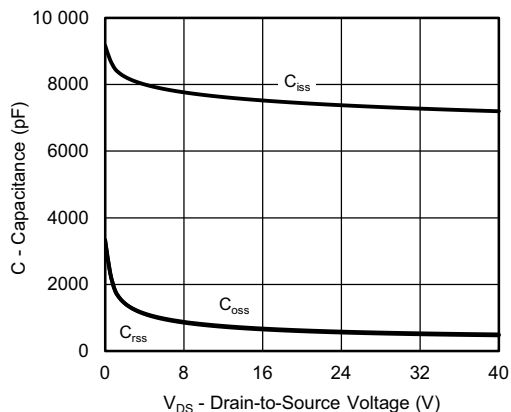
**Transfer Characteristics**



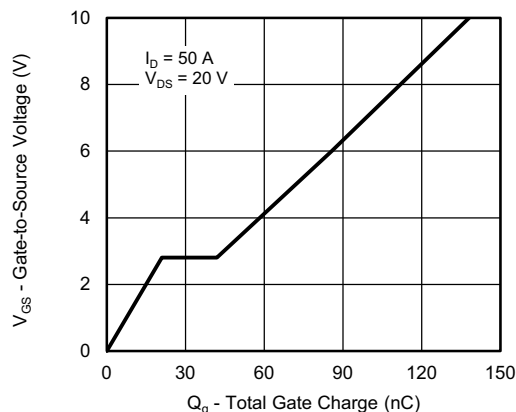
**Transconductance**



**On-Resistance vs. Drain Current**



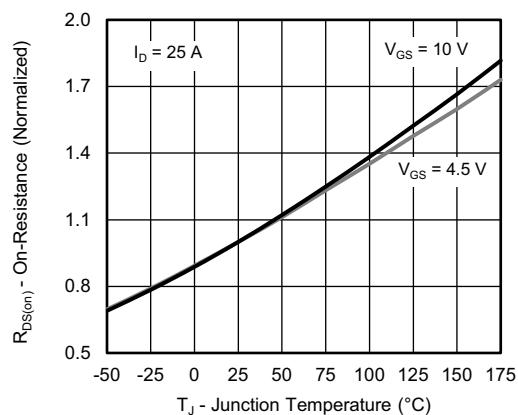
**Capacitance**



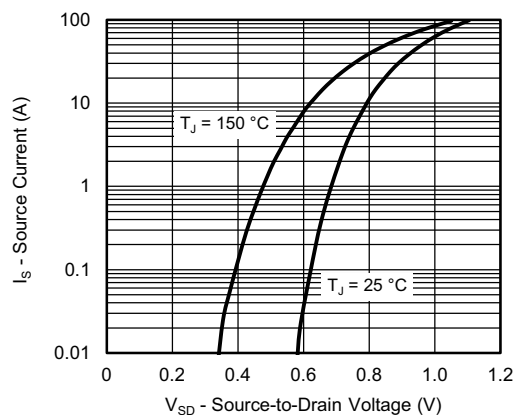
**Gate Charge**



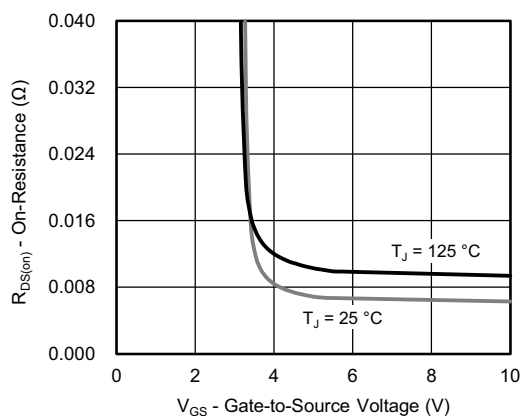
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



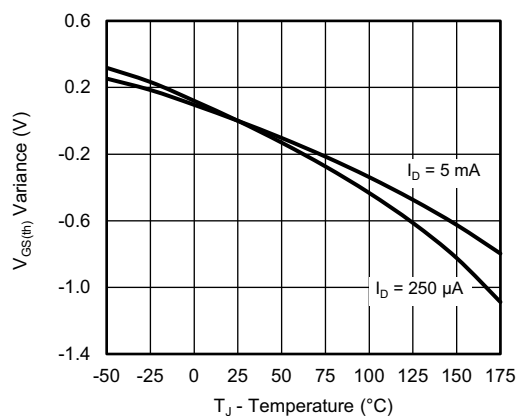
**On-Resistance vs. Junction Temperature**



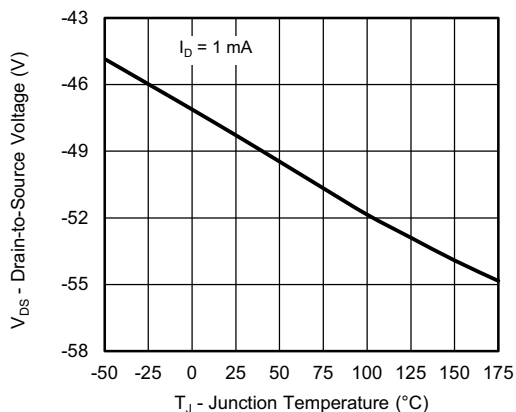
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



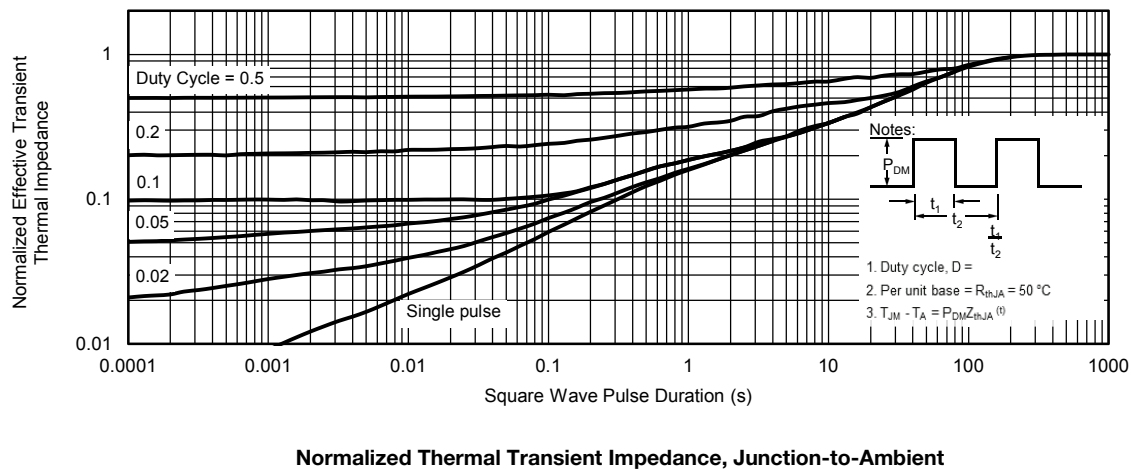
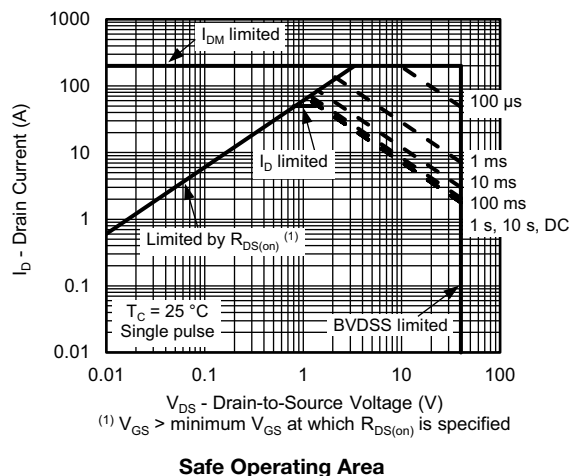
**Threshold Voltage**



**Drain Source Breakdown vs. Junction Temperature**

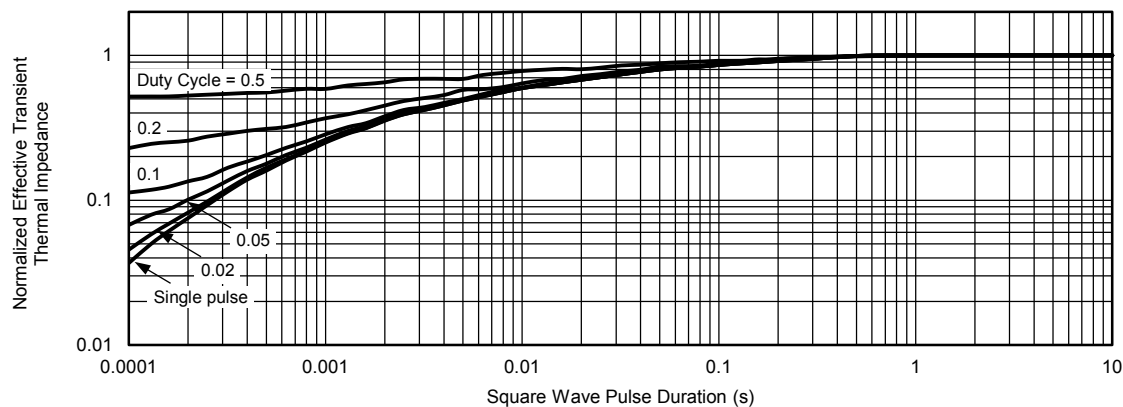


**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)





**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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## TO-252AA Case Outline

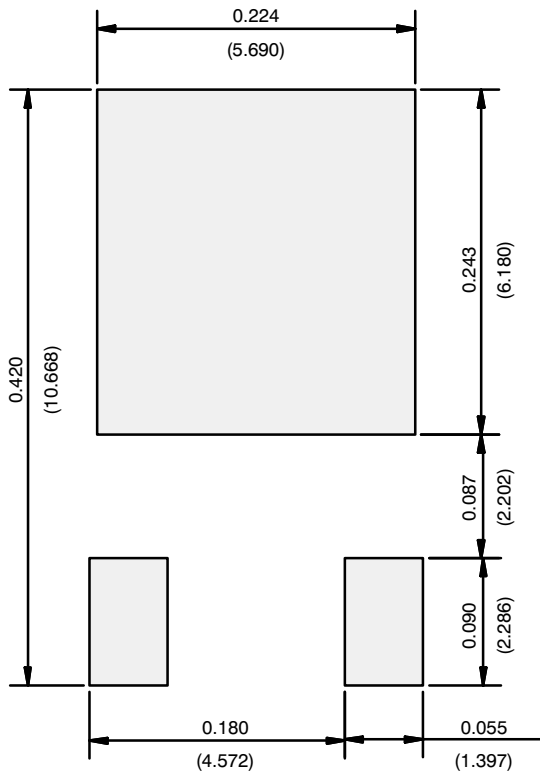


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13 DWG: 6019				

### Note

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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