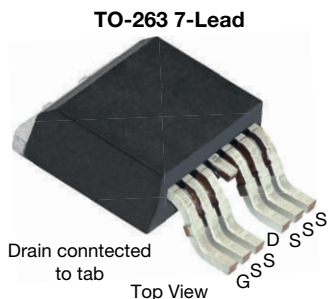


# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

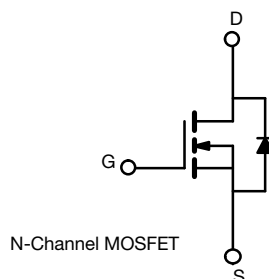


## FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 %  $R_g$  and UIS tested
- AEC-Q101 qualified
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.00163
$I_D$ (A)	150
Configuration	Single
Package	TO-263-7L

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	40	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current	$T_C = 25$ °C <sup>a</sup>	$I_D$	150	A
	$T_C = 125$ °C		125	
Continuous source current (diode conduction) <sup>a</sup>		$I_S$	136	
Pulsed drain current <sup>b</sup>		$I_{DM}$	300	
Single pulse avalanche current		$I_{AS}$	60	
Single pulse avalanche energy		$E_{AS}$	180	mJ
Maximum power dissipation <sup>b</sup>	$T_C = 25$ °C	$P_D$	150	W
	$T_C = 125$ °C		50	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-case (drain)		$R_{thJC}$	1	

## Notes

- a. Package limited  
b. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %  
c. When mounted on 1" square PCB (FR4 material)

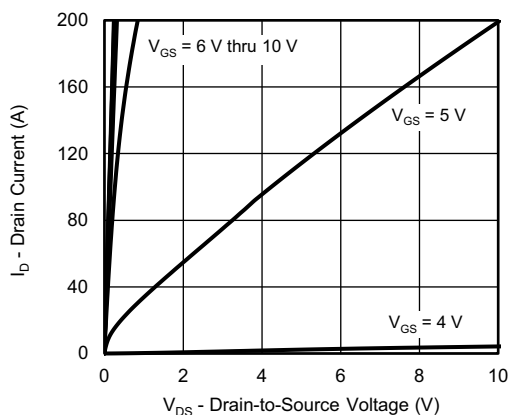
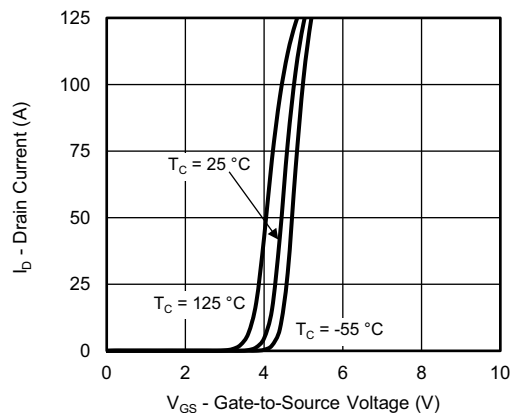
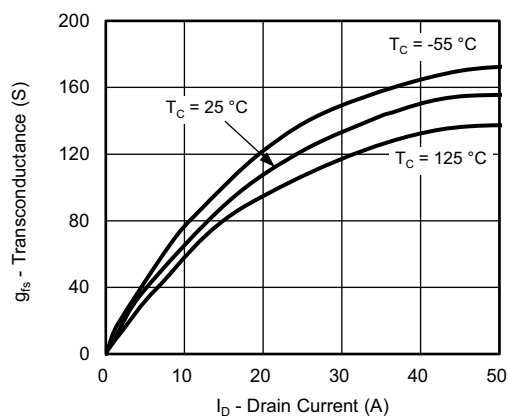
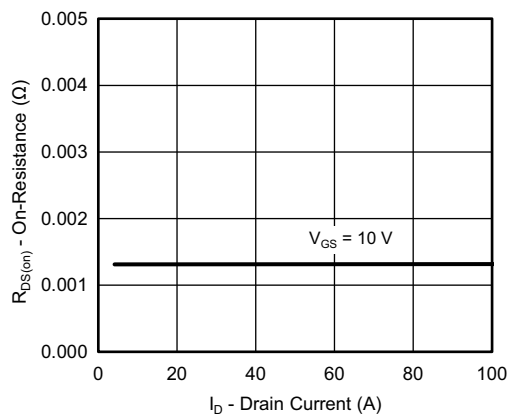
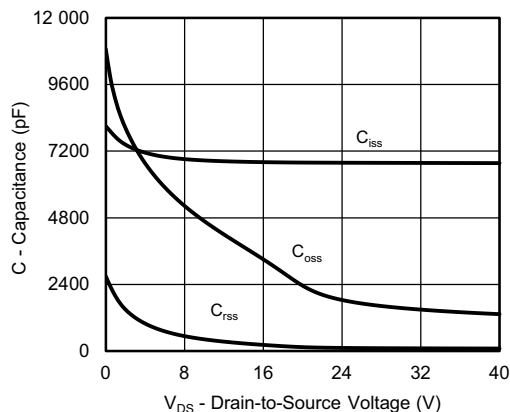
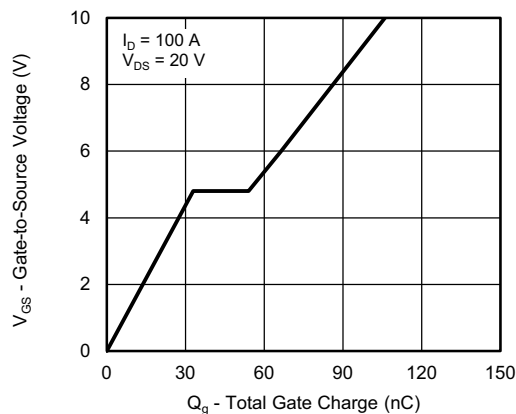


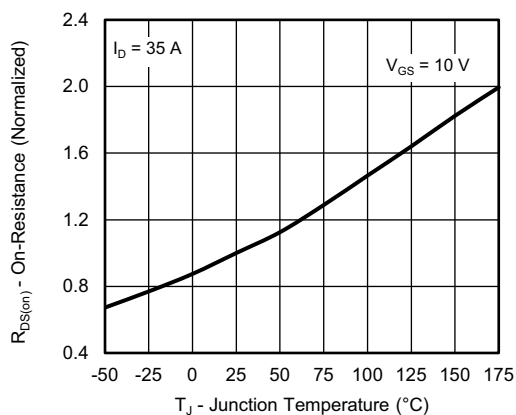
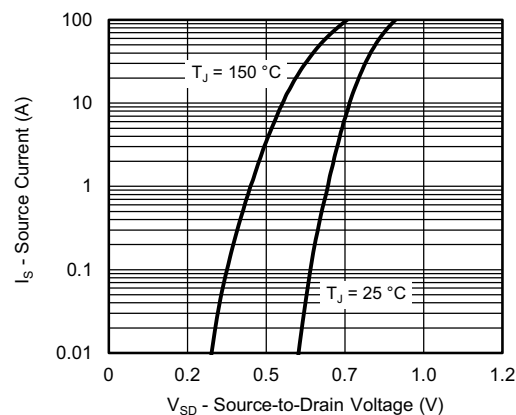
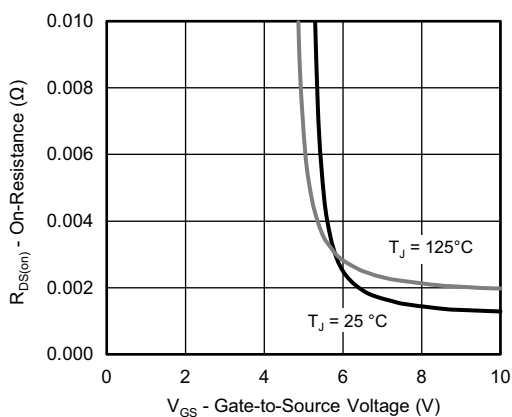
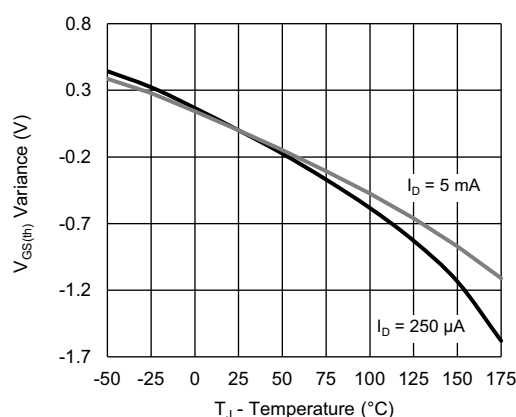
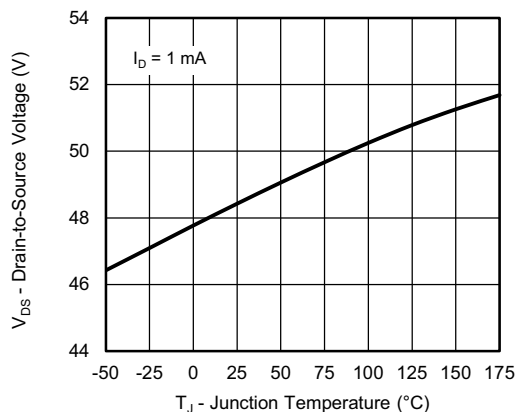
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		40	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.5	3.0	3.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	300	μA
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 35 A	-	0.00133	0.00163	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 35 A, T <sub>J</sub> = 125 °C	-	-	0.00268	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 35 A, T <sub>J</sub> = 175 °C	-	-	0.00326	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 35 A		-	143	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	6783	9200	pF
Output capacitance	C <sub>oss</sub>			-	1771	2400	
Reverse transfer capacitance	C <sub>rss</sub>			-	109	150	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 100 A	-	106	160	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	33	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	21	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		1.25	2.75	4.35	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 0.2 Ω I <sub>D</sub> ≅ 100 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	19	30	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	194	300	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	45	70	
Fall time <sup>c</sup>	t <sub>f</sub>			-	26	40	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	300	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 60 A, V <sub>GS</sub> = 0 V		-	0.83	1.5	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 30 A, di/dt = 100 A/μs		-	88	180	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	186	380	nC
Reverse recovery fall time	t <sub>a</sub>			-	57	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	31	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-4.6	-	A

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

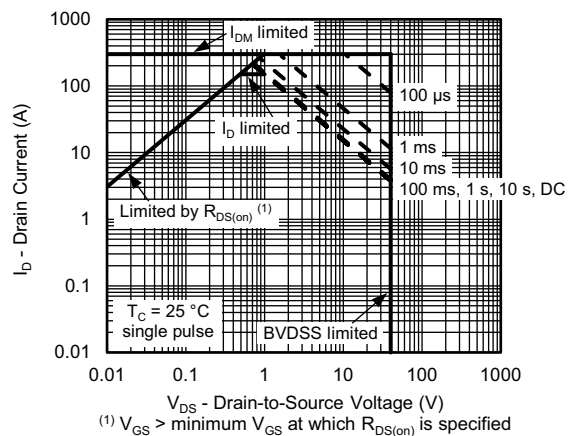
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

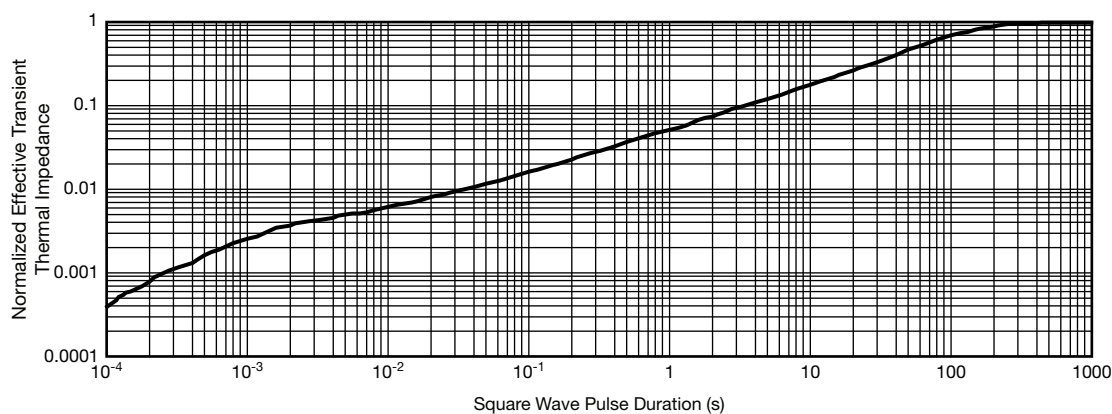
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Drain Source Breakdown vs. Junction Temperature**



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



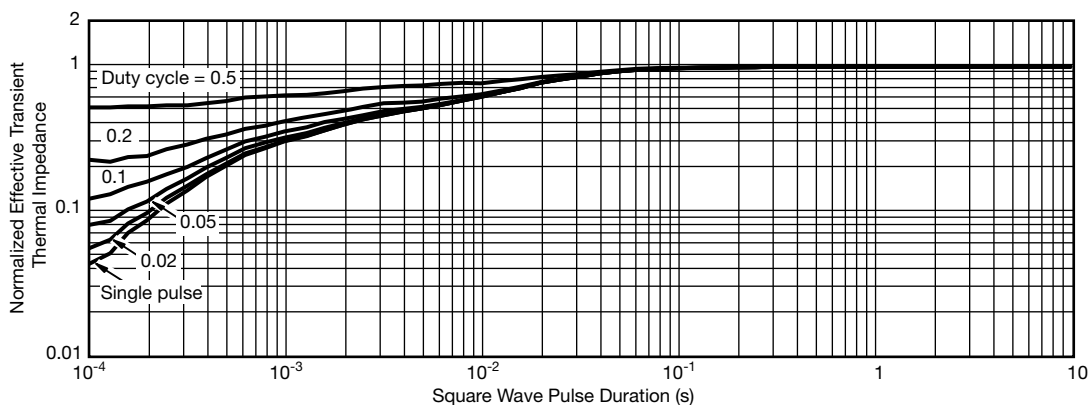
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



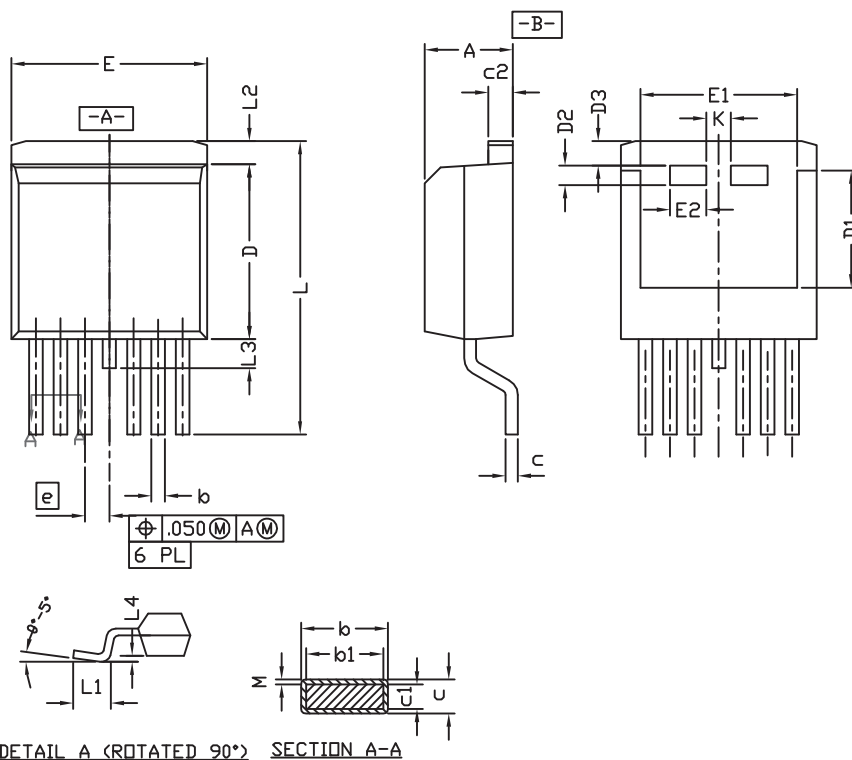
**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions


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## D<sup>2</sup>PAK (TO-263-7L) Case Outline

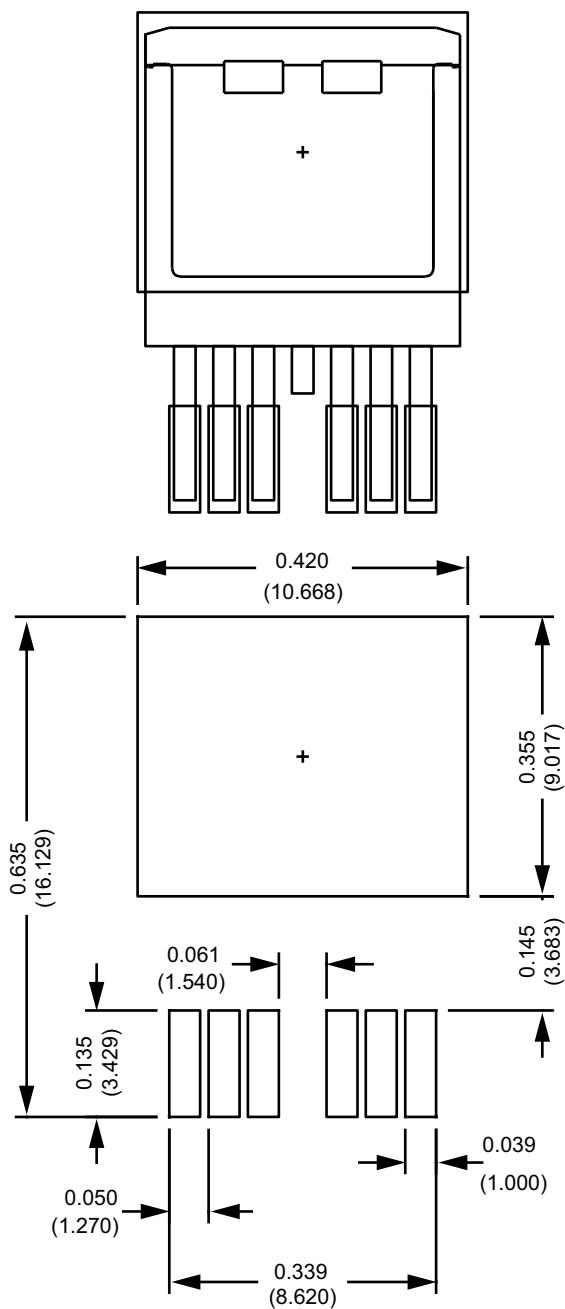


### Notes

1. Plane B includes maximum features of heat sink tab and plastic
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
3. Pin to pin coplanarity max. 4 mils
4. Lead thickness 25 mils
5. For SUM part numbers lead thickness is 24 mils to 29 mils
6. For reference only
7. Use inches as the primary measurement
8. This feature is only for SUM

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.260	0.280	6.604	7.112
D2	0.046	0.050	1.168	1.270
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
	0.050 BSC		1.27 BSC	
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
M	-	0.002	-	0.050
ECN: T22-0410-Rev. D, 19-Sep-2022				
DWG: 6006				

## Recommended Land Pattern D<sup>2</sup>PAK (TO-263-7L)







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