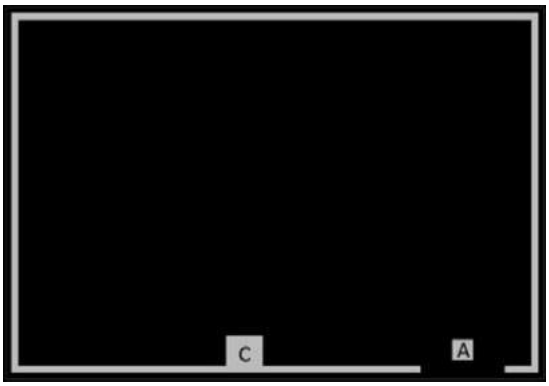
Silicon PIN Photodiode



FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 3.05 x 2.1 x 0.28
- Radiant sensitive area (in mm^2): 5.5
- Peak sensitivity wavelength: 970 nm
- High photo sensitivity
- Suitable for visible light and near infrared radiation
- Fast response times
- Angle of half sensitivity: φ = ± 60°
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

DESCRIPTION

T1112P is a high speed and high sensitive PIN photodiode chip with 5.5 mm^2 sensitive area detecting visible and near infrared radiation. Anode and cathode are the bond pads on top.

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY			
COMPONENT	I_{ra} (µA)	φ (deg)	$\lambda_{0.5}$ (nm)
T1112P	44	± 60	640 to 1070

Note

- Test conditions see table “Basic Characteristics”

ORDERING INFORMATION			
ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T1112P-SD-F	Wafer sawn on foil with disco frame	MOQ: 11 000 pcs	Chip

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	60	V
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	-40 to +100	°C
Storage temperature range		T_{stg1}	-40 to +100	°C
Storage temperature range on foil		T_{stg2}	-40 to +50	°C

For technical questions, contact: optochipsupport@vishay.com

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BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Breakdown voltage	I_R = 100 µA, E = 0	$V_{(BR)}$	60			V
Reverse dark current	V_R = 10 V, E = 0	I_{ro}		0.1	5	nA
Diode capacitance	V_R = 0 V, f = 1 MHz, E = 0	C_D		42		pF
	V_R = 3 V, f = 1 MHz, E = 0	C_D		19		pF
Reverse light current	E_e = 1 mW/cm², λ = 890 nm, V_R = 5 V	I_{ra}		40		µA
	E_e = 1 mW/cm², λ = 950 nm, V_R = 5 V	I_{ra}		44		µA
Angle of half sensitivity		φ		± 60		deg
Wavelength of peak sensitivity		λ_p		970		nm
Range of spectral bandwidth		$\lambda_{0.5}$		640 to 1070		nm
Rise time	V_R = 5 V, R_L = 50 Ω, λ = 870 nm	t_r		130		ns
Fall time		t_f		130		ns
Rise time	V_R = 5 V, R_L = 50 Ω, λ = 950 nm	t_r		7		µs
Fall time		t_f		7		µs

Note

- The measurements are based on samples of die which are mounted on a TO18-header without resin coating

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

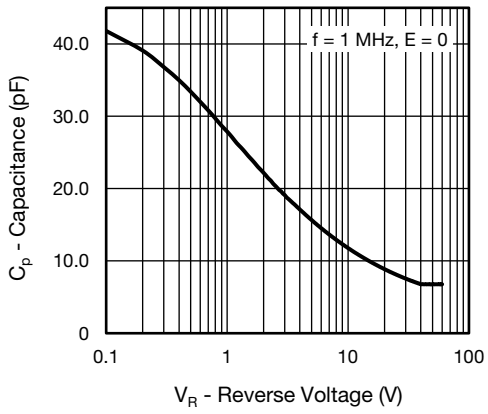


Fig. 1 - Diode Capacitance vs. Reverse Voltage

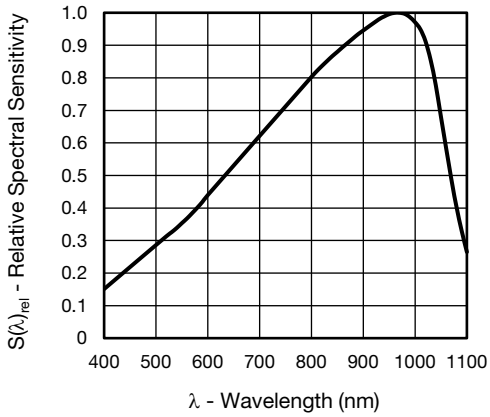
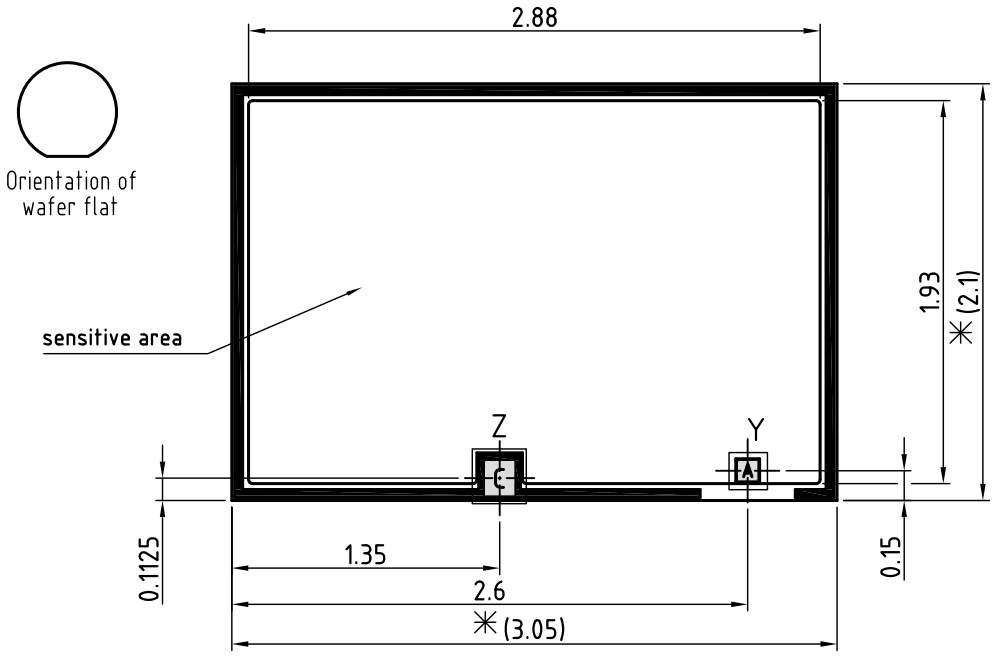


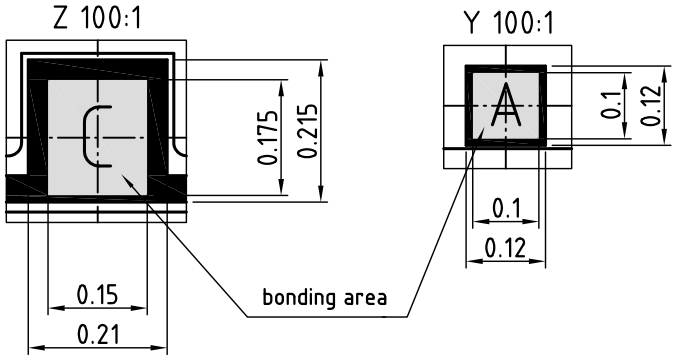
Fig. 2 - Relative Spectral Sensitivity vs. Wavelength without Epoxy Coating

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DIMENSIONS in millimeters



Only for information: Dimension of sawn die under consideration of 30µm saw kerf



technical drawings according to DIN specifications

All dimensions in mm
All dimensions ±0.005
Drawing-No: 9.000-5108.01-4
Issue: 2 / 23.01.2012

A: Anode
C: Cathode

Opt. sensitive area: 5.5mm²

Thickness: 280µm±10µm

Bonding area: A: 100µm x 100µm
C: 150µm x 175µm

Bonding restricted to this area in order to avoid damage of adjacent structures

MECHANICAL DIMENSIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Length of chip edge (x-direction)	L_x		3.05		mm
Length of chip edge (y-direction)	L_y		2.1		mm
Sensitive area	A_S		5.5		mm^2
Wafer diameter	D		150		mm
Die height	H	0.27	0.28	0.29	mm
Bond pad anode			0.1 x 0.1		mm^2
Bond pad cathode			0.15 x 0.175		mm^2

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ADDITIONAL INFORMATION	
Frontside metallization, anode	AlSi
Frontside metallization, cathode	AlSi
Dicing	Sawing
Die bonding technology	Epoxy bonding

Note

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870.
  The visual inspection shall be made in accordance with the “specification of visual inspection as referenced”. The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification.
  The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.

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