Thermal Characteristics of Power Phototriac

INTRODUCTION

Behavior of any semiconductor device depends on the temperature of its die. Hence, electrical parameters are given at a specified temperature. To sustain the performance of a component and to avoid failure or damage caused by overheat, the total power dissipation of the device has to be limited according to the maximum operating temperature.

Vishay VO3526 is a three dice DIP-16 Power Phototriac. Its detailed thermal model was simulated and validated against experimental results. It may help understanding the thermal energy transferring, assisting power dissipation calculation and PCB layout. For a detailed explanation of the thermal model principle, please refer to the Vishay's application note "Thermal Characteristics of Optocouplers".

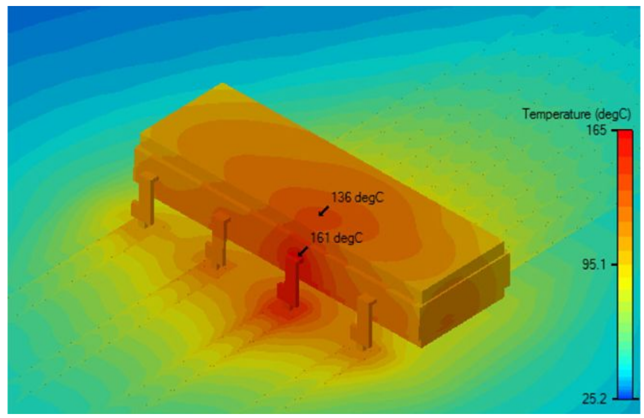

Fig. 1 - Example of Package Temperature Profile (2-Layer Board)

THERMAL ENERGY TRANSFER

There are three mechanisms by which thermal energy (heat) is transported; conduction, radiation, and convection.

- Heat conduction is the transfer of heat from warm areas to cooler ones, and effectively occurs by diffusion.
- Heat radiation (as opposed to particle radiation) is the transfer of internal energy in the form of electromagnetic waves.
- Heat convection is the transfer of heat from a solid surface to a moving liquid or gas.

All three methods occur in phototriac, however in most environments, the majority (~ 70 %) of heat leaving the package exits through the lead frame and into the board. This occurs because the heat transfer from board to ambient is a conductive phenomenon with a much lower thermal resistance (R_{BA}) than the convective and radiative phenomena associated with R_{CA} (case to ambient thermal resistance, typically an order of magnitude larger than other thermal resistances when the device package is small).

This is shown graphically by the package temperature profile and strong heat flux contours evident in the die, lead frame, and board in figures 1 (2-layer board, higher R_{BA}), and 2 (4-layer board, lower R_{BA}). R_{BA} is the thermal resistance from the board to the ambient, and is primarily driven by the geometry and composition of the board. The type of board design used defines this characteristic.

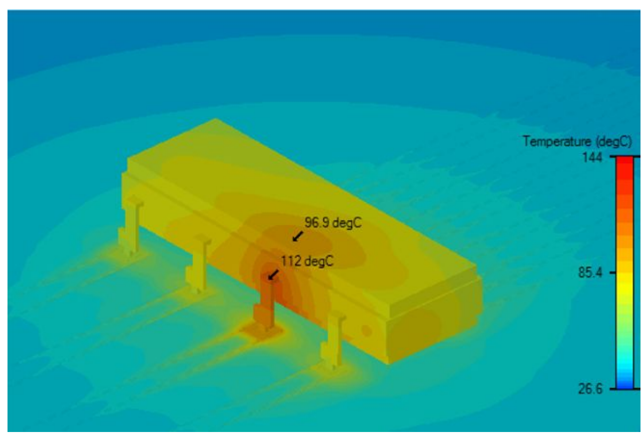

Fig. 2 - Example of Package Temperature Profile (4-Layer Board)

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POWER PHOTOTRIAC THERMAL MODEL

Vishay power phototriac VO3526 is a device with three dice, emitter, opto-triac and non-opto-triac (power triac). Its resistor network was derived from the experimental and validated model results and is outlined below.

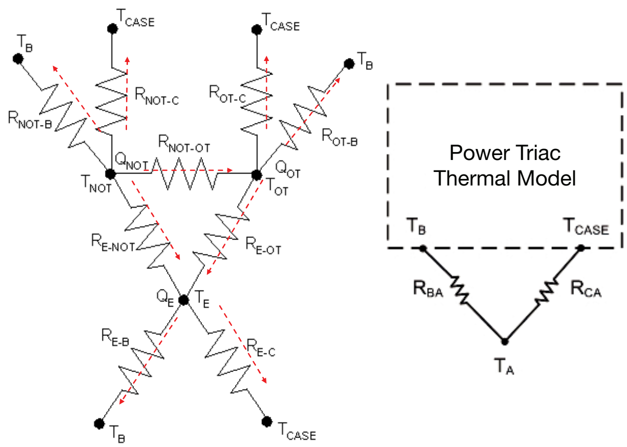

Fig. 3 - Three Dice Power Phototriac Thermal Model/Resistor Network

Where:

E:	Emitter
OT:	Opto-Triac
NOT:	Non-Opto-Triac
R_{EB}:	Thermal resistance, emitter die to board
R_{OTB}:	Thermal resistance, OT die to board
R_{NOTB}:	Thermal resistance, NOT die to board
R_{EOT}:	Thermal resistance, emitter die to OT die
R_{ENOT}:	Thermal resistance, emitter die to NOT die
R_{NOTOT}:	Thermal resistance, NOT die to OT die
R_{EC}:	Thermal resistance, emitter die to case
R_{OTC}:	Thermal resistance, OT die to case
R_{NOTC}:	Thermal resistance, NOT die to case
R_{BA}:	Thermal resistance, board to ambient
R_{CA}:	Thermal resistance, case to ambient
T_E:	Emitter junction temperature
T_{OT}:	OT junction temperature
T_{NOT}:	NOT junction temperature
T_C:	Case temperature (top center)
T_B:	Board temperature
T_A:	Ambient temperature
Q_E:	Power dissipation on emitter
Q_{OT}:	Power dissipation on OT
Q_{NOT}:	Power dissipation on NOT

In order to write equation to calculate the node temperatures, some heat flow directions are assumed and shown on figure 3. Based on Figure 3, the following equations in table 1 are created for calculating the node temperatures.

TABLE 1 - NODAL EQUATIONS (for reference)	
1	$Q_{NOTOT} + Q_{NOTE} + Q_{NOTB} + Q_{NOTC} = Q_{NOT}$
2	$Q_{OTE} - Q_{NOTOT} + Q_{OTB} + Q_{OTC} = Q_{OT}$
3	$-Q_{NOTE} - Q_{OTE} + Q_{EB} + Q_{EC} = Q_E$
4	$T_{NOT} - T_{OT} - R_{NOTOT}Q_{NOTOT} = 0$
5	$T_{NOT} - T_E - R_{NOTE}Q_{NOTE} = 0$
6	$T_{NOT} - T_B - R_{NOTB}Q_{NOTB} = 0$
7	$T_{NOT} - T_C - R_{NOTC}Q_{NOTC} = 0$
8	$T_{OT} - T_B - R_{OTB}Q_{OTB} = 0$
9	$T_{OT} - T_C - R_{OTC}Q_{OTC} = 0$
10	$T_{OT} - T_E - R_{OTE}Q_{OTE} = 0$
11	$T_E - T_B - R_{EB}Q_{EB} = 0$
12	$T_E - T_C - R_{EC}Q_{EC} = 0$
13	$T_B - R_{BA} (Q_{NOTB} + Q_{OTB} + Q_{EB}) = T_A$
14	$T_C - R_{CA} (Q_{NOTC} + Q_{OTC} + Q_{EC}) = T_A$

Assuming the power dissipated from the triacs (Q_{NOT} and Q_{OT}) and the emitter (Q_E), the temperatures of board (T_B), case (T_C) and ambient (T_A), are known (by measuring or estimated), the node temperatures can be calculated by EXCEL Tools/Solver or solving the network equations using matrix calculation.

$$\mathbf{A \times X = B}$$

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THERMAL ANALYSIS EXAMPLE

It is important to note that regardless of the package size and type, the thermal analysis will need to be done to insure a solid design. Exceeding the thermal parameters can have detrimental and sometimes even disastrous consequences.

Following is a thermal analysis example of Vishay power phototriac VO3526. Its thermal resistances are provided in its datasheet as table 2.

TABLE 2 - THERMAL RESISTANCE FOR VO3526 POWER PHOTOTRIAC (°C/W)	
R_{EB}	149
R_{OTB}	158
R_{NOTB}	75
R_{EOT}	235
R_{NOTE}	420
R_{NOTOT}	243
R_{EC}	161
R_{OTC}	157
R_{NOTC}	150

To predict the operating temperatures outside of a modeling environment use the derived resistor network values with appropriate Case-to-Ambient and Board-to-Ambient thermal resistances as shown in table 3.

TABLE 3 - THERMAL RESISTANCE OF CASE TO AMBIENT AND BOARD TO AMBIENT

RESISTANCE	BOARD TYPE	DERIVED RESISTANCE (°C/W)
R_{CA} (Case-Ambient)	2S2P	130
	2S0P	
R_{BA} (Board-Ambient)	2S2P	30
	2S0P	90

It is important to note that the R_{BA} is dependent upon the material, number of layers, and thickness of the board used. In our analysis, the phototriacs were mounted on 2 and 4 layer boards with thickness of 4 mm. Obviously, the R_{BA} of the 4-layer board (2S2P) is much less than the 2-layer board (2S0P).

Using equations 1 to 14, the thermal resistances shown in table 2 and 3, and assuming emitter and detectors power dissipation shown in table 4, the node temperatures when T_A is known are calculated to be as shown in table 5.

Obviously, the majority of heat leaving the package exits through the lead frame and into the board (Q_{NOTB}), so that the junction temperatures (T_{NOT}, T_{OT}, T_E) when the module is mounted on the 4-layer board (2S2P) are much lower than that when on the 2-layer board (2S0P).

TABLE 4 - INPUT VALUES

Q_E		0.028	W
Q_{OT}		0.018	W
Q_{NOT}		1.25	W
T_A		25	°C
R_{BA}	2-layer board	90	°C/W
	4-layer board	30	°C/W
R_{CA}		130	°C/W

TABLE 5 - CALCULATED NODE TEMPERATURE AND POWER (T_A = 25 °C)

CALCULATED VALUES	2-LAYER BOARD	4-LAYER BOARD
T_B (°C)	95.3	54.0
T_C (°C)	92.0	67.7
T_E (°C)	**104.0**	**70.7**
T_{OT} (°C)	**106.4**	**73.1**
T_{NOT} (°C)	**144.1**	**109.1**
Q_{NOTOT} (W)	0.1551	0.1480
Q_{NOTE} (W)	0.0955	0.0915
Q_{OTE} (W)	0.010	0.011
Q_{NOTB} (W)	0.651	0.735
Q_{OTB} (W)	0.071	0.121
Q_{EB} (W)	0.059	0.112
Q_{NOTC} (W)	0.35	0.28
Q_{OTC} (W)	0.09	0.03
Q_{EC} (W)	0.075	0.0183