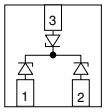
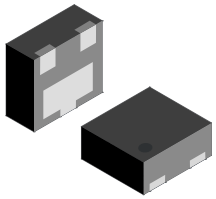
2-Line Low Capacitance, Bidirectional and Symmetrical (BiSy) ESD Protection Diode





DFN1110-3A

FEATURES

- Small DFN1110-3A
- 2-line ESD protection
- Working range ± 5.5 V
- Low leakage current I_R < 0.05 µA
- Low load capacitance C_D < 0.45 pF
- ESD immunity acc. IEC 61000-4-2
  ± 20 kV contact discharge
  ± 20 kV air discharge
- ESD capability according to AEC-Q101: human body model: class H3B: > 8 kV
- e3 - pins side wall plated with tin (Sn)
- AOI capable
- AEC-Q101 qualified available
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE Available

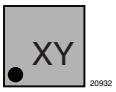
Pb-free

e3

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

MARKING (example only)



Dot = pin marking
X = date code
Y = type code (see table below)

LINKS TO ADDITIONAL RESOURCES

3D Models | SPICE Models | Application Notes

ORDERING INFORMATION

PART NUMBER (EXAMPLE)	ENVIRONMENTAL AND QUALITY CODE			PACKAGING CODE	ORDERING CODE (EXAMPLE)
	AEC-Q101 QUALIFIED	RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS GREEN	TIN PLATED	10K PER 7" REEL (8 mm TAPE) 10K/BOX = MOQ	
VBUS05M2-HT5	-	G	3	-08	VBUS05M2-HT5-G3-08
VBUS05M2-HT5	H	G	3	-08	VBUS05M2-HT5HG3-08

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS05M2-HT5	DFN1110-3A	M	1.43 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	I_{PPM}	3.4	A
Peak pulse power	Acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	P_{PP}	60	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 20	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 20	
Operating temperature	Junction temperature	T_J	-55 to +150	°C
Storage temperature		T_{STG}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (pin 1 or pin 2 to pin 3; in both directions) (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	2	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5.5	V
Reverse voltage	At I_R = 0.1 µA	V_R	5.5	-	-	V
Reverse current	At V_{RWM} = 5.5 V	I_R	-	< 0.001	0.1	µA
Reverse breakdown voltage	At I_R = 1 mA	V_{BR}	7.5	8.5	9.5	V
Reverse clamping voltage	At I_{PP} = 1 A	V_C	-	11	13	V
	At $I_{PP} = I_{PPM}$ = 3.4 A	V_C	-	15	18	V
Clamping voltage	Transmission line pulse (TLP), t_p = 100 ns I_{TLP} = 8 A	$V_{C\text{-}TLP}$	-	20	-	V
	Transmission line pulse (TLP), t_p = 100 ns I_{TLP} = 16 A	$V_{C\text{-}TLP}$	-	27	-	V
Dynamic resistance	Transmission line pulse (TLP), t_p = 100 ns	R_{DYN}	-	1	-	Ω
Capacitance	At V_R = 0 V; f = 1 MHz	C_D	-	0.37	0.45	pF
	At V_R = 3.3 V; f = 1 MHz		-	0.37	0.45	pF

APPLICATION NOTE

The VBUS05M2-HT5 is a two-line ESD protection device with a bidirectional and symmetrical (BiSy) breakdown and clamping performance made for application with a voltage working range up to ± 5.5 V. The high ESD immunity and a very low capacitance makes it usable for high frequency applications like USB2.0, USB3.0, or HDMI.

With the VBUS05M2-HT5 two high speed data lines can be protected against transient voltage signals like ESD (electro static discharge). Connected to the data line (pin 1 and pin 2) and to ground (pin 3) negative transients will be clamped close above the 5.5 V working range.

SCHEMATIC DIAGRAM

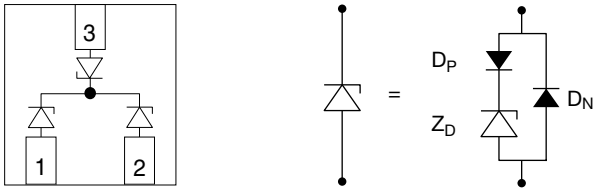


Fig. A

The simplified schematic diagram in Fig. A shows three identical Z-diodes with the cathode on pin 1, 2, or 3 and common anodes. In reality each Z-diode consist of one Z-diode for the adjustment of the breakdown voltage, and two low capacitance switching diodes which provide the low capacitance. Positive transients will be clamped through the switching diode D_P and the Z-diode Z_D while negative transients will be clamped through the switching diode D_N.

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

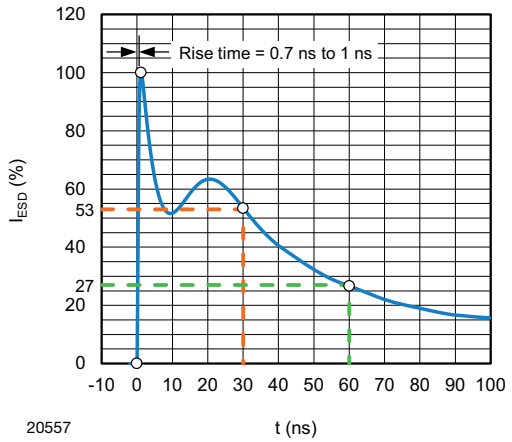


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

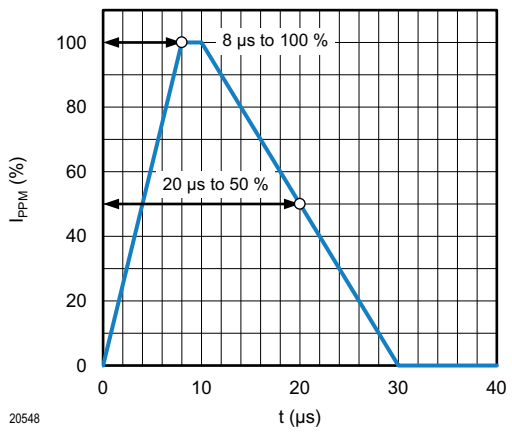


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

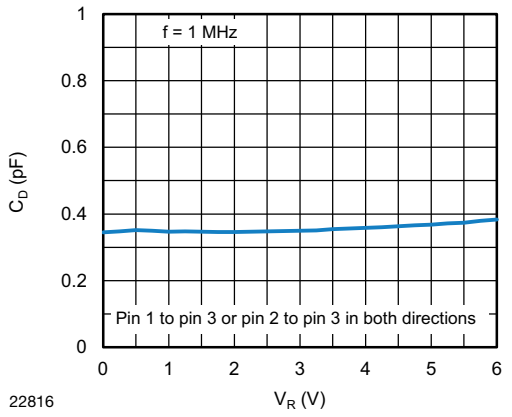


Fig. 3 - Typical Capacitance vs. Reverse Voltage

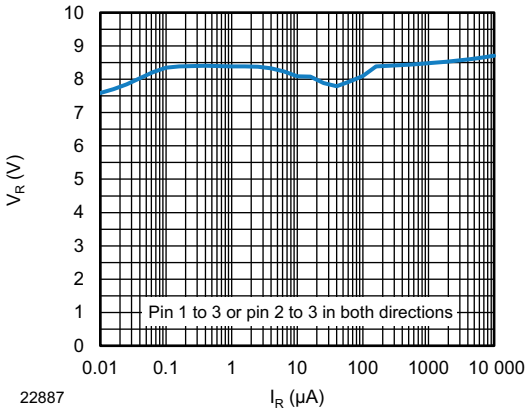


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

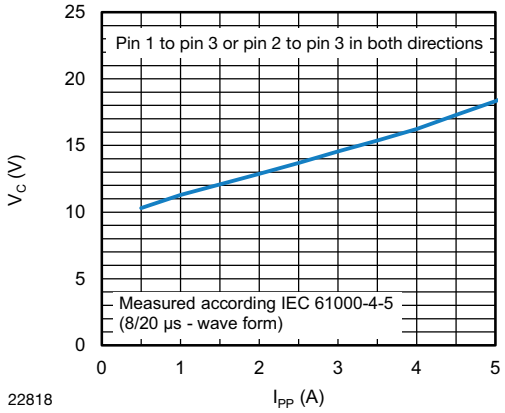


Fig. 5 - Typical Peak Clamping Voltage vs. Peak Pulse Current

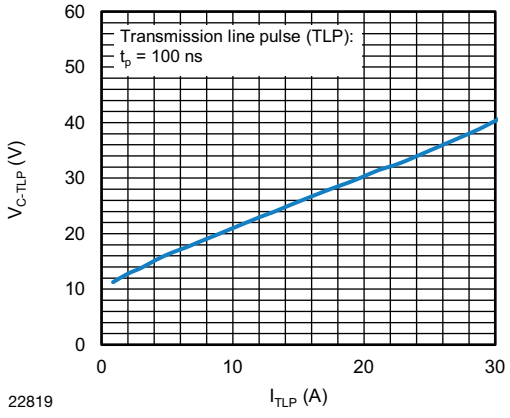
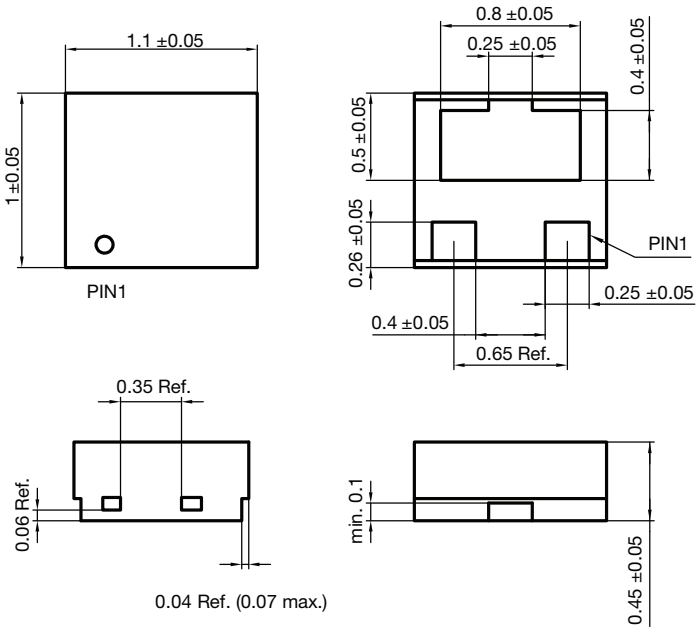
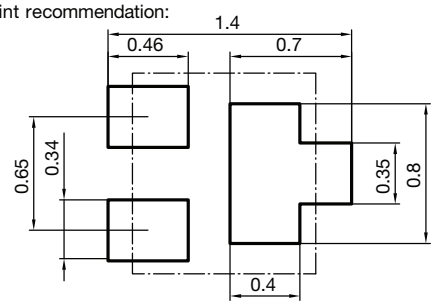


Fig. 6 - Typical Peak Forward Voltage vs. Forward Current

PACKAGE DIMENSIONS in millimeters (inches)

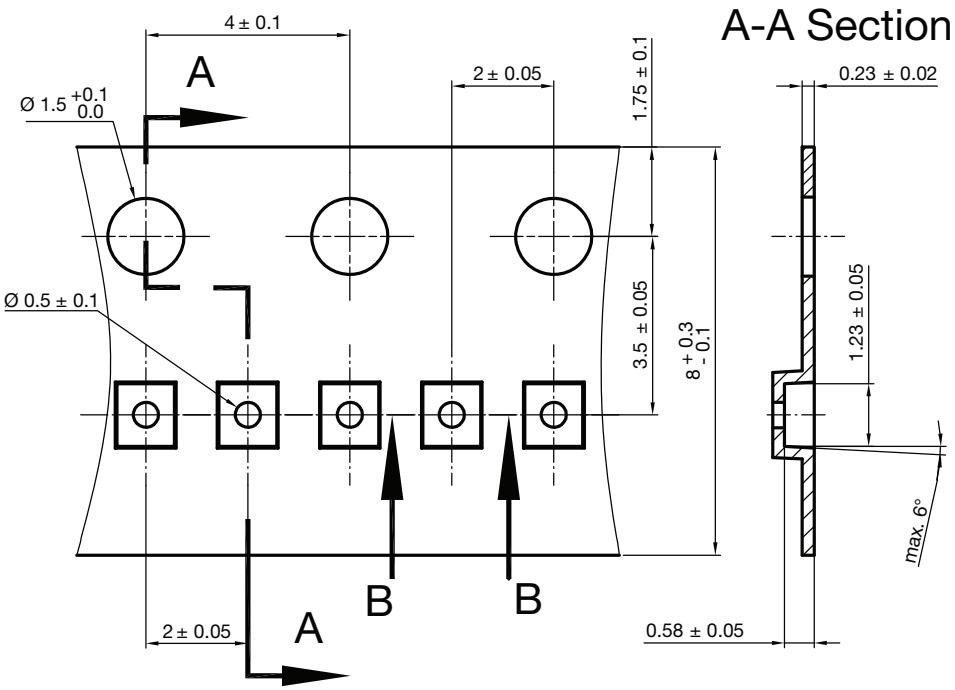


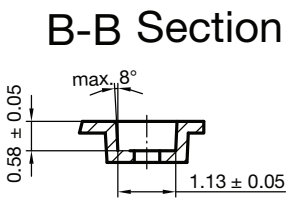
foot print recommendation:



Document no.: S8-V-3906.04-062 (4)
Package name: DFN1110-3A
Created - Date: 04-Apr-2019

CARRIER TAPE DFN1110-3A

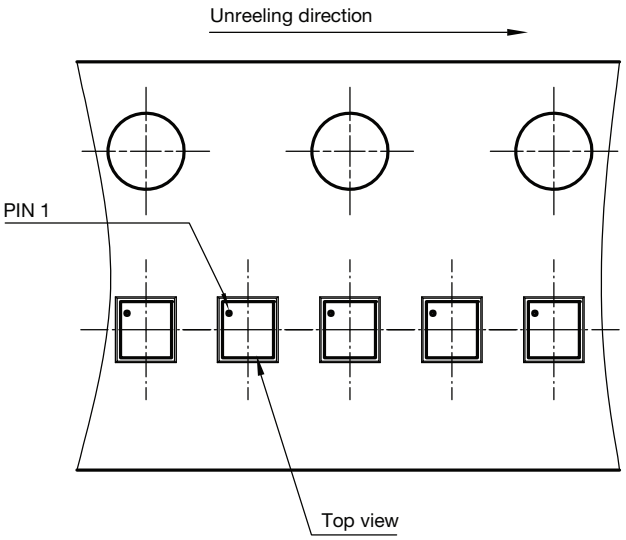




Document no: S8-V-3906.04-065 (4)
Package name: DFN1110-3A
Created date: 28.10.2019

surface resistance: 10^5 - 10^{11} $\frac{OHMS}{SQ}$
Cummulative tolerances of 10 sprocket holes is ± 0.2 mm

ORIENTATION IN CARRIER TAPE DFN1110-3A



Document no: S8-V-3906.04-066 (4)
Package name: DFN1110-3A
Created date: 28.10.2019

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