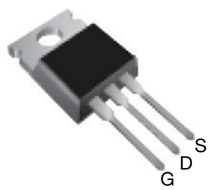
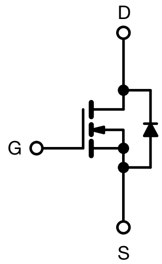
# Power MOSFET

TO-220AB




N-Channel MOSFET

## FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V $V_{GS}$ rating
- Reduced $C_{iss}$, $C_{oss}$, $C_{rss}$
- Extremely high frequency operation
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available
RoHS* Available

**Note**

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 500 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.85 |
| $Q_g$ max. (nC) | 39 | |
| $Q_{gs}$ (nC) | 10 | |
| $Q_{gd}$ (nC) | 19 | |
| Configuration | Single | |

## DESCRIPTION

This new series of low charge power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

| ORDERING INFORMATION | |
|---|---|
| Package | TO-220AB |
| Lead (Pb)-free | IRF840LCPbF |
| Lead (Pb)-free and halogen-free | IRF840LCPbF-BE3 |

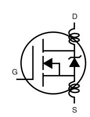
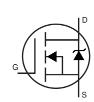
**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DS}$ | 500 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 30 | V |
| Continuous drain current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 8.0 | A |
| | | $T_C$ = 100 °C | | 5.1 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 28 | |
| Linear derating factor | | | | 1.0 | W/°C |
| Single pulse avalanche energy [b] | | | $E_{AS}$ | 510 | mJ |
| Repetitive avalanche current [a] | | | $I_{AR}$ | 8.0 | A |
| Repetitive avalanche energy [a] | | | $E_{AR}$ | 13 | mJ |
| Maximum power dissipation | $T_C$ = 25 °C | | $P_D$ | 125 | W |
| Peak diode recovery dV/dt [c] | | | dV/dt | 3.5 | V/ns |
| Operating junction and storage temperature range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering recommendations (peak temperature) [d] | For 10 s | | | 300 | |
| Mounting torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 14 mH, $R_g$ = 25 Ω, $I_{AS}$ = 8.0 A (see fig. 12)
c. $I_{SD} \leq$ 8.0 A, dI/dt $\leq$ 100 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C
d. 1.6 mm from case

| **THERMAL RESISTANCE RATINGS** | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum junction-to-ambient | $R_{thJA}$ | - | 62 | °C/W |
| Case-to-sink, flat, greased surface | $R_{thCS}$ | 0.50 | - | |
| Maximum junction-to-case (drain) | $R_{thJC}$ | - | 1.0 | |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 500 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.63 | - | V/°C |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | | 2.0 | - | 4.0 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | | - | - | ± 100 | nA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | | - | - | 25 | μA |
| | | $V_{DS}$ = 400V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 250 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 4.8 A [b] | - | - | 0.85 | Ω |
| Forward transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 4.8 A [b] | | 4.0 | - | - | S |
| **Dynamic** | | | | | | | |
| Drain-source breakdown voltage | $C_{iss}$ | $V_{GS}$ = 0 V,<br>$V_{DS}$ = 25 V,<br>f = 1.0 MHz, see fig. 5 | | - | 1100 | - | pF |
| $V_{DS}$ temperature coefficient | $C_{oss}$ | | | - | 170 | - | |
| Gate-source threshold voltage | $C_{rss}$ | | | - | 18 | - | |
| Gate-source leakage | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 8.0 A, $V_{DS}$ = 400 V<br>see fig. 6 and 13 [b] | - | - | 39 | nC |
| Zero gate voltage drain current | $Q_{gs}$ | | | - | - | 10 | |
| | $Q_{gd}$ | | | - | - | 19 | |
| Drain-source on-state resistance | $t_{d(on)}$ | $V_{DD}$ = 250 V, $I_D$ = 8.0 A,<br>$R_g$ = 9.1 Ω, $R_D$= 30 Ω<br>see fig. 10 [b] | | - | 12 | - | ns |
| Forward transconductance | $t_r$ | | | - | 25 | - | |
| Drain-source breakdown voltage | $t_{d(off)}$ | | | - | 27 | - | |
| $V_{DS}$ temperature coefficient | $t_f$ | | | - | 19 | - | |
| Gate input resistance | $R_g$ | f = 1 MHz, open drain | | 0.7 | - | 3.7 | Ω |
| Internal drain inductance | $L_D$ | Between lead,<br>6 mm (0.25") from<br>package and center of<br>die contact |  | - | 4.5 | - | nH |
| Internal source inductance | $L_S$ | | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous source-drain diode current | $I_S$ | MOSFET symbol<br>showing the<br>integral reverse<br>p - n junction diode |  | - | - | 8.0 | A |
| Pulsed diode forward current [a] | $I_{SM}$ | | | - | - | 28 | |
| Body diode voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 8.0 A, $V_{GS}$ = 0 V [b] | | - | - | 2.0 | V |
| Body diode reverse recovery time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 8.0 A,<br>dI/dt = 100 A/μs [b] | | - | 490 | 740 | ns |
| Body diode reverse recovery charge | $Q_{rr}$ | | | - | 3.0 | 4.5 | μC |
| Forward turn-on time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

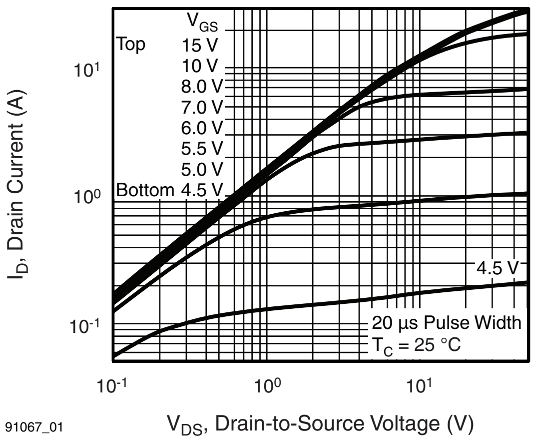



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

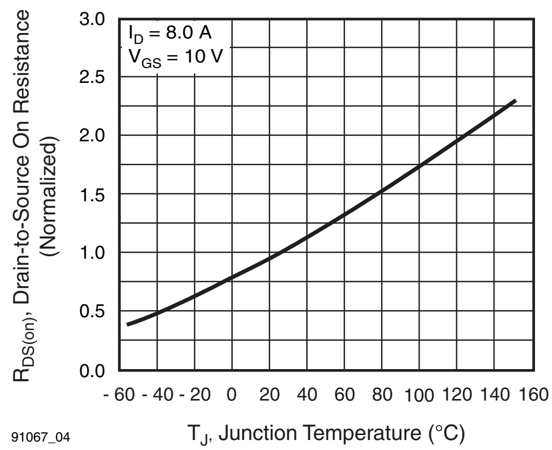



**Fig. 4 - Normalized On-Resistance vs. Temperature**

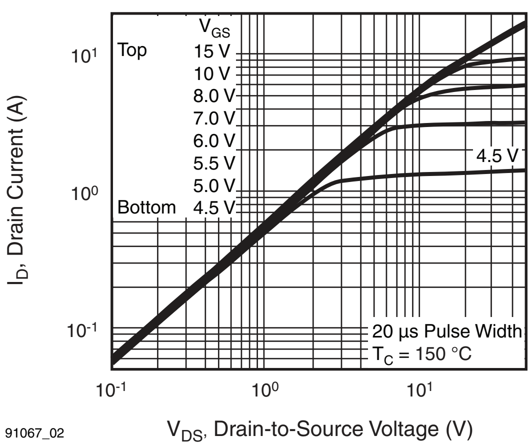



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

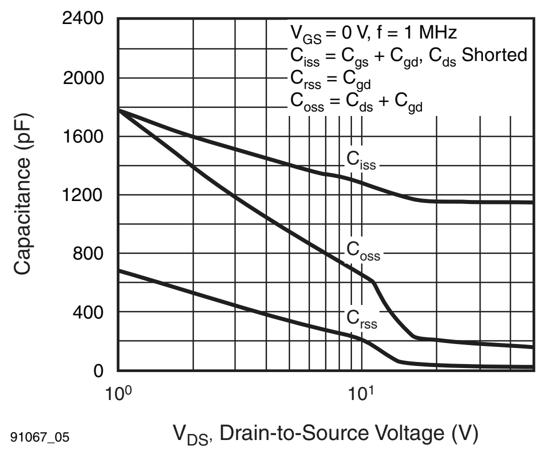



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

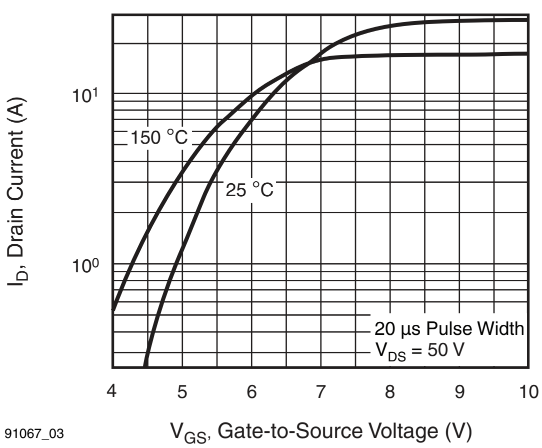



**Fig. 3 - Typical Transfer Characteristics**

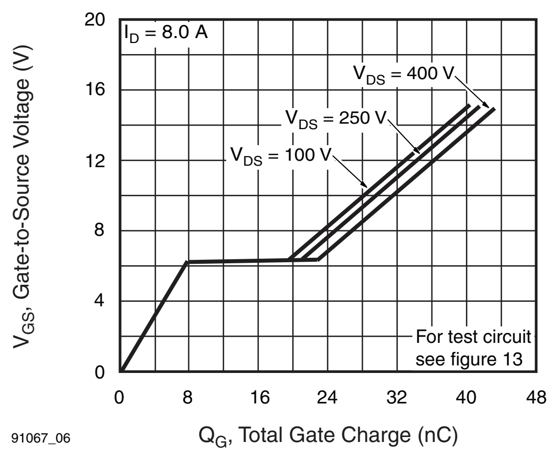



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

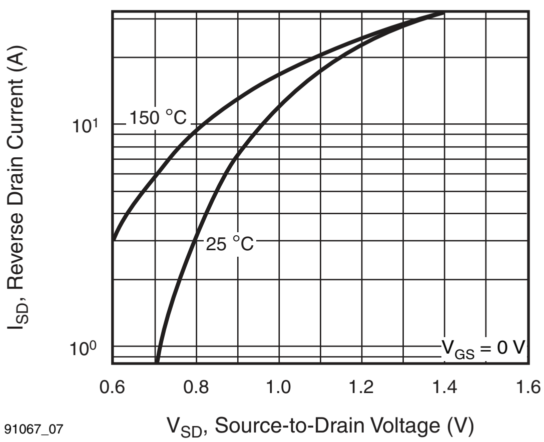



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

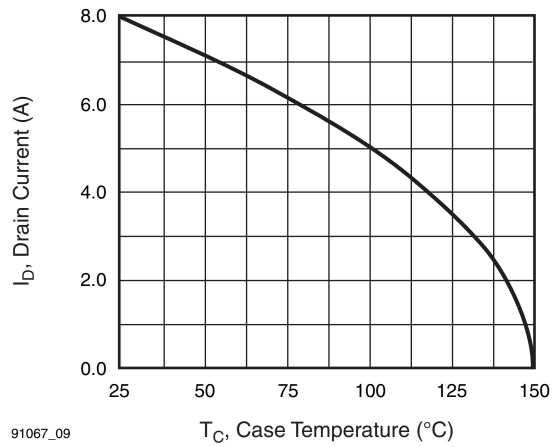



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

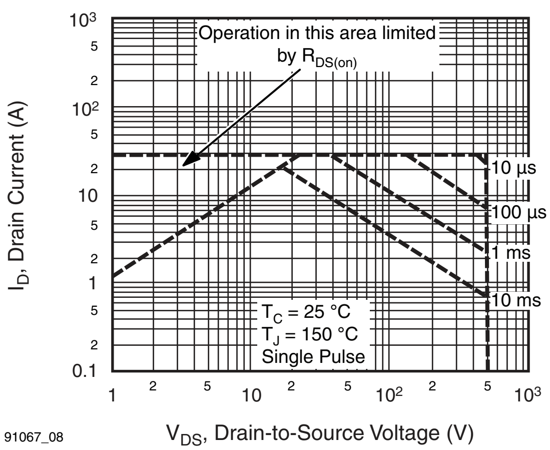



**Fig. 8 - Maximum Safe Operating Area**

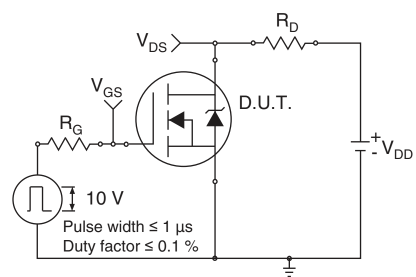



**Fig. 10a - Switching Time Test Circuit**

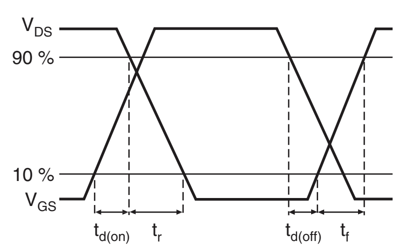



**Fig. 10b - Switching Time Waveforms**

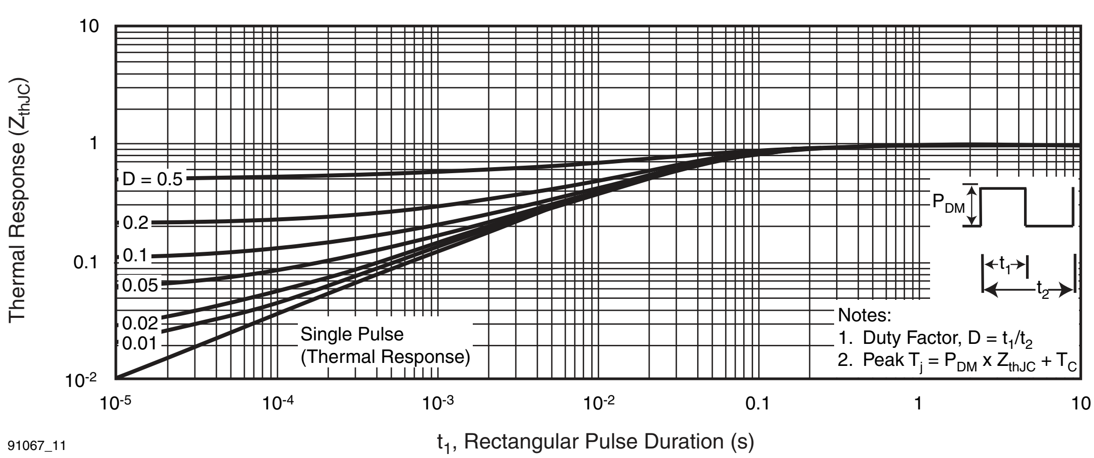



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

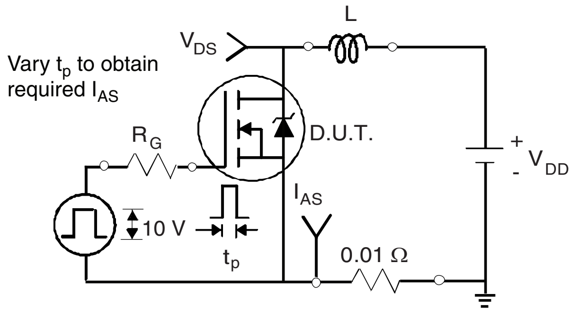



**Fig. 12a - Unclamped Inductive Test Circuit**

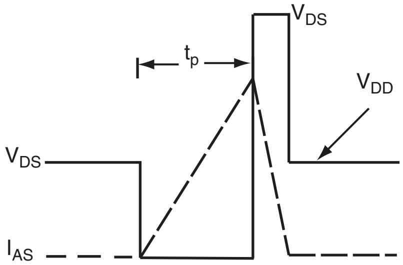



**Fig. 12b - Unclamped Inductive Waveforms**

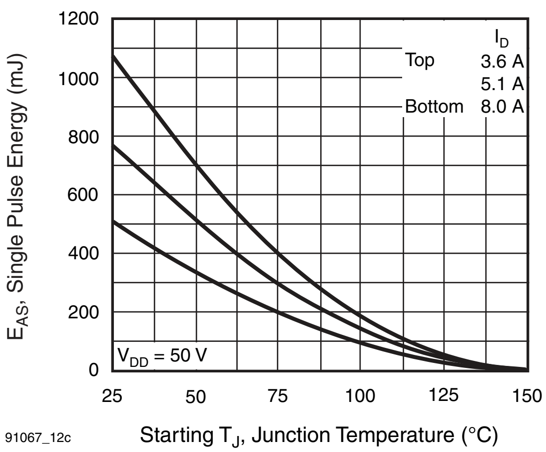



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

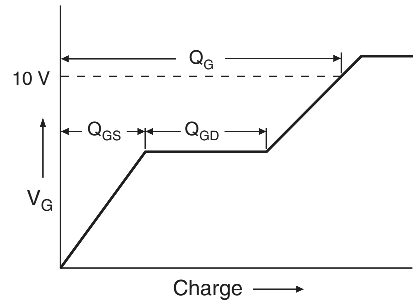



**Fig. 13a - Basic Gate Charge Waveform**

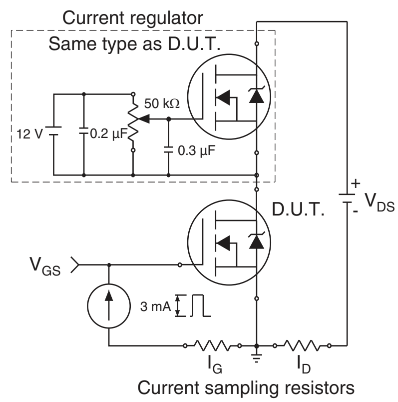
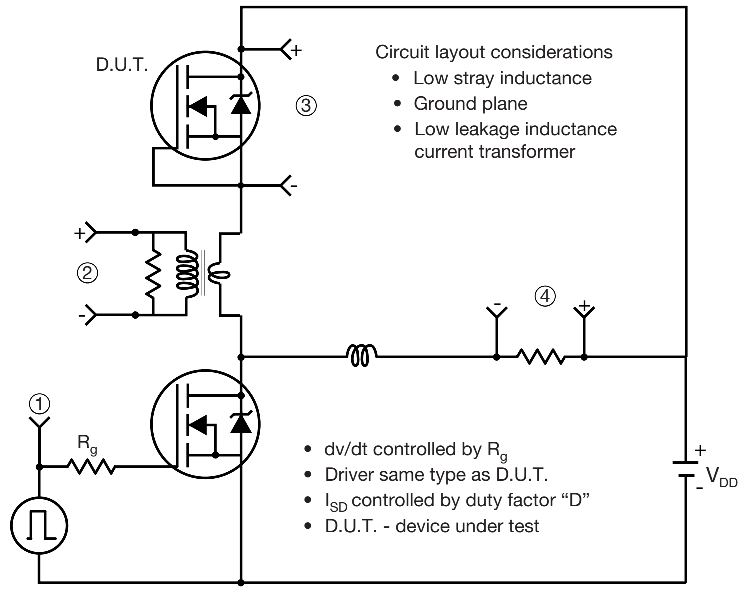
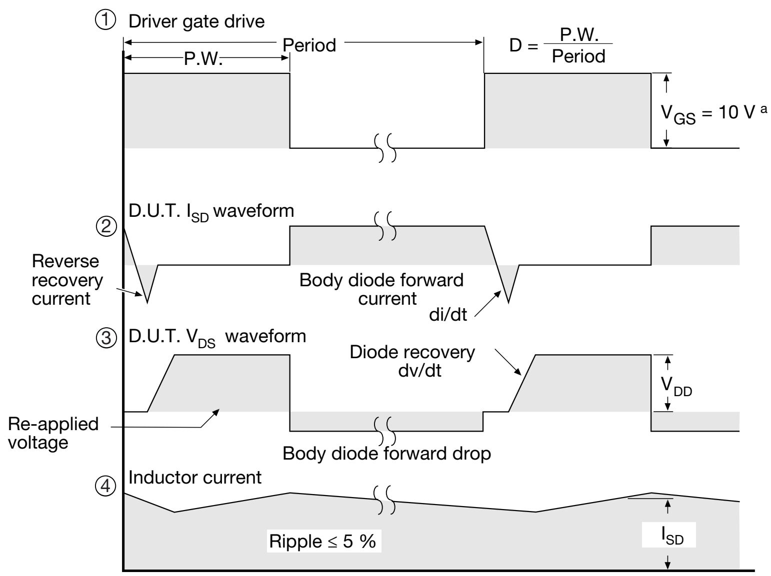



**Fig. 13b - Gate Charge Test Circuit**

**Peak Diode Recovery dv/dt Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

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