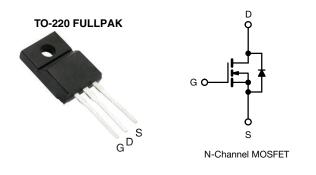




Power MOSFET



PRODUCT SUMMA	RY	
V _{DS} (V)	800)
R _{DS(on)} (Ω)	$V_{GS} = 10 V$	6.5
Q _g (Max.) (nC)	38	
Q _{gs} (nC)	5.0	
Q _{gd} (nC)	21	
Configuration	Sing	le

FEATURES

- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- Dynamic dV/dt rating
- · Low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

Third generation power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIBE20GPbF

ABSOLUTE MAXIMUM RATINGS T_C =	= 25 °C, unle	ess otherwis	e noted			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	800	v	
Gate-source voltage		V _{GS}	± 20			
Continuous drain current	V _{GS} at 10 V	$T_C = 25 \text{ °C}$ $T_C = 100 \text{ °C}$	1_	1.4		
	VGS at 10 V	T _C = 100 °C	ID	0.86	А	
Pulsed drain current ^a			I _{DM}	5.6		
Linear derating factor				0.24	W/°C	
Single pulse avalanche energy ^b			E _{AS}	180	mJ	
Repetitive avalanche current ^a			I _{AR}	1.4	А	
Repetitive avalanche energy ^a			E _{AR}	3.0	mJ	
Maximum power dissipation $T_{\rm C} = 25 ^{\circ}{\rm C}$		25 °C	P _D	30	W	
k diode recovery dV/dt ^c dV/dt 2.0		V/ns				
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	0 °C	
Soldering recommendations (peak temperature) ^d	For	10 s		300		
Mounting torque	M3 s	screw		0.6	Nm	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 172 mH, R_G = 25 Ω , I_{AS} = 1.4 A (see fig. 12)

c. $I_{SD} \leq 1.8$ A, dI/dt ≤ 80 A/µs, $V_{DD} \leq 600, \, T_J \leq 150 \ ^\circ C$

d. 1.6 mm from case

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COMPLIANT

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PABAMETER	NGS SYMBOL	TVD	\	MAX.			UNIT	
		TYP	•				UNIT	
Maximum junction-to-ambient	R _{thJA}	- 65				°C/W		
Maximum junction-to-case (drain)	R _{thJC}	- 4.1						
SPECIFICATIONS T _J = 25 °C, u	nless otherwi	se noted						
PARAMETER	SYMBOL	TES		ONS	MIN.	TYP.	MAX.	UNIT
Static		•						
Drain-ssource breakdown voltage	V _{DS}	V _{GS} :	= 0 V, I _D = 2	50 µA	800	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C,	I _D = 1 mA	-	0.98	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 2	250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}		$V_{GS} = \pm 20^{\circ}$	V	-	-	± 100	nA
		V _{DS} =	= 800 V, V _{GS}	s = 0 V	-	-	100	μA
Zero gate voltage drain current	I _{DSS}	-		, T _J = 125 °C	-	-	500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D =	= 0.84 A ^b	-	-	6.5	Ω
Forward transconductance	9 _{fs}	V _{DS} =	10 V, I _D = 0	.84 A ^b	1.0	-	-	S
Dynamic								1
Input capacitance	C _{iss}		<u> </u>		-	530	-	
Output capacitance	Coss		V _{GS} = 0 V, V _{DS} = 25 V,		-	150	-	- pF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see fig. 5 f = 1.0 MHz		fig. 5	-	90	-	
Drain to sink capacitance	С			Z	-	12	-	
Total gate charge	Qg				-	-	38	
Gate-source charge	Q _{gs}	V _{GS} = 10 V		A, V _{DS} = 400 V, J. 6 and 13 ^b	-	-	5.0	nC
Gate-drain charge	Q _{gd}		See ng	J. O and 15	-	-	21	
Turn-on delay time	t _{d(on)}				-	8.2	-	
Rise time	t _r	$\label{eq:VDD} \begin{array}{l} V_{DD} = 400 \ V, \ I_D = 1.8 \ A, \\ R_G = 18 \ \Omega, \ R_D = 230 \ \Omega, \\ \text{see fig. 10} \ ^{b} \end{array}$		-	17	-	- ns	
Turn-off delay time	t _{d(off)}			-	58	-		
Fall time	t _f			-	27	-		
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-		
Internal source inductance	L _S			-	7.5	-	nH	
Drain-Source Body Diode Characteristi	cs	•				•		
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	1.4	A	
Pulsed diode forward current ^a	I _{SM}			-	-	5.6		
Body diode voltage	V_{SD}	T _J = 25 °C	, I _S = 1.4 A,	V_{GS} = 0 V ^b	-	-	1.4	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 1.8 A, dl/dt = 100 A/μs ^b		dt - 100 A (up b	-	380	570	ns
Body diode reverse recovery charge	Q _{rr}	$I_{\rm J} = 20$ 0, I _F	– 1.0 A, Ul/	$a_1 = 100 Av \mu s^{-5}$	-	0.94	1.4	μC
Forward turn-on time	t _{on}	Intrinsic tu	ırn-on time	is negligible (turn	-on is dor	ninated b	y L _S and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

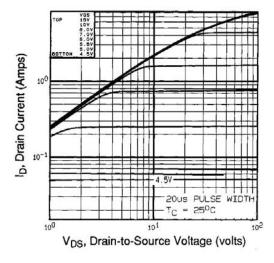
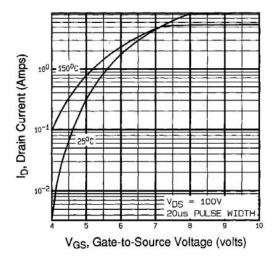


Fig. 1 - Typical Output Characteristics, $T_C = 25 \ ^{\circ}C$





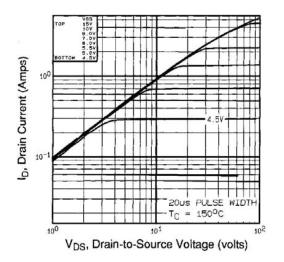


Fig. 2 - Typical Output Characteristics, $T_C = 150 \ ^\circ C$

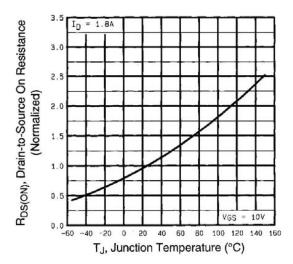


Fig. 4 - Normalized On-Resistance vs. Temperature



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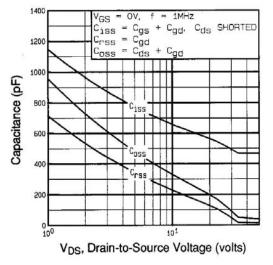


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

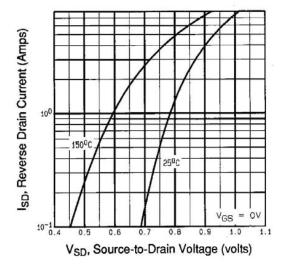


Fig. 7 - Typical Source-Drain Diode Forward Voltage

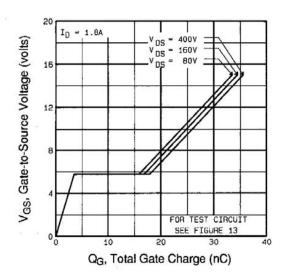


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

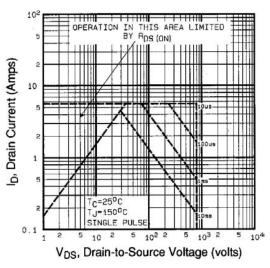


Fig. 8 - Maximum Safe Operating Area

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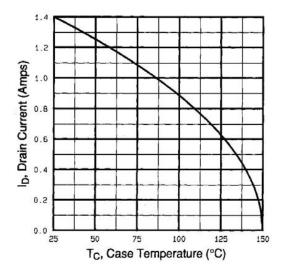


Fig. 9 - Maximum Drain Current vs. Case Temperature

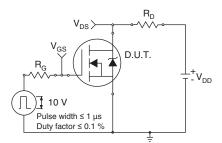


Fig. 10a - Switching Time Test Circuit

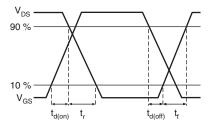


Fig. 10b - Switching Time Waveforms

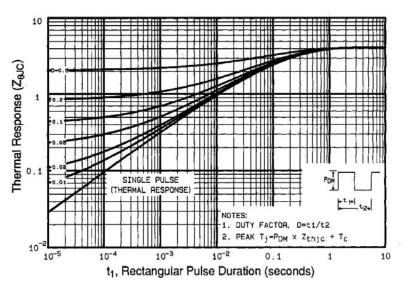


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

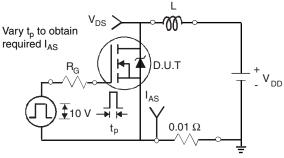


Fig. 12a - Unclamped Inductive Test Circuit

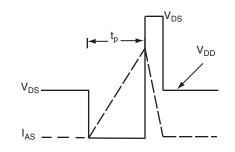


Fig. 12b - Unclamped Inductive Waveforms

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Document Number: 91183

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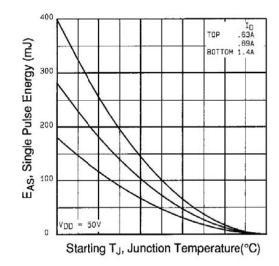


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

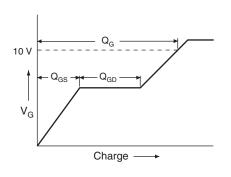


Fig. 13a - Basic Gate Charge Waveform

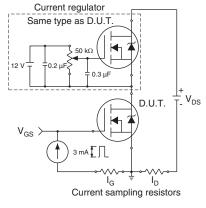
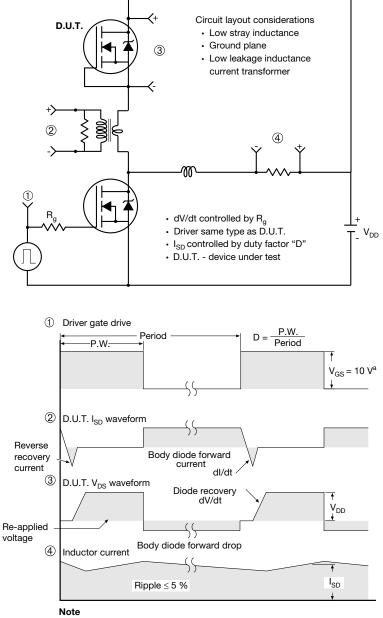


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



a. $V_{GS} = 5 V$ for logic level devices

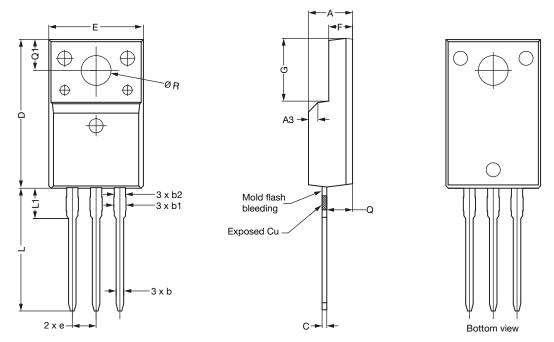
Fig. 14 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



		MILLIMETERS	
DIM.	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
С	0.45	0.50	0.63
D	15.80	15.87	15.97
е		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
ØR	3.08	3.18	3.28

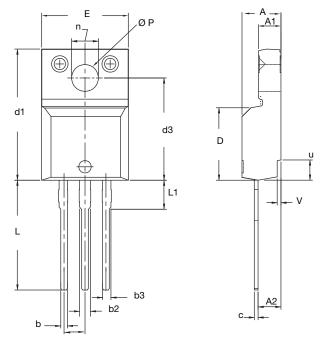
Notes

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
 6. Facility code will be the 1st character located at the 2nd row of the unit marking

1



OPTION 2: FACILITY CODE = Y



MILLIMETERS		IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
С	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
е	2.54	BSC	0.100) BSC
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØP	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

DWG: 5972

Notes

1. To be used only for process drawing

2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads

3. All critical dimensions should C meet $C_{pk} > 1.33$

4. All dimensions include burrs and plating thickness

5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

2

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