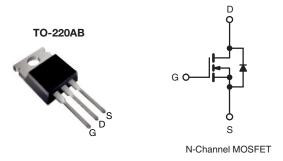
Vishay Siliconix

HALOGEN FREE

# **D Series Power MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V) at T <sub>J</sub> max.	650			
R <sub>DS(on)</sub> max. at 25 °C (Ω)	V <sub>GS</sub> = 10 V	0.340		
Q <sub>g</sub> (Max.) (nC)	90			
Q <sub>gs</sub> (nC)	14			
Q <sub>gd</sub> (nC)	22			
Configuration	Single			



#### **FEATURES**

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance (Ciss)
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM):  $R_{on} \times Q_g$
  - Fast Switching
- Material categorization: For definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### **APPLICATIONS**

- Consumer Electronics
  - Displays (LCD or Plasma TV)
- Lighting
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
  - Battery Chargers
- SMPS

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP17N60D-E3
Lead (Pb)-free and Halogen-free	SiHP17N60D-GE3

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	600	V		
Gate-Source Voltage			$V_{GS}$		± 30	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	$T_{\rm C} = 25  ^{\circ}{\rm C}$ $T_{\rm C} = 100  ^{\circ}{\rm C}$	- I <sub>D</sub>	17		
		T <sub>C</sub> = 100 °C		10.7	Α	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	48		
Linear Derating Factor				2.22	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	165.6	mJ	
Maximum Power Dissipation			$P_{D}$	277.8	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C		
Drain-Source Voltage Slope	T <sub>J</sub> = 125 °C		ط///ط <del>ا</del>	24	1//	
Reverse Diode dV/dt <sup>d</sup>		dV/dt	0.2	- V/ns		
Soldering Recommendations (Peak Temperature)c	for 10 s			300	°C	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $V_{DD} = 50 \text{ V}$ , starting  $T_J = 25 \,^{\circ}\text{C}$ ,  $L = 2.3 \,^{\circ}\text{mH}$ ,  $R_q = 25 \,^{\circ}\Omega$ ,  $I_{AS} = 12 \,^{\circ}\text{A}$ .
- c. 1.6 mm from case.
- d.  $I_{SD} \le I_D$ , starting  $T_J = 25$  °C.



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	=	62	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	0.45	G/ <b>VV</b>	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static						L	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.7	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> :	$V_{DS} = V_{GS}, I_D = 250 \mu A$		-	5	V
Gate-Source Leakage	I <sub>GSS</sub>		$V_{GS} = \pm 30 \text{ V}$		-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$		-	1	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V			0.275	0.340	Ω
Forward Transconductancea	9 <sub>fs</sub>	$V_{DS} = 50 \text{ V}, I_{D} = 8 \text{ A}$		-	6.2	-	S
Dynamic	<u> </u>		<u>-</u>			L	
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 V$ ,		-	1780	-	pF
Output Capacitance	C <sub>oss</sub>	1	$V_{DS} = 100 \text{ V},$		140	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		-	15	-	
Total Gate Charge	Qg		<sub>GS</sub> = 10 V I <sub>D</sub> = 8 A, V <sub>DS</sub> = 480 V	-	45	90	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	14	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	22	-	
Turn-On Delay Time	t <sub>d(on)</sub>		V <sub>DD</sub> = 300 V, I <sub>D</sub> = 8 A		22	45	- ns
Rise Time	t <sub>r</sub>	$V_{DD}$			56	85	
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_g = 9.1 \Omega, V_{GS} = 10 V$		-	37	75	
Fall Time	t <sub>f</sub>			-	30	60	
Internal Gate Resistance	$R_g$	f = 1 MHz, open drain		-	1.6	-	Ω
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET sym showing the	MOSFET symbol showing the		-	17	A
Pulsed Diode Forward Current	I <sub>SM</sub>	integral reverse p - n junction diode		-	-	48	A
Body Diode Voltage	V <sub>SD</sub>	$T_J = 25  ^{\circ}\text{C},  I_S = 8  \text{A},  V_{GS} = 0  \text{V}$		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = I_S,$ $dI/dt = 100 \text{ A/}\mu\text{s}, V_R = 20 \text{ V}$		-	633	950	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	7	15	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	21	42	Α

## Note

a. Repetitive rating; pulse width limited by maximum junction temperature.



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

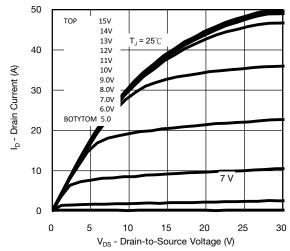


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 150 °C

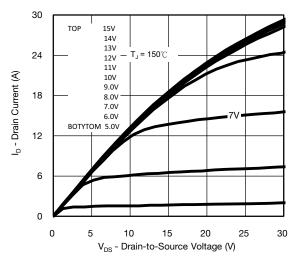


Fig. 2 - Typical Output Characteristics, T<sub>C</sub> = 150 °C

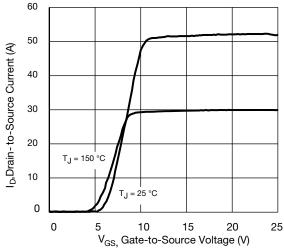


Fig. 3 - Typical Transfer Characteristics

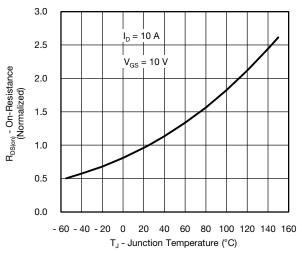


Fig. 4 - Normalized On-Resistance vs. Temperature

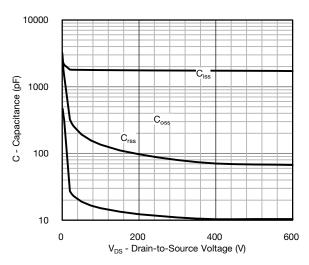


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

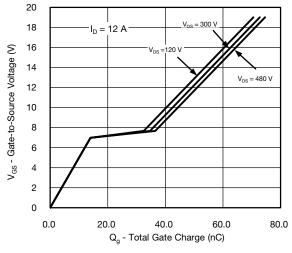


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



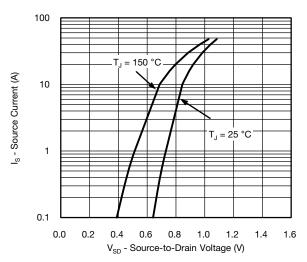


Fig. 7 - Typical Source-Drain Diode Forward Voltage

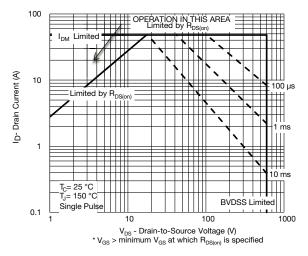


Fig. 8 - Maximum Safe Operating Area

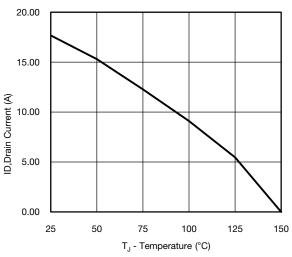


Fig. 9 - Maximum Drain Current vs. Case Temperature

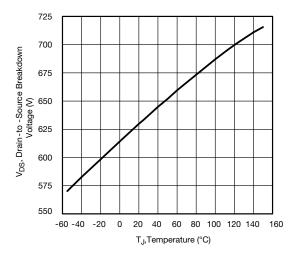


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

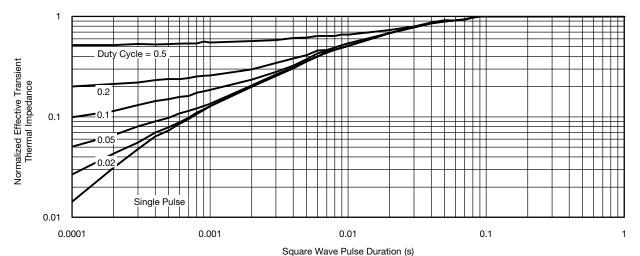


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

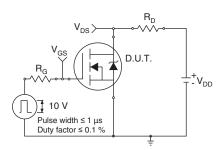


Fig. 12 - Switching Time Test Circuit

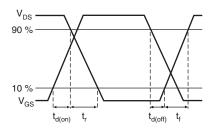


Fig. 13 - Switching Time Waveforms

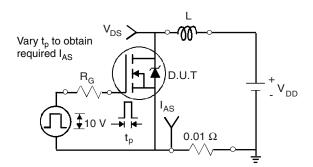


Fig. 14 - Unclamped Inductive Test Circuit

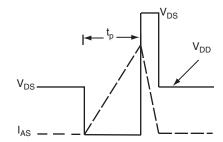


Fig. 15 - Unclamped Inductive Waveforms

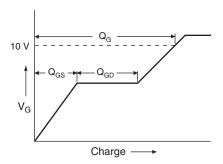


Fig. 16 - Basic Gate Charge Waveform

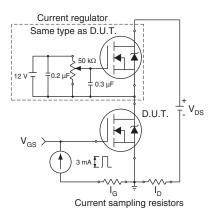
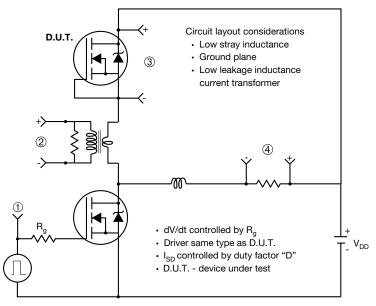


Fig. 17 - Gate Charge Test Circuit



### Peak Diode Recovery dV/dt Test Circuit



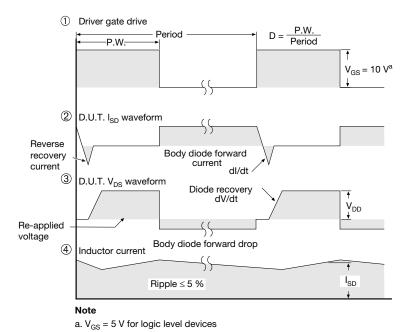


Fig. 18 - For N-Channel

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