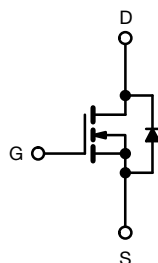
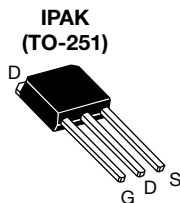


E Series Power MOSFET



N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{DS(on)} \times Q_g$
- Low effective capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	850	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	1.25
Q_g max. (nC)	16.5	
Q_{gs} (nC)	3	
Q_{gd} (nC)	5	
Configuration	Single	

ORDERING INFORMATION

Package	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHU4N80AE-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	800	V
Gate-source voltage			V _{GS}	± 30	
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	4.1	A
		T _C = 100 °C		2.6	
Pulsed drain current ^a			I _{DM}	7.0	
Linear derating factor				0.5	W/°C
Single pulse avalanche energy ^b			E _{AS}	6.9	mJ
Maximum power dissipation			P _D	62.5	W
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Drain-source voltage slope		T _J = 125 °C	dv/dt	70	V/ns
Reverse diode dv/dt ^d				0.2	
Soldering recommendations (peak temperature) ^c		For 10 s		260	°C


Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 0.7$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, di/dt = 100 A/ μ s, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

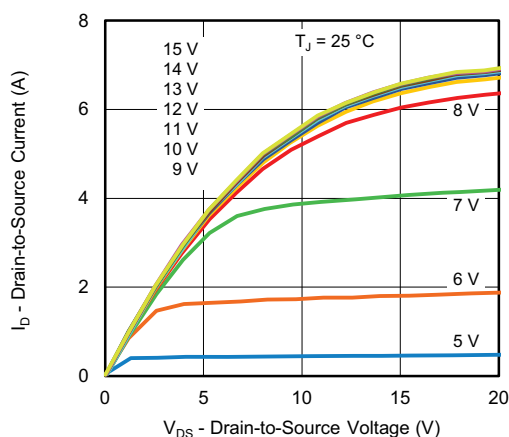
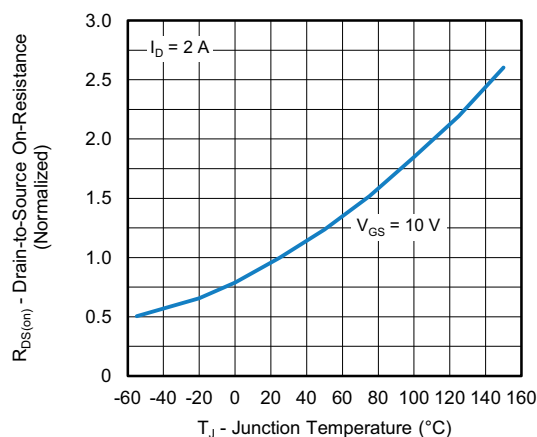
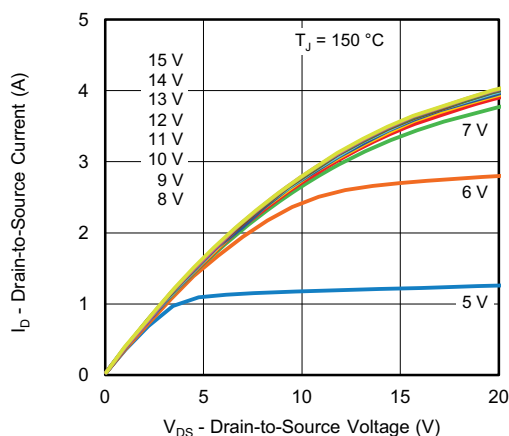
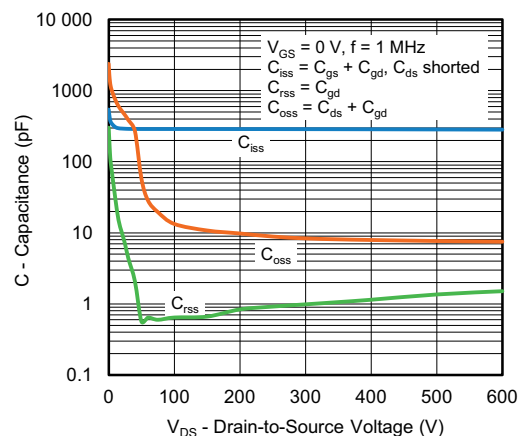
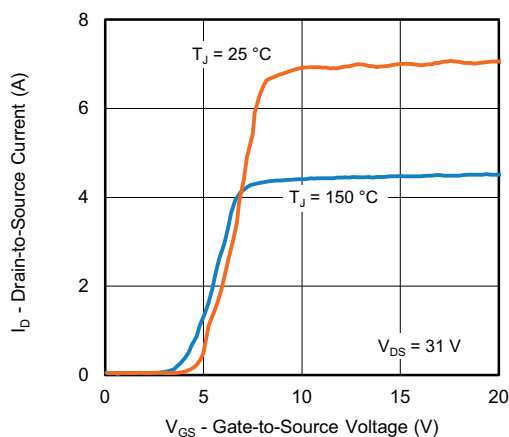
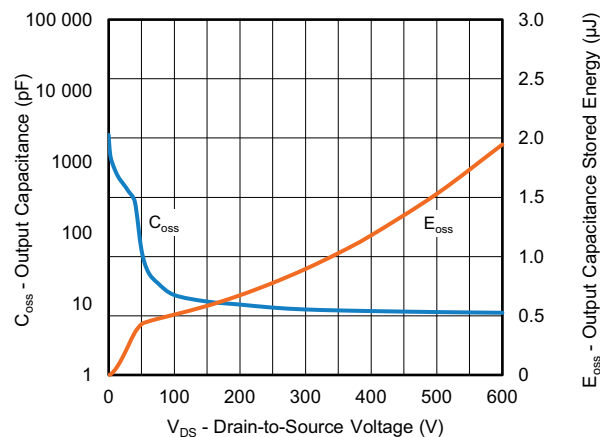
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	2.0	

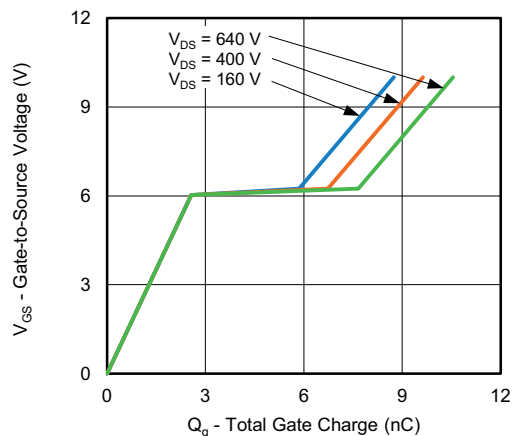
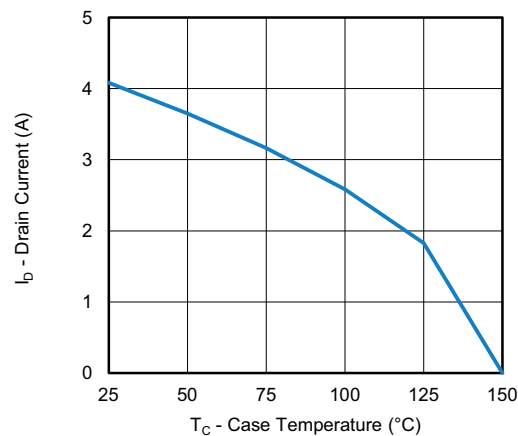
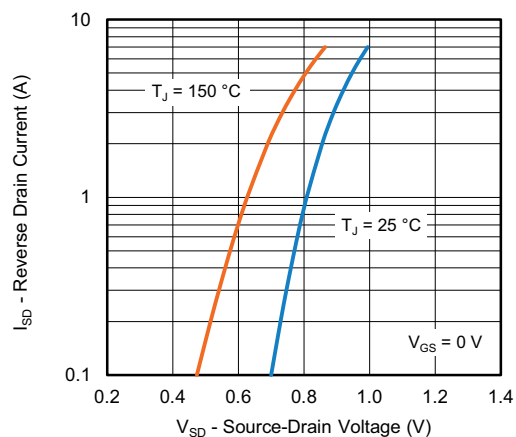
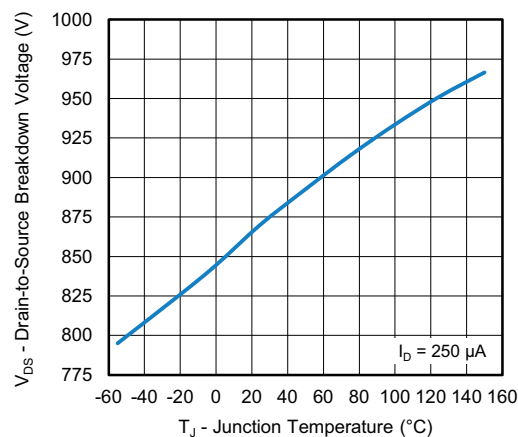
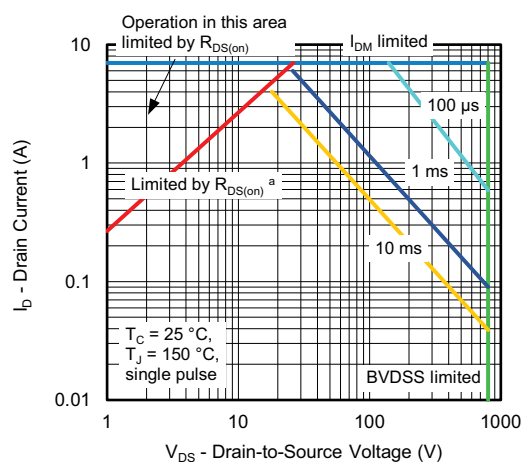
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		800	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$		-	0.8	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 10	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 640\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.0\text{ A}$	-	1.25	1.44	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 2\text{ A}$		-	1.1	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$		-	11	-	pF
Output capacitance	C_{oss}			-	3	-	
Reverse transfer capacitance	C_{rss}			-	5	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}$, $V_{GS} = 0\text{ V}$		-	10	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	65	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 2\text{ A}$, $V_{DS} = 640\text{ V}$	-	11	16.5	nC
Gate-source charge	Q_{gs}			-	3	-	
Gate-drain charge	Q_{gd}			-	5	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 640\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 4.7\text{ }\Omega$		-	11	22	ns
Rise time	t_r			-	7	14	
Turn-off delay time	$t_{d(off)}$			-	12	24	
Fall time	t_f			-	25	50	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain		1.7	3.5	7.0	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4.0	A
Pulsed diode forward current	I_{SM}			-	-	7.0	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 2\text{ A}$, $V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$		-	266	532	ns
Reverse recovery charge	Q_{rr}			-	1.1	2.2	μC
Reverse recovery current	I_{RRM}			-	6.6	-	A

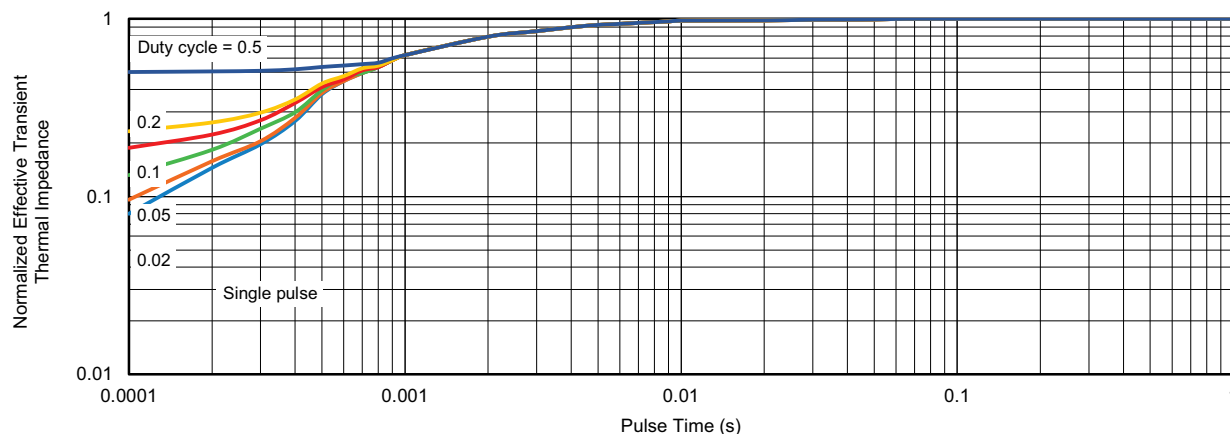
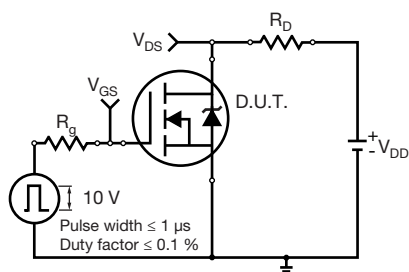
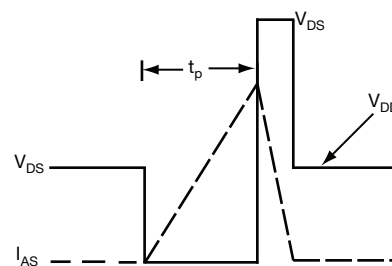
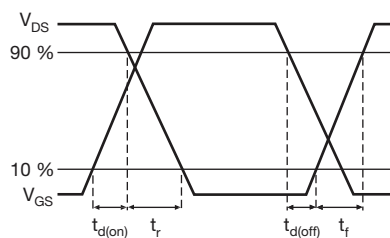
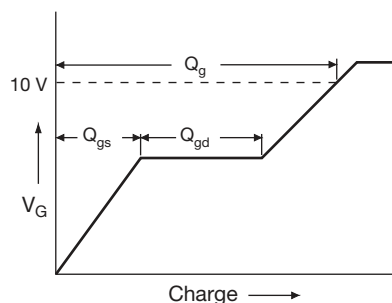
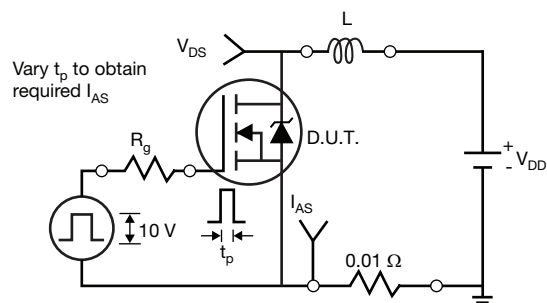
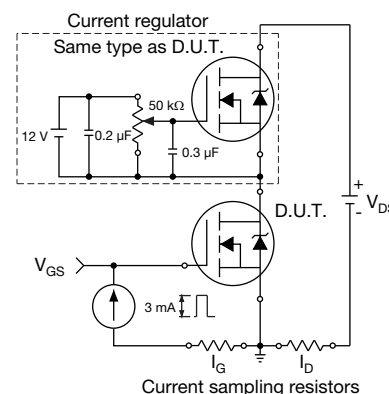
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

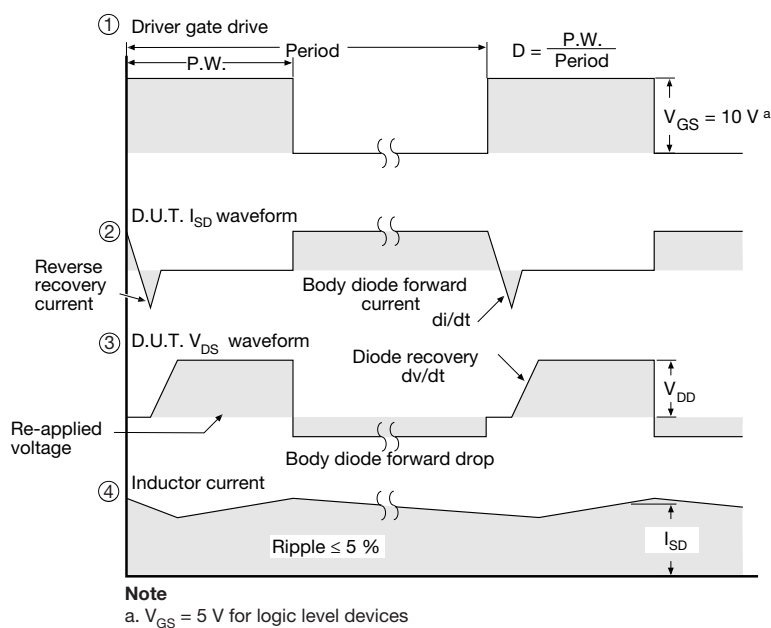
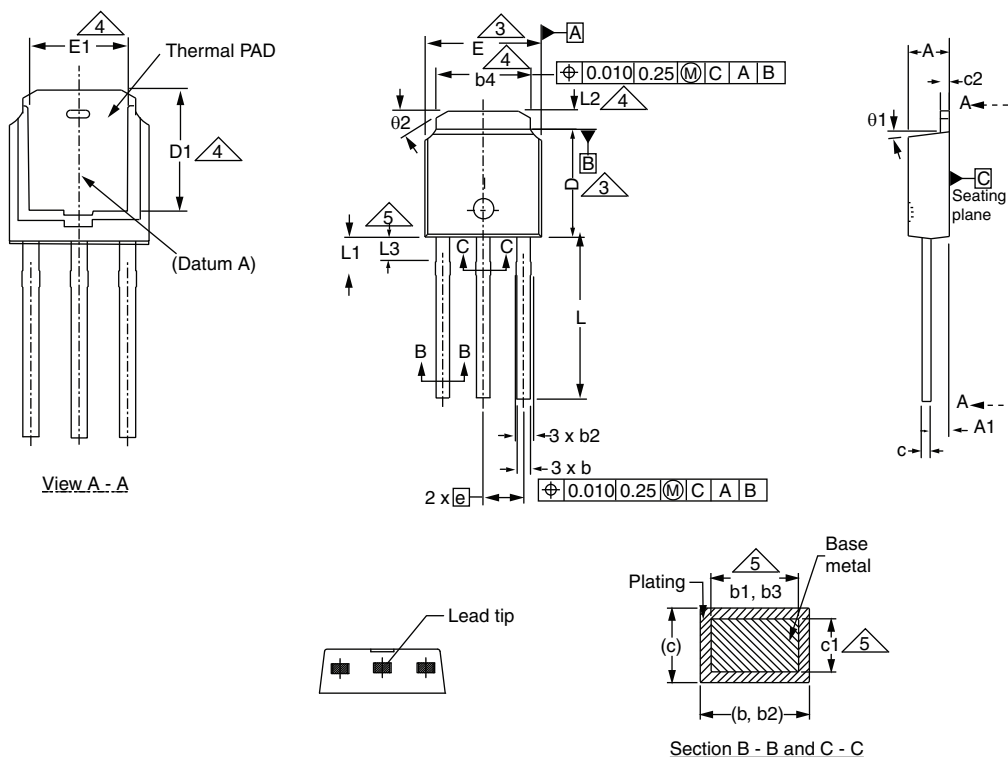


Fig. 19 - For N-Channel

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Case Outline for TO-251AA (High Voltage)

OPTION 1:



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

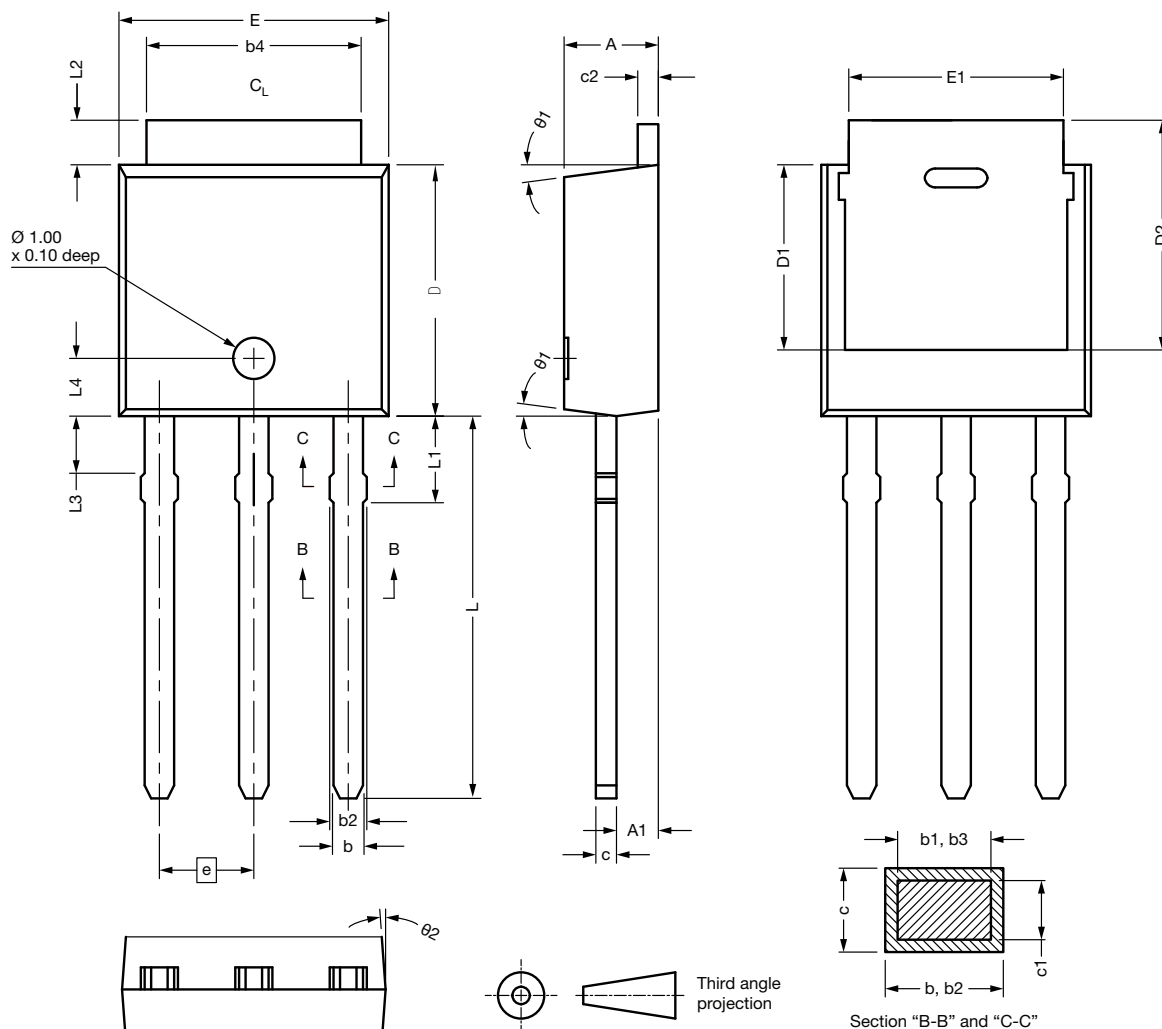
ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
theta1	0°	7.5°	15°
theta2	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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