SCR/SCR and SCR/Diode (MAGN-A-PAK Power Modules), 230 A



MAGN-A-PAK

FEATURES

- High voltage
- Electrically isolated base plate
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	230 A
Type	Modules - thyristor, standard
Package	MAGN-A-PAK

DESCRIPTION

This VSK series of MAGN-A-PAK modules uses high voltage power thyristor/thyristor and thyristor/diode in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode. These modules are intended for general purpose applications such as battery chargers, welders, motor drives, UPS, etc.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$	85 °C	230	A
$I_{T(RMS)}$		510	
I_{TSM}	50 Hz	7500	
	60 Hz	7850	
I^2t	50 Hz	280	kA^2s
	60 Hz	260	
$I^2\sqrt{t}$		280	$kA^2\sqrt{s}$
V_{DRM}/V_{RRM}		800 to 2000	V
T_J	Range	-40 to +130	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE BLOCKING VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 130 °C MAXIMUM mA
VS-VSK.230-	08	800	900	50
	12	1200	1300	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

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ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			230	A
					85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch			510	A
Maximum peak, one-cycle on-state non-repetitive, surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	7500	
		t = 8.3 ms			7850	
		t = 10 ms	100 % V_{RRM} reapplied		6300	
		t = 8.3 ms			6600	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		280	kA^2s
		t = 8.3 ms			256	
		t = 10 ms	100 % V_{RRM} reapplied		198	
		t = 8.3 ms			181	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			2800	$kA^2\sqrt{s}$
Low level value or threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.03	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.07	
Low level value on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.77	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.73	
Maximum on-state voltage drop	V_{TM}	I_{TM} = π x $I_{T(AV)}$, $T_J = T_J$ maximum, 180° conduction, average power = $V_{T(TO)}$ x $I_{T(AV)}$ + r_f x $(I_{T(RMS)})^2$			1.59	V
Maximum holding current	I_H	Anode supply = 12 V, initial I_T = 30 A, T_J = 25 °C			500	mA
Maximum latching current	I_L	Anode supply = 12 V, resistive load = 1 Ω, gate pulse: 10 V, 100 µs, T_J = 25 °C			1000	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical delay time	t_d	T_J = 25 °C, gate current = 1 A dI_g/dt = 1 A/µs, V_d = 0.67 % V_{DRM}	1.0	µs
Typical rise time	t_r		2.0	
Typical turn-off time	t_q	I_{TM} = 300 A; dI/dt = 15 A/µs; $T_J = T_J$ maximum; V_R = 50 V; dV/dt = 20 V/µs; gate 0 V, 100 Ω	50 to 150	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum	50	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted, 25 °C, 1 s	3000	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated V_{DRM}	1000	V/µs

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P_{GM}	$t_p \le 5$ ms, $T_J = T_J$ maximum		10.0	W
Maximum average gate power	$P_{G(AV)}$	f = 50 Hz, $T_J = T_J$ maximum		2.0	
Maximum peak gate current	+ I_{GM}	$t_p \le 5$ ms, $T_J = T_J$ maximum		3.0	A
Maximum peak negative gate voltage	- V_{GT}	$t_p \le 5$ ms, $T_J = T_J$ maximum		5.0	V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = -40 °C	Anode supply = 12 V, resistive load; Ra = 1 Ω	4.0	
		T_J = 25 °C		3.0	
		$T_J = T_J$ maximum		2.0	
Maximum required DC gate current to trigger	I_{GT}	T_J = - 40 °C	Anode supply = 12 V, resistive load; Ra = 1 Ω	350	mA
		T_J = 25 °C		200	
		$T_J = T_J$ maximum		100	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied		0.25	V
Maximum gate current that will not trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied		10.0	mA
Maximum rate of rise of turned-on current	dI/dt	$T_J = T_J$ maximum, I_{TM} = 400 A, rated V_{DRM} applied		500	A/µs

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THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Junction operating temperature range	T_J		-40 to +130	°C
Storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.125	K/W
Typical thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface flat, smooth, and greased	0.02	
Mounting torque ± 10 % — MAGN-A-PAK to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of about 3 h to allow for the spread of the compound.	4 to 6	Nm
Mounting torque ± 10 % — busbar to MAGN-A-PAK				
Approximate weight			500	g
			17.8	oz.
Case style			MAGN-A-PAK	

ΔR CONDUCTION PER JUNCTION											
DEVICES	**SINUSOIDAL CONDUCTION AT T_J MAXIMUM**					**RECTANGULAR CONDUCTION AT T_J MAXIMUM**					**UNITS**
	180°	**120°**	**90°**	**60°**	**30°**	**180°**	**120°**	**90°**	**60°**	**30°**	
VSK.230-	0.009	0.010	0.010	0.020	0.032	0.007	0.011	0.015	0.020	0.033	K/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

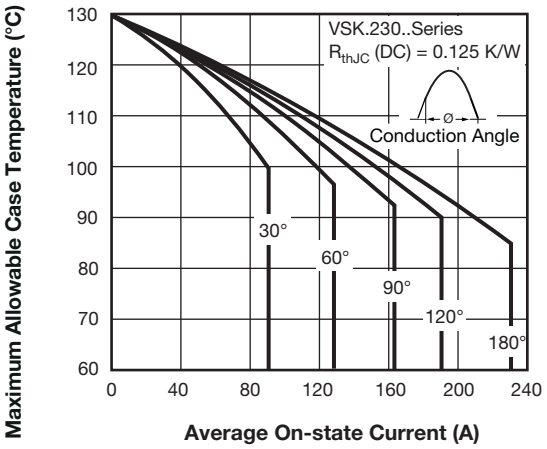


Fig. 1 - Current Ratings Characteristics

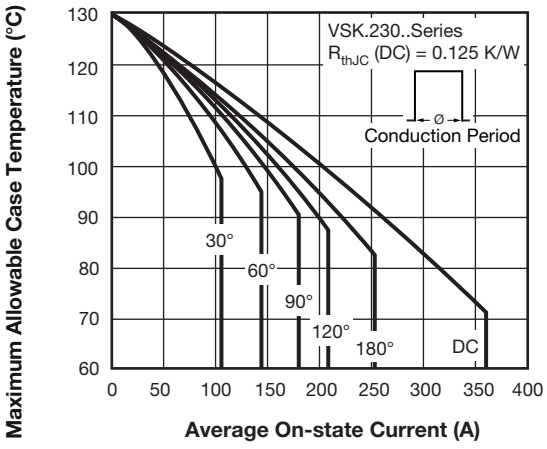


Fig. 2 - Current Ratings Characteristics

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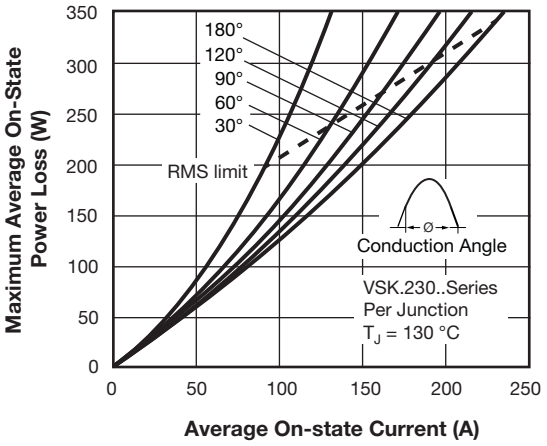


Fig. 3 - On-State Power Loss Characteristics

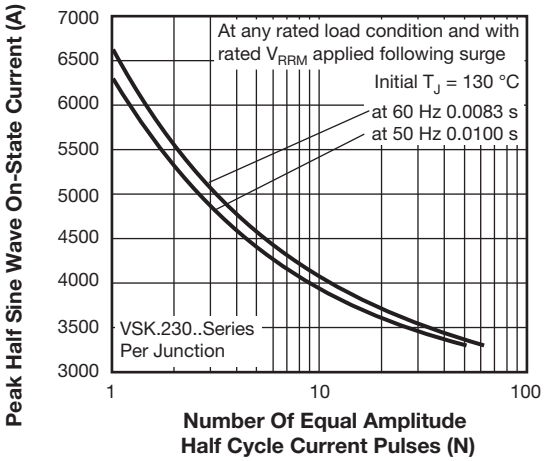


Fig. 5 - Maximum Non-Repetitive Surge Current

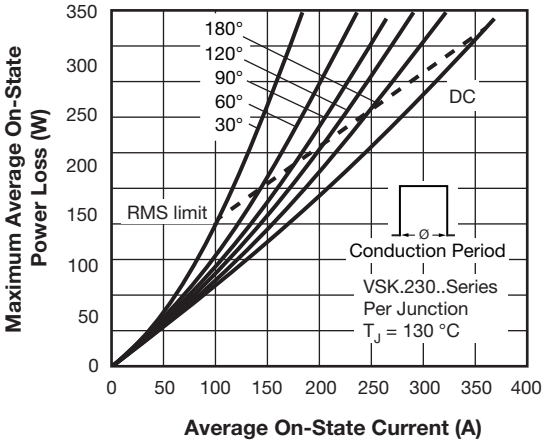


Fig. 4 - On-State Power Loss Characteristics

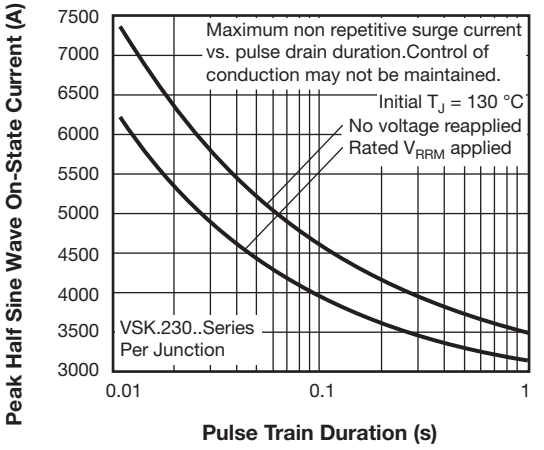


Fig. 6 - Maximum Non-Repetitive Surge Current

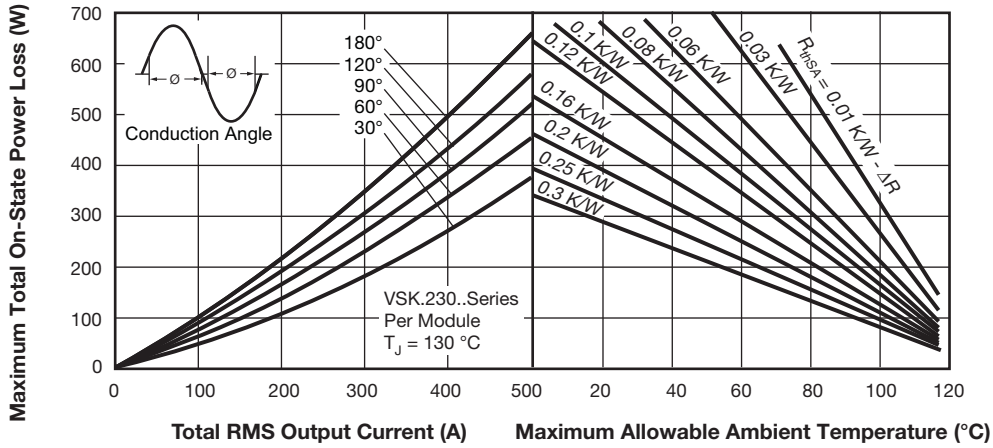


Fig. 7 - On-State Power Loss Characteristics

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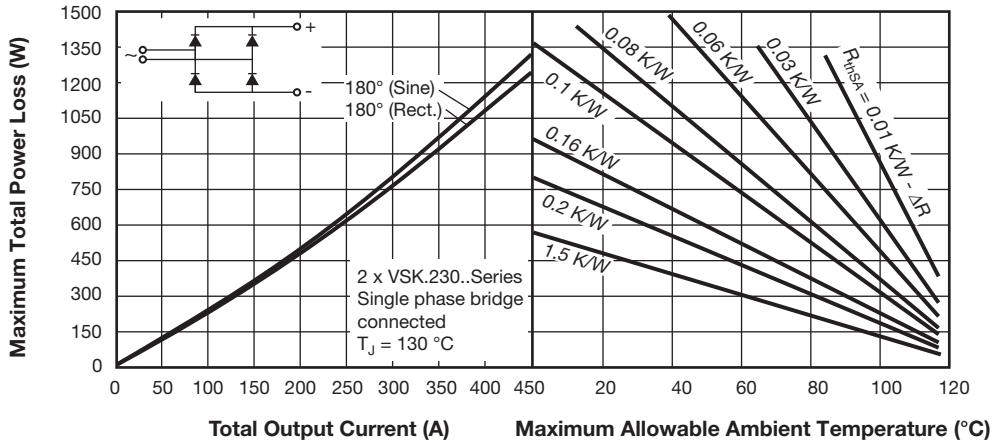


Fig. 8 - On-State Power Loss Characteristics

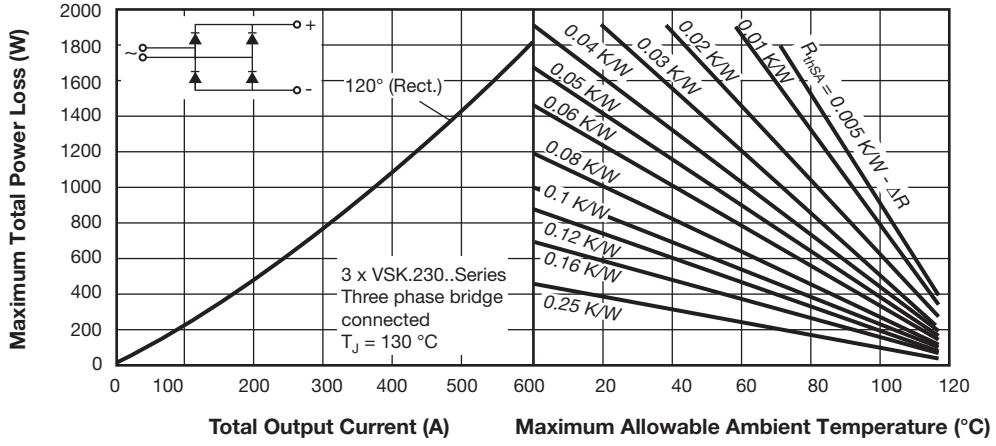


Fig. 9 - On-State Power Loss Characteristics

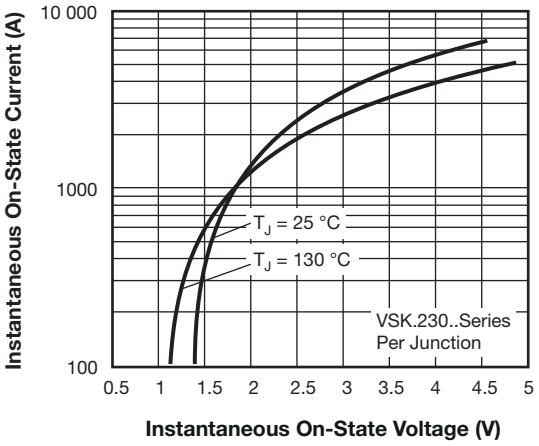


Fig. 10 - On-State Voltage Drop Characteristics

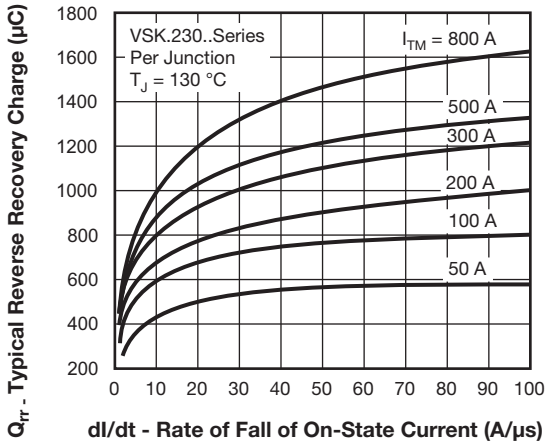


Fig. 11 - Reverse Recovery Charge Characteristics

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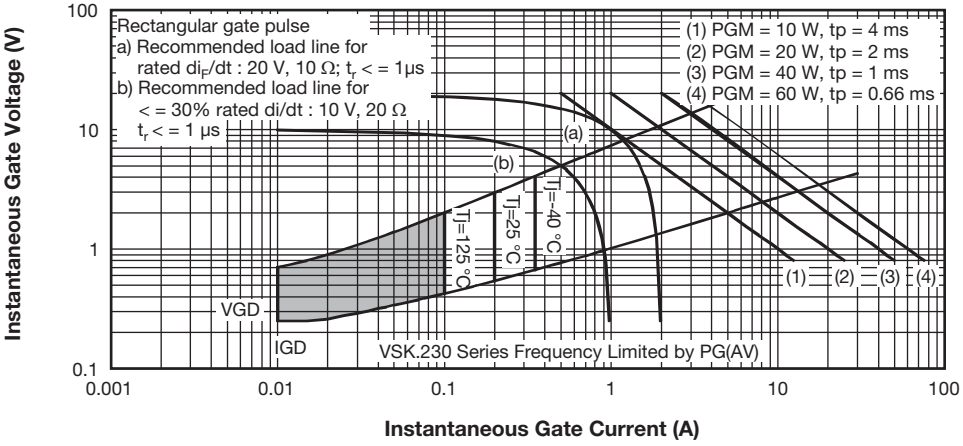


Fig. 12 - Gate Characteristics

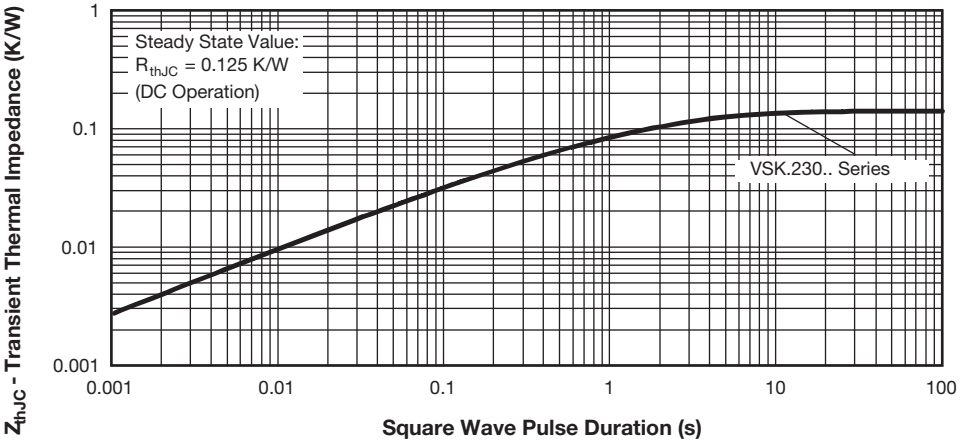


Fig. 13 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

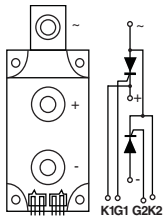
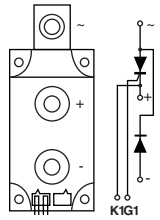
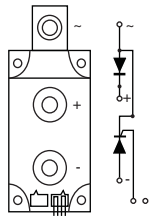
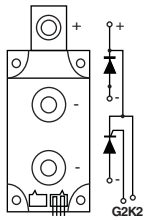
Device code	VS-VS	KT	230	-	20	PbF
	1	2	3		4	5

- **1** - Vishay Semiconductors product
- **2** - Circuit configuration (see dimensions - link at the end of datasheet)
- **3** - Current rating
- **4** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- **5** - • None = standard production
  • PbF = lead (Pb)-free

Note

- To order the optional hardware go to www.vishay.com/doc?95172

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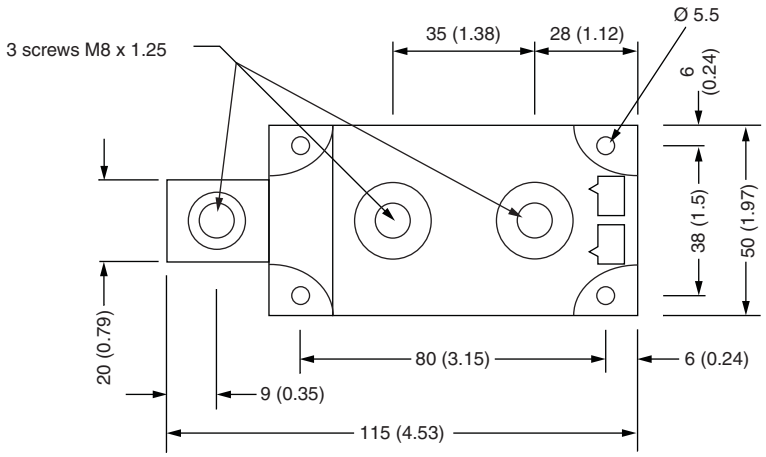
CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Two SCRs doubler circuit	KT	**VSKT...**  Available 800 V: contact factory for different requirements
SCR/diode doubler circuit, positive control	KH	**VSKH...**  Available 800 V: contact factory for different requirements
SCR/diode doubler circuit, negative control	KL	**VSKL...**  Available 800 V: contact factory for different requirements
Two SCRs common cathodes	KK	**VSKK...**  Available 800 V: contact factory for different requirements

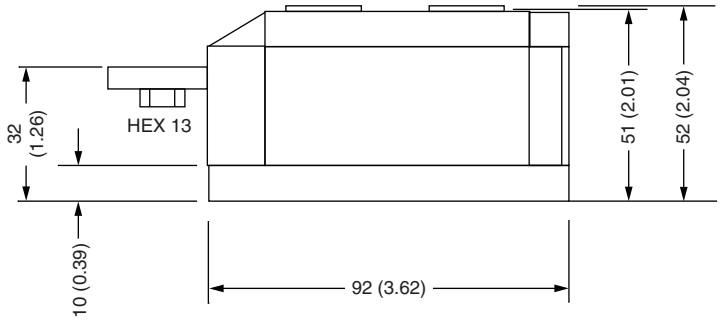
LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95086

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MAGN-A-PAK

DIMENSIONS in millimeters (inches)





Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0

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