



## Phase Control Thyristors (Stud Version), 80 A



TO-94 (TO-209AC)

### FEATURES

- Hermetic glass-metal seal
- International standard case TO-94 (TO-209AC)
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

**RoHS**  
COMPLIANT

### TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

### PRIMARY CHARACTERISTICS

$I_{T(AV)}$	80 A
$V_{DRM}/V_{RRM}$	400 V, 800 V, 1200 V
$V_{TM}$	1.60 V
$I_{GT}$	120 mA
$T_J$	-40 °C to +125 °C
Package	TO-94 (TO-209AC)
Circuit configuration	Single SCR

### MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		80	A
	$T_C$	85	°C
$I_{T(RMS)}$		125	A
$I_{TSM}$	50 Hz	1900	
	60 Hz	1990	
$I^2t$	50 Hz	18	kA <sup>2</sup> s
	60 Hz	16	
$V_{DRM}/V_{RRM}$		400 to 1200	V
$t_q$	Typical	110	μs
$T_J$		-40 to +125	°C

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = 125$ °C mA
VS-80RIA VS-81RIA	40	400	500	15
	80	800	900	
	120	1200	1300	

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave	80	A
			85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 75 °C case temperature	125	
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	t = 10 ms t = 8.3 ms t = 10 ms t = 8.3 ms	No voltage reappplied 100 % $V_{RRM}$ reappplied	1900 1990 1600 1675
		Sinusoidal half wave, initial $T_J = T_J$ maximum		A
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms t = 8.3 ms t = 10 ms t = 8.3 ms	No voltage 100 % $V_{RRM}$ reappplied	18 16 12.7 11.7
				$kA^2s$
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied	180.5	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum	0.99	V
High level value of threshold voltage	$V_{T(TO)2}$	( $I > \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum	1.13	
Low level value of on-state slope resistance	$r_{t1}$	(16.7 % $\times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum	2.29	$m\Omega$
High level value of on-state slope resistance	$r_{t2}$	( $I > \pi \times I_{T(AV)}$ ), $T_J = T_J$ maximum	1.84	
Maximum on-state voltage	$V_{TM}$	$I_{pk} = 250$ A, $T_J = 25$ °C, $t_p = 10$ ms sine pulse	1.60	V
Maximum holding current	$I_H$	$T_J = 25$ °C, anode supply 12 V resistive load	200	mA
Typical latching current	$I_L$		400	

**SWITCHING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	$di/dt$	$T_J = 125$ °C, $V_d = \text{Rated } V_{DRM}$ , $I_{TM} = 2 \times di/dt$ snubber 0.2 $\mu F$ , 15 $\Omega$ , gate pulse: 20 V, 65 $\Omega$ , $t_p = 6$ $\mu s$ , $t_r = 0.5$ $\mu s$ Per JEDEC standard RS-397, 5.2.2.6.	300	A/ $\mu s$
Typical delay time	$t_d$	Gate pulse: 10 V, 15 $\Omega$ source, $t_p = 6$ $\mu s$ , $t_r = 0.1$ $\mu s$ , $V_d = \text{Rated } V_{DRM}$ , $I_{TM} = 50$ Adc, $T_J = 25$ °C	1	$\mu s$
Typical turn-off time	$t_q$	$I_{TM} = 50$ A, $T_J = T_J$ maximum, $di/dt = -5$ A/ $\mu s$ , $V_R = 50$ V, $dV/dt = 20$ V/ $\mu s$ , gate bias: 0 V 25 $\Omega$ , $t_p = 500$ $\mu s$	110	

**BLOCKING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	$dV/dt$	$T_J = 125$ °C exponential to 67 % rated $V_{DRM}$	500	V/ $\mu s$
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = 125$ °C rated $V_{DRM}/V_{RRM}$ applied	15	mA



TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P <sub>GM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, t <sub>p</sub> ≤ 5 ms		12	W
Maximum average gate power	P <sub>G(AV)</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, f = 50 Hz, d% = 50		3	
Maximum peak positive gate current	I <sub>GM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, t <sub>p</sub> ≤ 5 ms		3	A
Maximum peak positive gate voltage	+ V <sub>GM</sub>			20	V
Maximum peak negative gate voltage	- V <sub>GM</sub>			10	
Maximum DC gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 6 V anode to cathode applied	270	mA
		T <sub>J</sub> = 25 °C		120	
		T <sub>J</sub> = 125 °C		60	
Maximum DC gate voltage required to trigger	V <sub>GT</sub>	T <sub>J</sub> = - 40 °C		3.5	V
		T <sub>J</sub> = 25 °C		2.5	
		T <sub>J</sub> = 125 °C		1.5	
DC gate current not to trigger	I <sub>GD</sub>	T <sub>J</sub> = T <sub>J</sub> maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V <sub>DRM</sub> anode to cathode applied	6	mA
DC gate voltage not to trigger	V <sub>GD</sub>			0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T <sub>J</sub>		- 40 to 125	°C
Maximum storage temperature range	T <sub>Stg</sub>		- 40 to 150	
Maximum thermal resistance, junction to case	R <sub>thJC</sub>	DC operation	0.30	K/W
Maximum thermal resistance, case to heatsink	R <sub>thCS</sub>	Mounting surface, smooth, flat and greased	0.1	
Mounting torque, ± 10 %		Non-lubricated threads	15.5 (137)	N · m (lbf · in)
		Lubricated threads	14 (120)	
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-94 (TO-209AC)	

$\Delta R_{thJC}$ CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.042	0.030	$T_J = T_J$ maximum	K/W
120°	0.050	0.052		
90°	0.064	0.070		
60°	0.095	0.100		
30°	0.164	0.165		

#### Note

- The table above shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

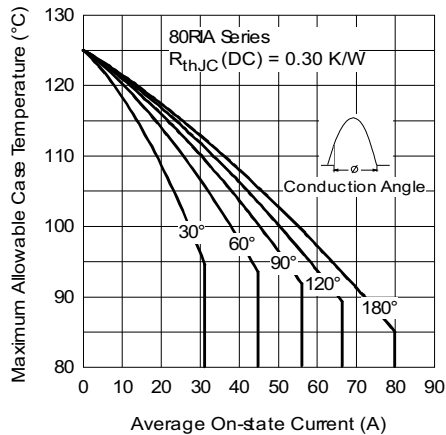


Fig. 1 - Current Ratings Characteristics

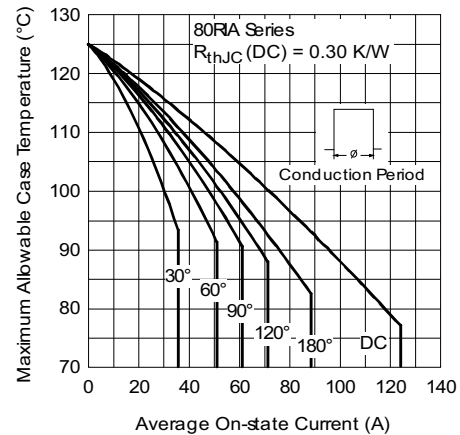


Fig. 2 - Current Ratings Characteristics

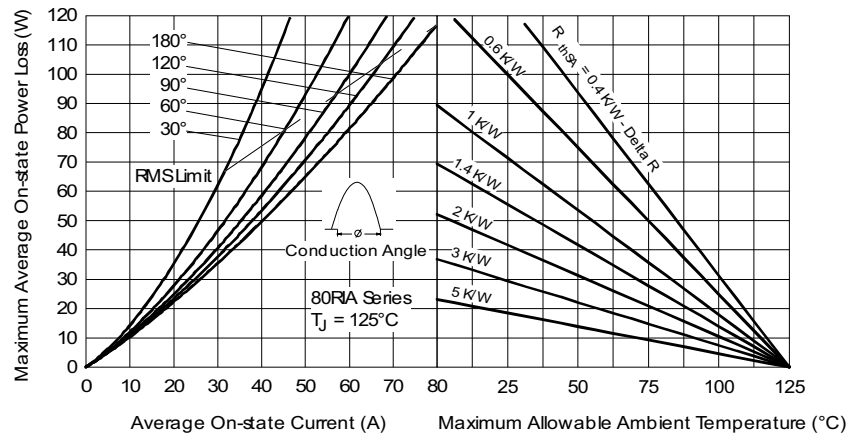


Fig. 3 - On-State Power Loss Characteristics

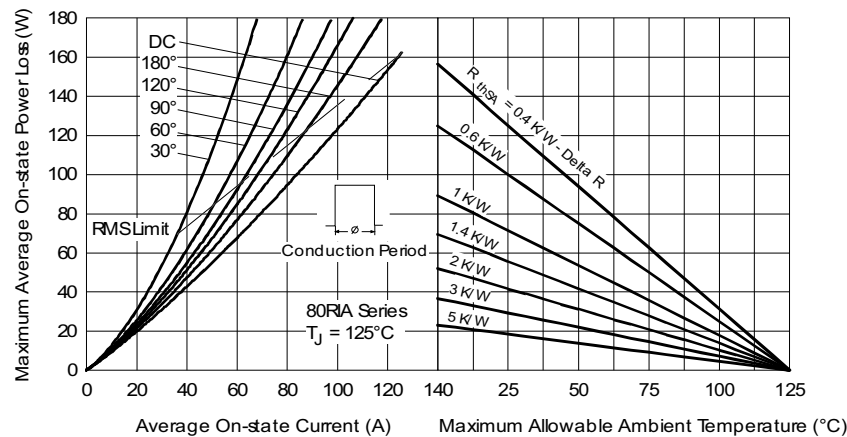


Fig. 4 - On-State Power Loss Characteristics

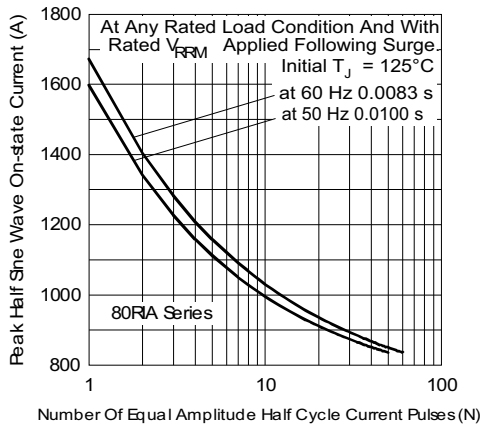


Fig. 5 - Maximum Non-Repetitive Surge Current

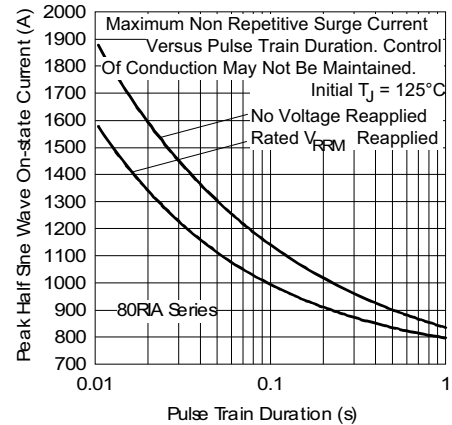


Fig. 6 - Maximum Non-Repetitive Surge Current

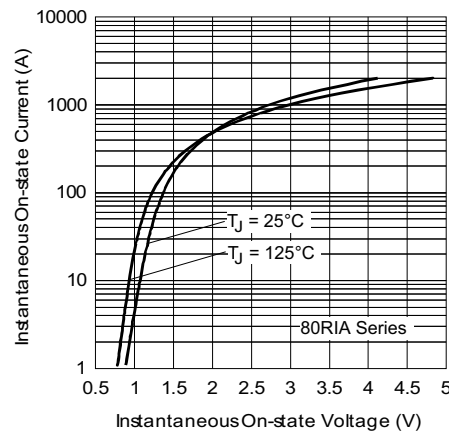


Fig. 7 - On-State Voltage Drop Characteristics

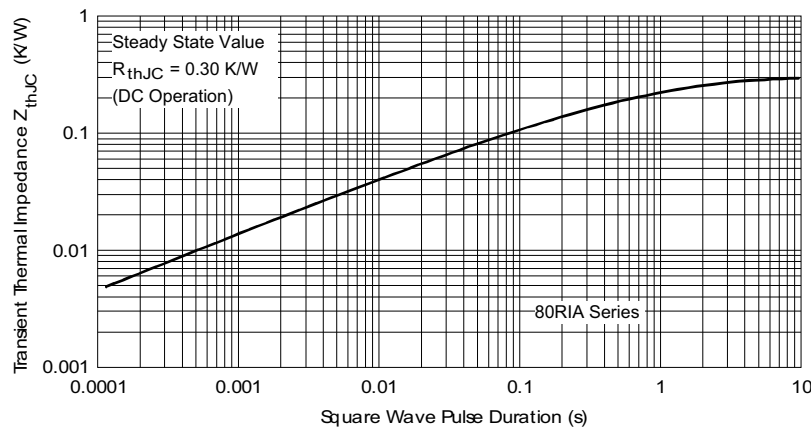


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

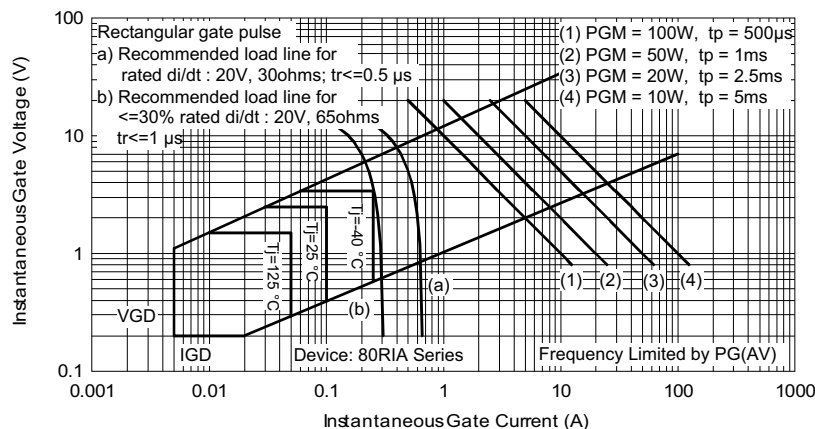


Fig. 9 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	VS-	8	0	RIA	120	M	PbF
	1	2	3	4	5	6	7
1	-	Vishay Semiconductors product					
2	-	$I_{TAV} \times 10$ A					
3	-		• 0 = eyelet terminals (gate and auxiliary cathode leads) • 1 = fast-on terminals (gate and auxiliary cathode leads) • 2 = flag terminals (gate and auxiliary cathode terminals)				
4	-	RIA = essential part number					
5	-	Voltage code $\times 100 = V_{RRM}$ (see Voltage Ratings table)					
6	-		• None = stud base 1/2"-20UNF- 2 A threads • M = stud base metric threads M12 x 1.75 E 6				
7	-		None = standard production PbF = lead (Pb)-free				

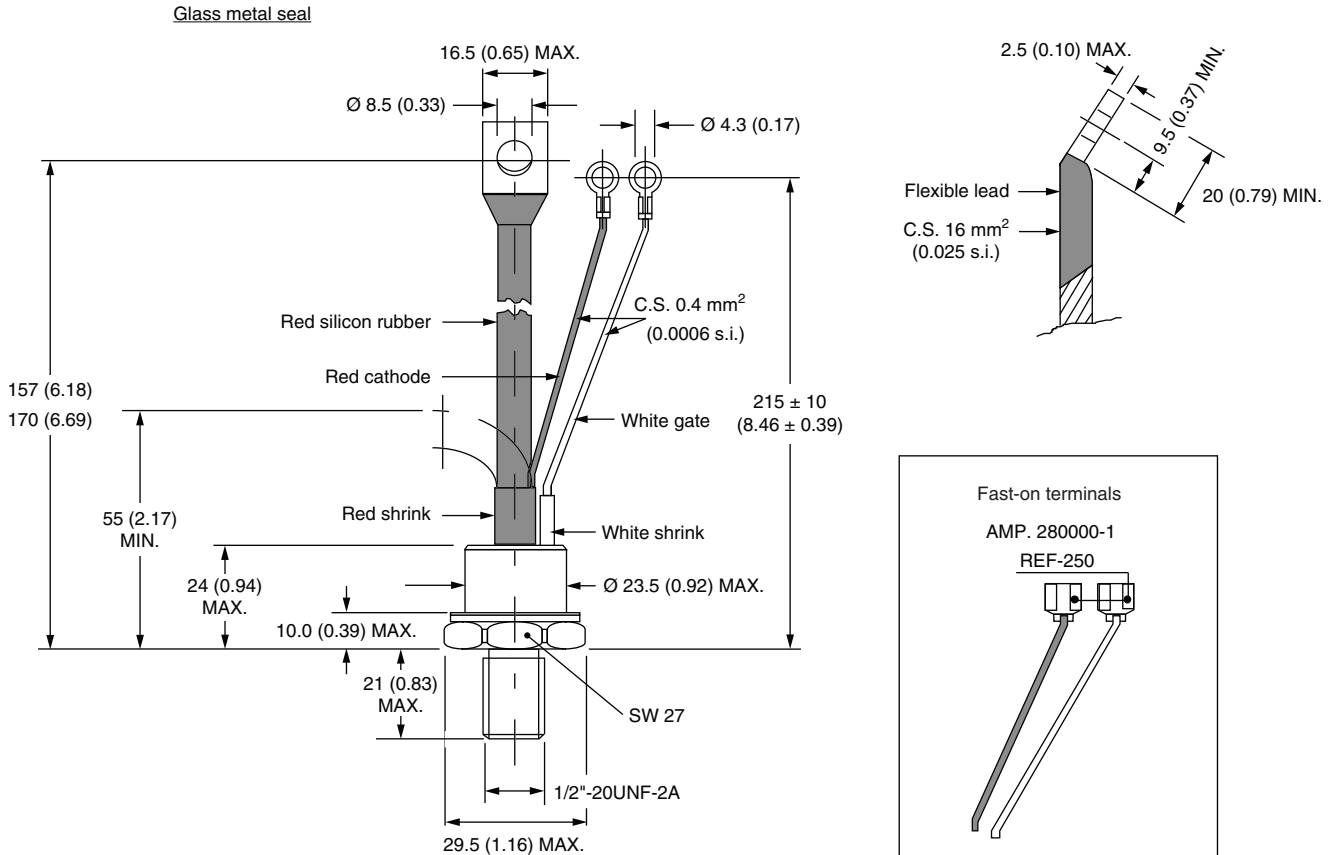
## LINKS TO RELATED DOCUMENTS

Dimensions

[www.vishay.com/doc?95362](http://www.vishay.com/doc?95362)

## TO-209AC (TO-94) for 80RIA Series

**DIMENSIONS** in millimeters (inches)





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