EMIPAK 1B PressFit Power Module 650 V PFC and Full Bridge MOSFET, 25 A

EMIPAK 1B (package example)

PRIMARY CHARACTERISTICS	
QB1 - QB2 PFC MOSFET	
V_{DSS}	650 V
$R_{DS(on)}$ typical at I_C = 25 A	59 mΩ
I_D at T_{SINK} = 65 °C	25 A
Q1 to Q4 FULL BRIDGE MOSFET	
V_{DSS}	650 V
$R_{DS(on)}$ typical at I_C = 25 A	59 mΩ
I_D at T_{SINK} = 65 °C	25 A
DB1 - DB2 SILICON CARBIDE CLAMP DIODE	
V_{RRM}	650 V
V_{FM} typical at 12 A	1.52 V
I_F at T_{SINK} = 69 °C	12 A
Package	EMIPAK 1B
Circuit configuration	MOSFET dual boost PFC and MOSFET full bridge inverter
Type	Modules - MOSFET

FEATURES

- E series power MOSFET with fast body diode
- SiC diode technology
- Exposed Al_2O_3 substrate with low thermal resistance
- Low input capacitance
- Low switching and conduction losses
- Low figure-of-merit (FOM) R_{on} x Q_g
- Ultra low gate charge Q_g
- Low internal inductances
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
  PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

ABSOLUTE MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T_J		150	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	T_J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
QB1 - QB2 PFC MOSFET				
Drain to source voltage	V_{DSS}		650	V
Gate to source voltage	V_{GS}		± 20	
Pulsed drain current	I_{DM}		49	A
Continuous drain current	I_D	T_{SINK} = 25 °C	29	A
		T_{SINK} = 80 °C	22	
Power dissipation	P_D	T_{SINK} = 25 °C	139	W
		T_{SINK} = 80 °C	78	
Single pulse avalanche energy	E_{AS}	L = 10 mH, I_{AS} = 16 A, T_J = 25 °C	1280	mJ
Pulsed source current (body diode)	I_{SM}		225	A

PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and International patents.

ABSOLUTE MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)				
Q1 to Q4 FULL BRIDGE MOSFET				
Drain to source voltage	V_{DSS}		650	V
Gate to source voltage	V_{GS}		± 20	V
Pulsed drain current	I_{DM}	V_{GS} = 10 V	49	A
Continuous drain current	I_D	T_{SINK} = 25 °C	29	A
		T_{SINK} = 80 °C	22	
Power dissipation	P_D	T_{SINK} = 25 °C	139	W
		T_{SINK} = 80 °C	78	
Single pulse avalanche energy	E_{AS}	L = 10 mH, I_{AS} = 16 A, T_J = 25 °C	1280	mJ
Pulsed source current (body diode)	I_{SM}		225	A
DB1 - DB2 SILICON CARBIDE CLAMP DIODE				
Cathode to anode voltage	V_{RRM}		650	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, T_J = 25 °C	85	A
Diode continuous forward current	I_F	T_{SINK} = 25 °C	15	A
		T_{SINK} = 80 °C	11	
Power dissipation	P_D	T_{SINK} = 25 °C	44	W
		T_{SINK} = 80 °C	25	

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 - QB2 PFC MOSFET						
Drain to source breakdown voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	650	-	-	
Drain to source on resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A	-	59	80	mΩ
		V_{GS} = 10 V, I_D = 25 A, T_J = 150 °C	-	132	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.8	2.9	4.4	V
Temperature coefficient of threshold voltage	$\Delta V_{GS(th)}/\Delta T_J$	V_{DS} = V_{GS}, I_D = 250 µA (25 °C to 125 °C)	-	-10.8	-	mV/°C
Forward transconductance	g_{fs}	V_{DS} = 20 V, I_D = 25 A	-	31	-	S
Transfer characteristics	V_{GS}	V_{DS} = 20 V, I_D = 25 A	-	4.76	-	V
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V	-	2	100	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_J = 150 °C	-	700	-	
Gate to source leakage current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 150	nA
QB1 - QB2 PFC MOSFET BODY DIODE						
Source-to-drain voltage drop	V_{SD}	I_{SD} = 25 A, V_{GS} = 0 V	-	0.95	1.32	V
Q1 to Q4 FULL BRIDGE MOSFET						
Drain to source breakdown voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	650	-	-	
Drain to source on resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A	-	59	80	mΩ
		V_{GS} = 10 V, I_D = 25 A, T_J = 150 °C	-	132	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.8	2.9	4.4	V
Temperature coefficient of threshold voltage	$\Delta V_{GS(th)}/\Delta T_J$	V_{DS} = V_{GS}, I_D = 250 µA (25 °C to 125 °C)	-	-10.8	-	mV/°C
Forward transconductance	g_{fs}	V_{DS} = 20 V, I_D = 25 A	-	31	-	S
Transfer characteristics	V_{GS}	V_{DS} = 20 V, I_D = 25 A	-	4.76	-	V
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V	-	2	100	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_J = 150 °C	-	700	-	
Gate to source leakage current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 150	nA
Q1 to Q4 FULL BRIDGE MOSFET BODY DIODE						
Source-to-drain voltage drop	V_{SD}	I_{SD} = 25 A, V_{GS} = 0 V	-	0.95	1.32	V
DB1 - DB2 SILICON CARBIDE CLAMP DIODE						
Forward voltage drop	V_{FM}	I_F = 12 A	-	1.52	2.00	V
		I_F = 12 A, T_J = 150 °C	-	1.92	-	
Breakdown voltage	V_{BR}	I_R = 500 µA	650	-	-	V
Reverse leakage current	I_{RM}	V_R = 650 V	-	1.8	100	µA
		V_R = 650 V, T_J = 150 °C	-	600	-	

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 - QB2 PFC MOSFET						
Total gate charge (turn-on)	Q_g	I_D = 24 A, V_{DS} = 480 V, V_{GS} = 10 V	-	190	-	nC
Gate to source charge (turn-on)	Q_{gs}		-	41	-	
Gate to drain charge (turn-on)	Q_{gd}		-	67	-	
Turn-on switching loss	E_{ON}	I_D = 25 A, V_{DD} = 325 V, V_{GS} = +10 V / -10 V, R_g = 4.7 Ω, L = 500 µH	-	0.11	-	mJ
Turn-on delay time	$t_{d(on)}$		-	14	-	ns
Rise time	t_r		-	9	-	
Turn-off switching loss	E_{OFF}		-	0.06	-	mJ
Turn-off delay time	$t_{d(off)}$		-	78	-	ns
Fall time	t_f		-	7	-	
Turn-on switching loss	E_{ON}	I_D = 25 A, V_{DD} = 325 V, V_{GS} = +10 V / -10 V, R_g = 4.7 Ω, L = 500 µH, T_J = 125 °C	-	0.12	-	mJ
Turn-on delay time	$t_{d(on)}$		-	12	-	ns
Rise time	t_r		-	9	-	
Turn-off switching loss	E_{OFF}		-	0.06	-	mJ
Turn-off delay time	$t_{d(off)}$		-	82	-	ns
Fall time	t_f		-	7	-	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	5900	-	pF
Output capacitance	C_{oss}		-	260	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T_J = 150 °C, I_D = 120 A, V_{DD} = 400 V, V_P = 600 V, R_g = 4.7 Ω, V_{GS} = +10 V / 0 V				
QB1 - QB2 PFC MOSFET BODY DIODE						
Diode reverse recovery time	t_{rr}	V_R = 400 V, T_J = 25 °C, I_S = 22 A, dI/dt = 100 A/µs	-	203	-	ns
Diode reverse recovery current	I_{rr}		-	16	-	A
Diode reverse recovery charge	Q_{rr}		-	1625	-	nC
Q1 to Q4 FULL BRIDGE MOSFET						
Total gate charge (turn-on)	Q_g	I_D = 24 A, V_{DS} = 480 V, V_{GS} = 10 V	-	190	-	nC
Gate-source charge	Q_{gs}		-	41	-	
Gate-drain charge	Q_{gd}		-	67	-	
Turn-off switching loss	E_{OFF}	I_D = 25 A, V_{DD} = 325 V, V_{GS} = +10 V / -10 V, R_g = 4.7 Ω, L = 500 µH	-	0.05	-	mJ
Turn-off delay time	$t_{d(off)}$		-	76	-	ns
Fall time	t_f		-	7	-	
Turn-off switching loss	E_{OFF}	I_D = 25 A, V_{DD} = 325 V, V_{GS} = +10 V / -10 V, R_g = 4.7 Ω, L = 500 µH, T_J = 125 °C	-	0.05	-	mJ
Turn-off delay time	$t_{d(off)}$		-	79	-	ns
Fall time	t_f		-	7	-	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	5900	-	pF
Output capacitance	C_{oss}		-	260	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T_J = 150 °C, I_D = 50 A, V_{DD} = 400 V, V_P = 600 V, R_g = 4.7 Ω, V_{GS} = +10 V / 0 V				
Q1 to Q4 FULL BRIDGE MOSFET BODY DIODE						
Diode reverse recovery time	t_{rr}	V_R = 400 V, T_J = 25 °C, I_S = 22 A, dI/dt = 100 A/µs	-	203	-	ns
Diode reverse recovery current	I_{rr}		-	16	-	A
Diode reverse recovery charge	Q_{rr}		-	1625	-	nC
DB1 - DB2 SILICON CARBIDE CLAMP DIODE						
Total capacitive charge	Q_C	V_R = 400 V, I_F = 12 A, dI/dt = 500 A/µs	-	29	-	nC

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNITS**
Resistance	R_{25}	T_C = 25 °C	5000	Ω
	R_{100}	T_C = 100 °C	493 ± 5 %	
B-value	$B_{25/50}$	$R_2 = R_{25}$ exp. [$B_{25/50}$ (1/T2 - 1/(298.15K))]	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 - QB2 PFC MOSFET - Junction to sink thermal resistance (per switch) [1]	R_{thJS}	-	0.75	-	°C/W
Q1 to Q4 FULL BRIDGE MOSFET - Junction to sink thermal resistance (per switch) [1]		-	0.75	-	
DB1 - DB2 SILICON CARBIDE CLAMP DIODE - Junction to sink thermal resistance (per diode) [1]		-	2.35	-	
Case to sink thermal resistance (per module) [1]		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

[1] Mounting surface flat, smooth, and greased, λ_{grease} = 0.67 W/mK

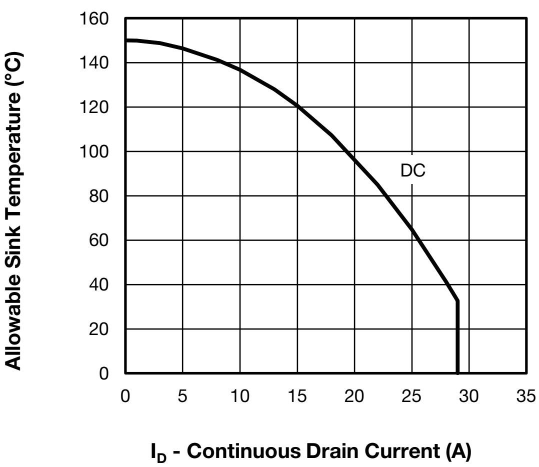


Fig. 1 - Maximum MOSFET Continuous Drain Current vs. Sink Temperature

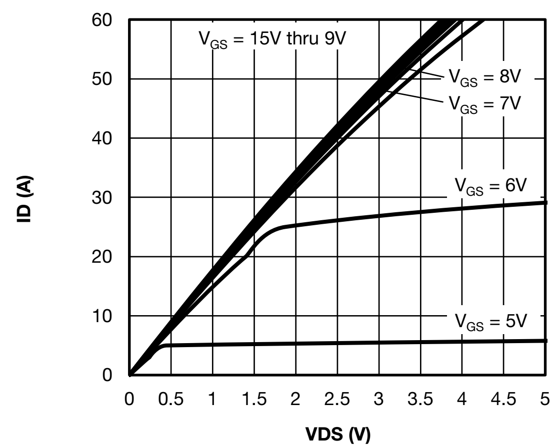


Fig. 3 - Typical MOSFET Drain-to-Source Current Output Characteristics at T_J = 25 °C

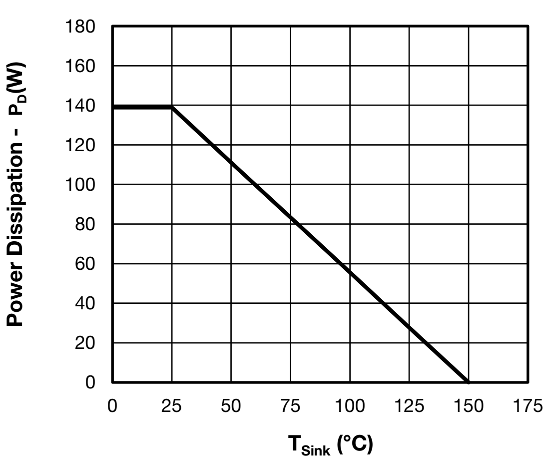


Fig. 2 - MOSFET Power Dissipation Curve

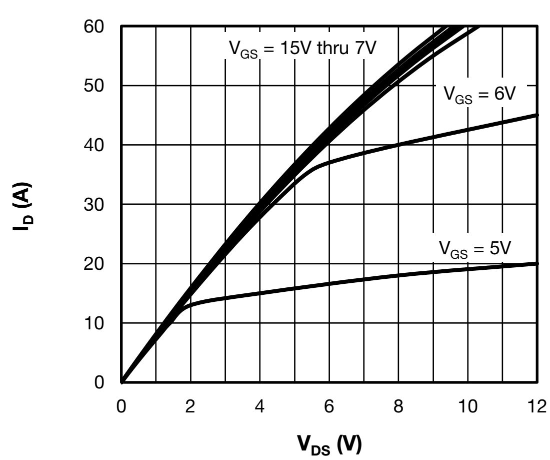


Fig. 4 - Typical MOSFET Drain-to-Source Current Output Characteristics at T_J = 150 °C

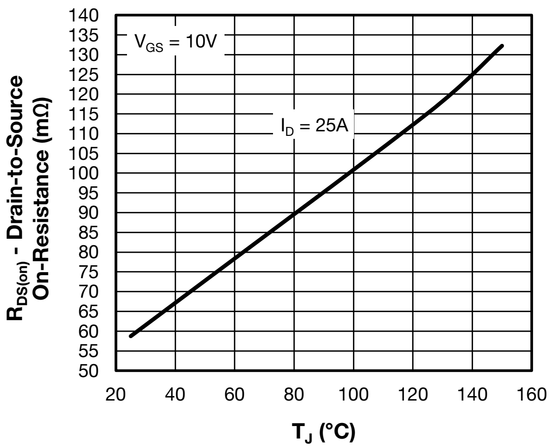


Fig. 5 - Typical MOSFET
Drain-to-Source On-Resistance vs. Temperature

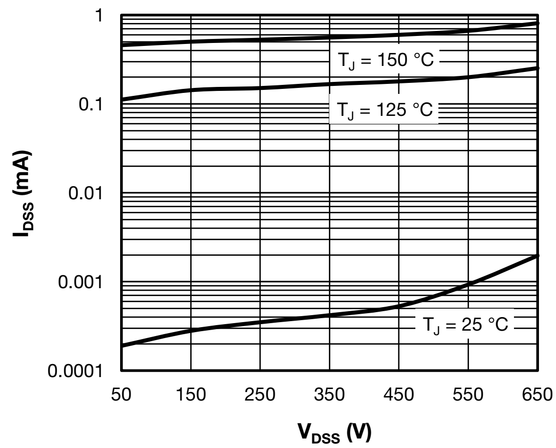


Fig. 8 - Typical MOSFET Zero Gate Voltage Drain Current

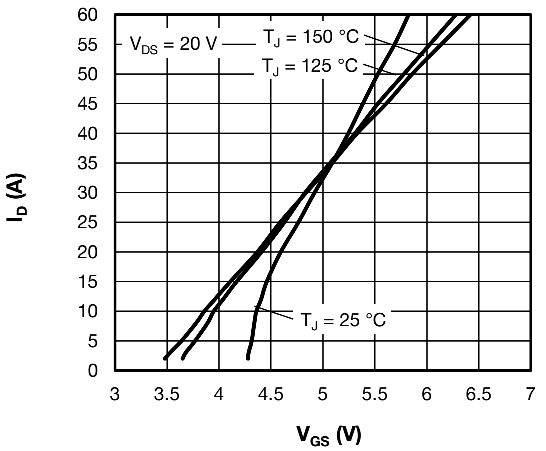


Fig. 6 - Typical MOSFET Transfer Characteristics

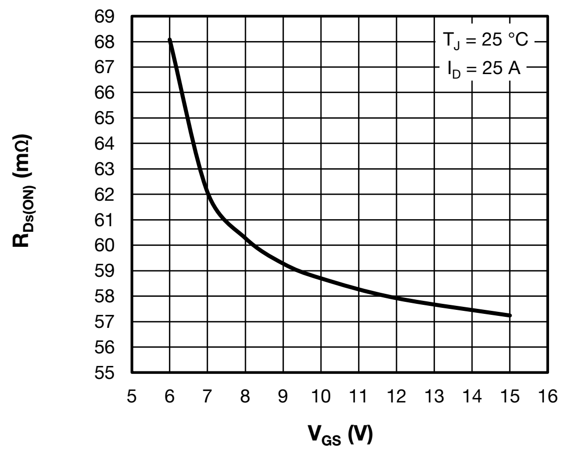


Fig. 9 - Typical MOSFET
Drain - State Resistance vs. Gate-to-Source Voltage

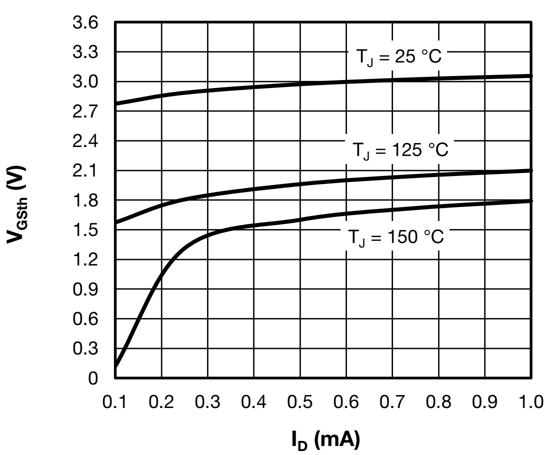


Fig. 7 - Typical MOSFET Gate Threshold Voltage Characteristics

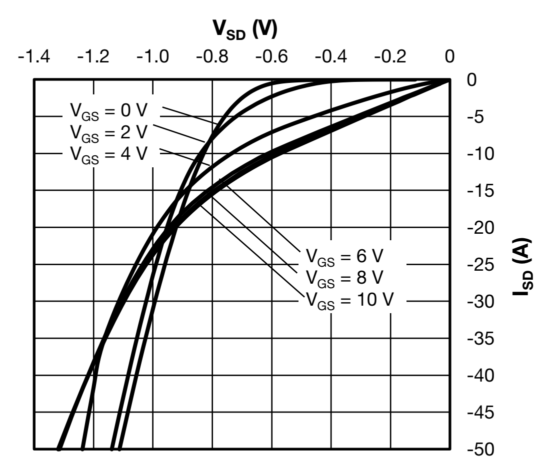


Fig. 10 - Typical MOSFET Source-to-Drain Current Characteristics at T_J = 25 °C

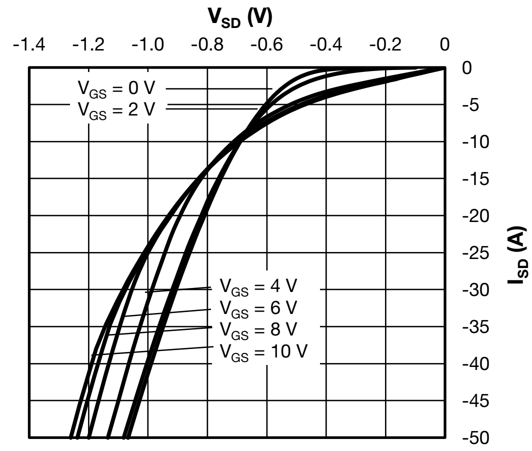


Fig. 11 - Typical MOSFET Source-to-Drain Current Characteristics at T_J = 125 °C

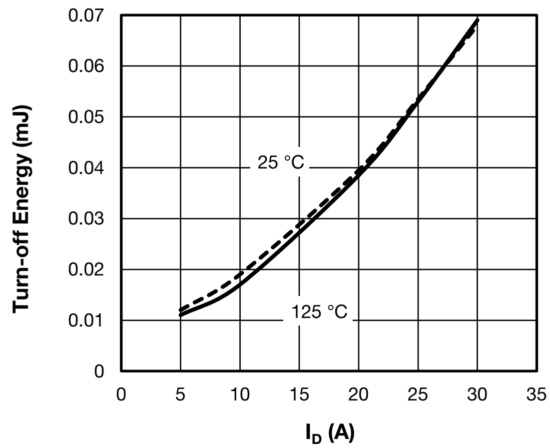


Fig. 14 - Typical Q1 to Q4 Turn-off Energy Loss vs. I_D
V_{DD} = 325 V, R_g = 4.7 Ω, V_{GS} = ± 10 V, L = 500 µH

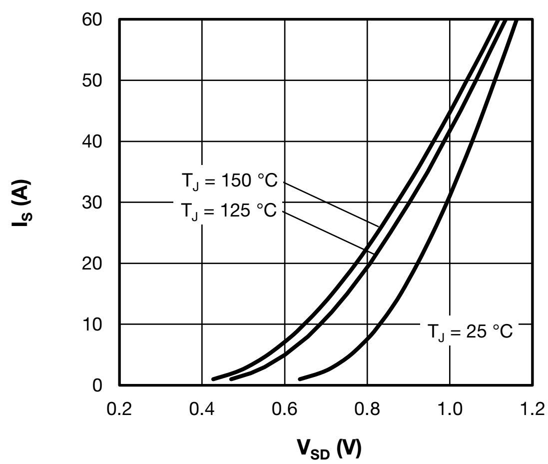


Fig. 12 - Typical MOSFET
Body Diode Source-to-Drain Current Characteristics

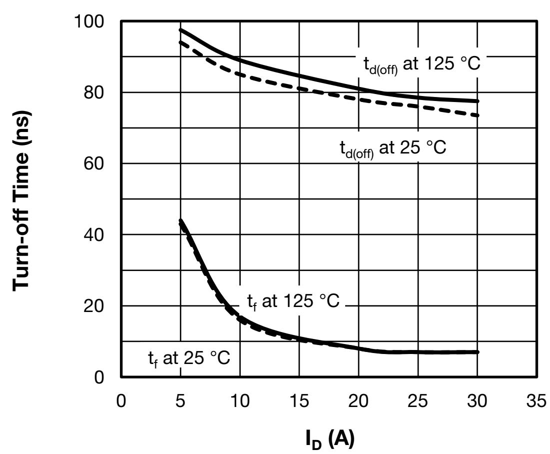


Fig. 15 - Typical Q1 to Q4 Turn-off Switching Time vs. I_D
V_{DD} = 325 V, R_g = 4.7 Ω, V_{GS} = ± 10 V, L = 500 µH

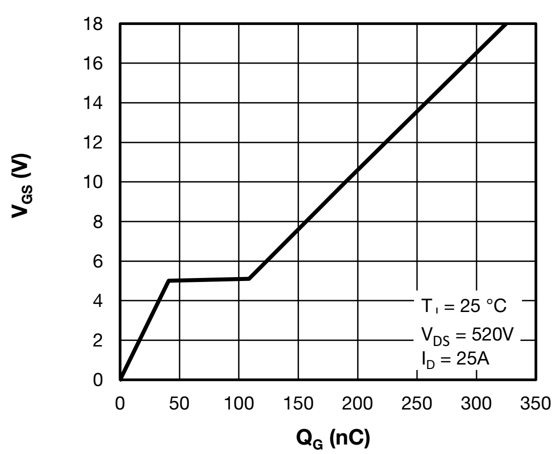


Fig. 13 - Typical MOSFET Gate charge vs. Gate-to-Source Voltage

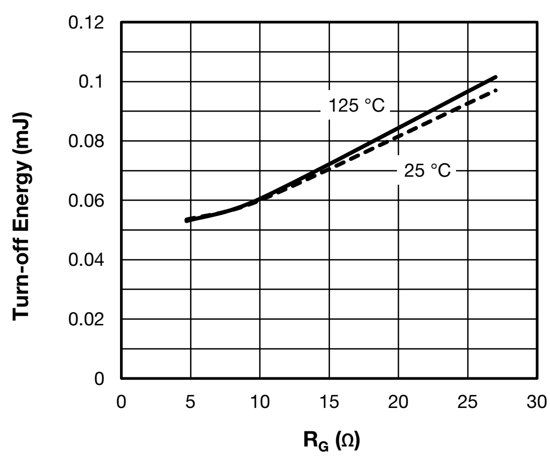


Fig. 16 - Typical Q1 to Q4 Turn-off Energy Loss vs. R_g
V_{DD} = 325 V, I_D = 25 A, V_{GS} = ± 10 V, L = 500 µH

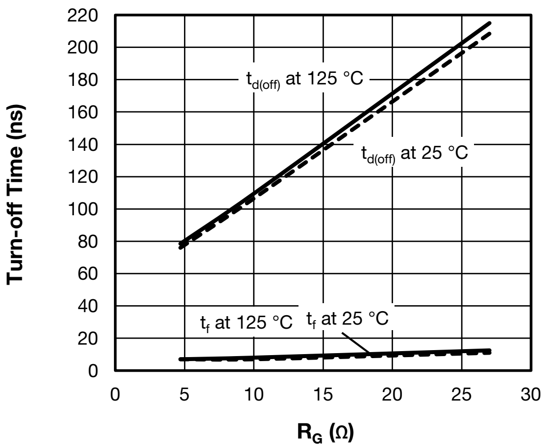


Fig. 17 - Typical Q1 to Q4 Turn-off Switching Time vs. R_g
V_{DD} = 325 V, I_D = 25 A, V_{GS} = ± 10 V, L = 500 µH

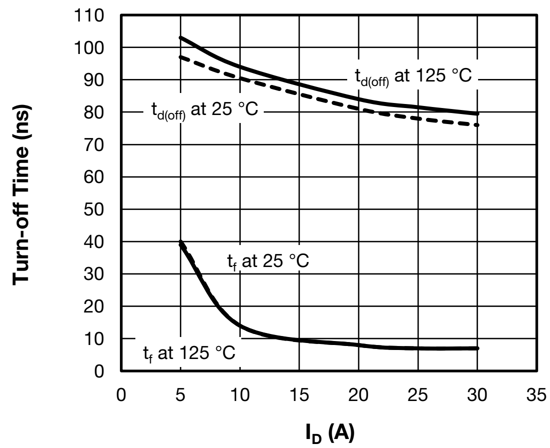


Fig. 20 - Typical QB1 to QB2 Turn-off Switching Time vs. I_D
V_{DD} = 325 V, R_g = 4.7 Ω, V_{GS} = ± 10 V, L = 500 µH

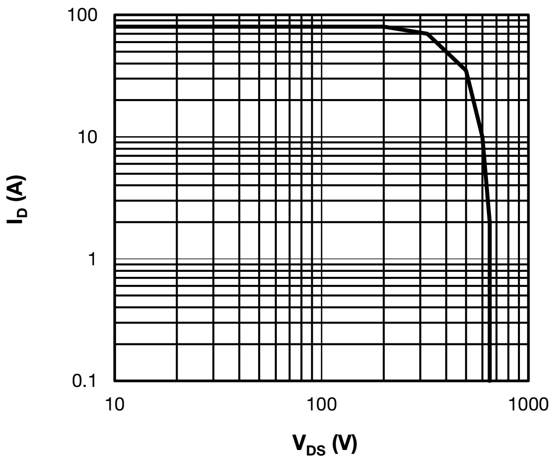


Fig. 18 - Q1 to Q4 Reverse BIAS SOA T_J = 150 °C, V_{GS} = 10 V

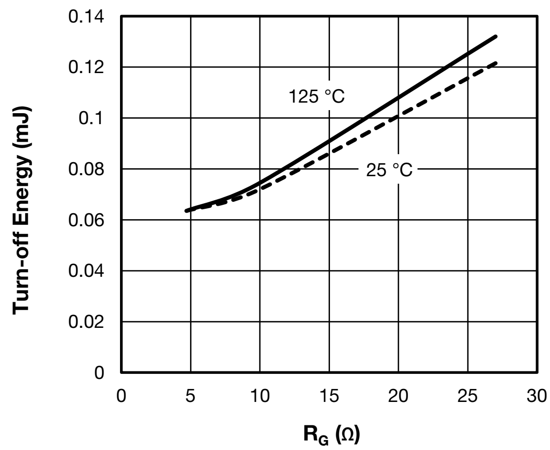


Fig. 21 - Typical QB1 - QB2 Turn-off Energy Loss vs. R_g

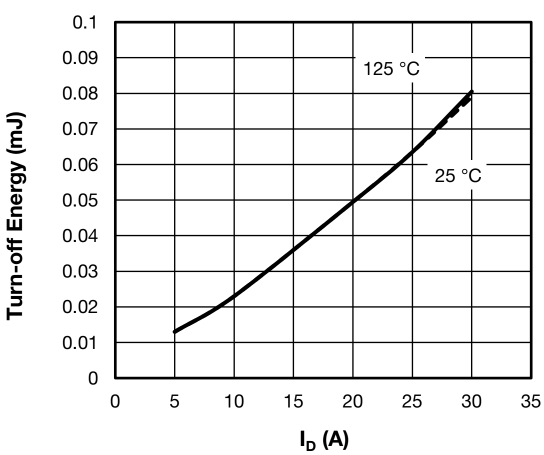


Fig. 19 - Typical QB1 - QB2 Turn-off Energy Loss vs. I_D
V_{DD} = 325 V, R_g = 4.7 Ω, V_{GS} = ± 10 V, L = 500 µH

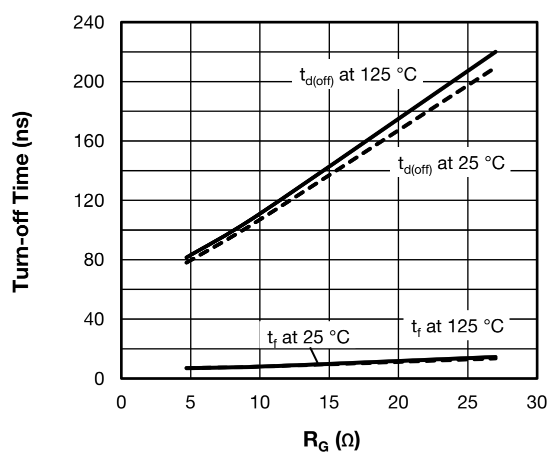


Fig. 22 - Typical QB1 - QB2 Turn-off Switching Time vs. R_g

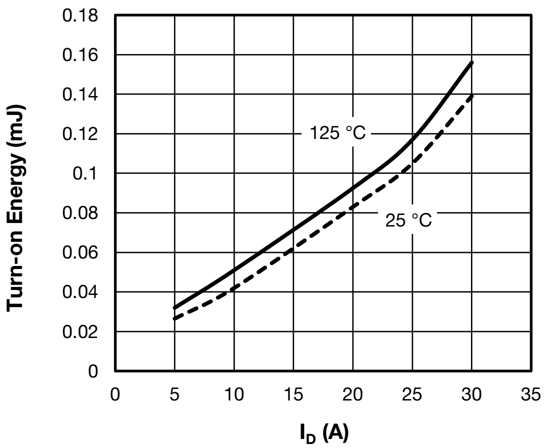


Fig. 23 - Typical QB1 - QB2 Turn-on Energy Loss vs. I_D
V_{DD} = 325 V, R_g = 4.7 Ω, V_{GS} = ± 10 V, L = 500 μH

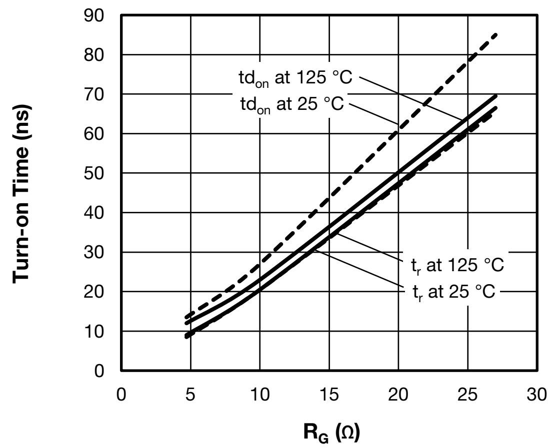


Fig. 26 - Typical QB1 - QB2 Turn-on Switching Time vs. R_g
V_{DD} = 325 V, I_D = 25 A, V_{GS} = ± 10 V, L = 500 μH

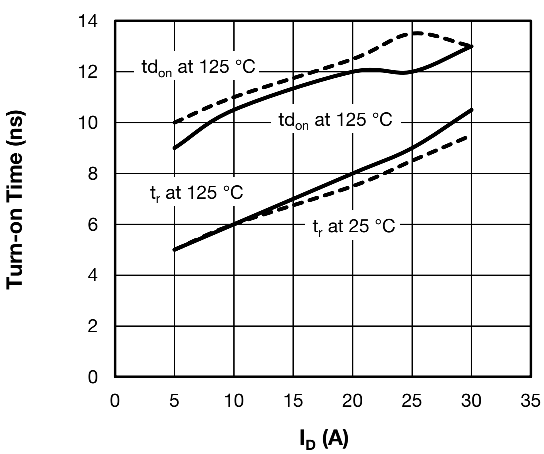


Fig. 24 - Typical QB1 - QB2 Turn-on Switching Time vs. I_D
V_{DD} = 325 V, R_g = 4.7 Ω, V_{GS} = ± 10 V, L = 500 μH

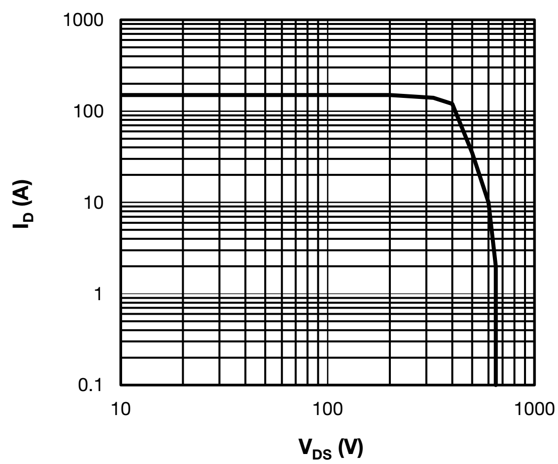


Fig. 27 - QB1 - QB2 Reverse BIAS SOA
T_J = 150 °C, V_{GS} = 10 V

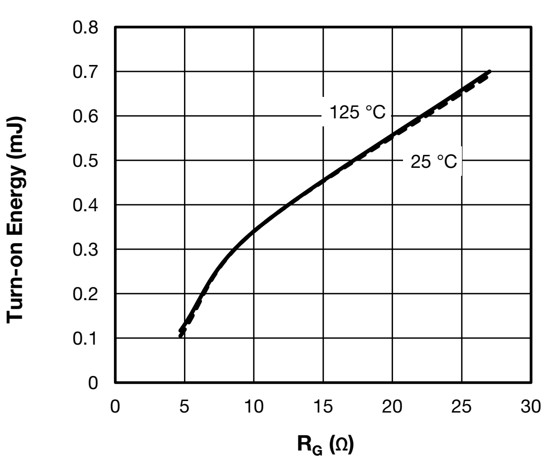


Fig. 25 - Typical QB1 - QB2 Turn-on Energy Loss vs. R_g
V_{DD} = 325 V, I_D = 25 A, V_{GS} = ± 10 V, L = 500 μH

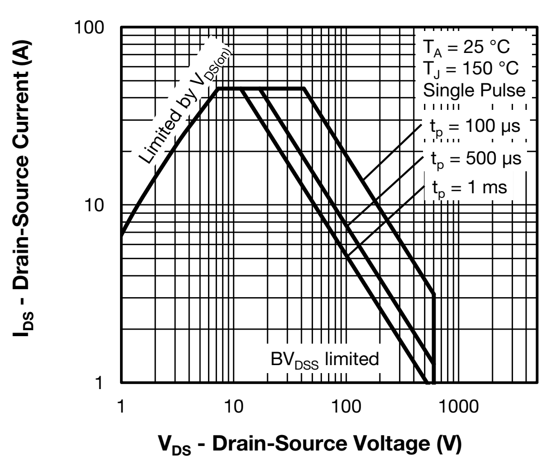


Fig. 28 - MOSFET Safe Operating Area

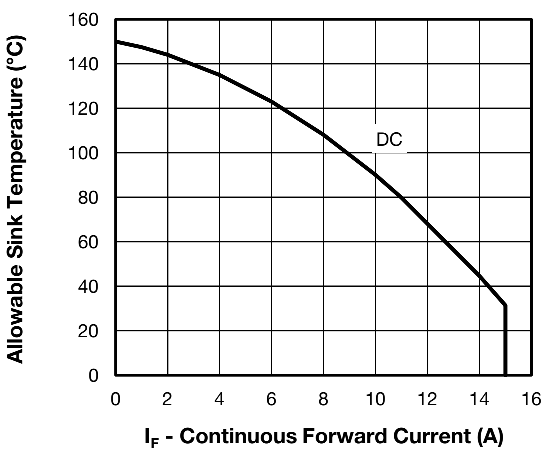


Fig. 29 - Maximum DB1 - DB2 Continuous Forward Current vs. Sink Temperature

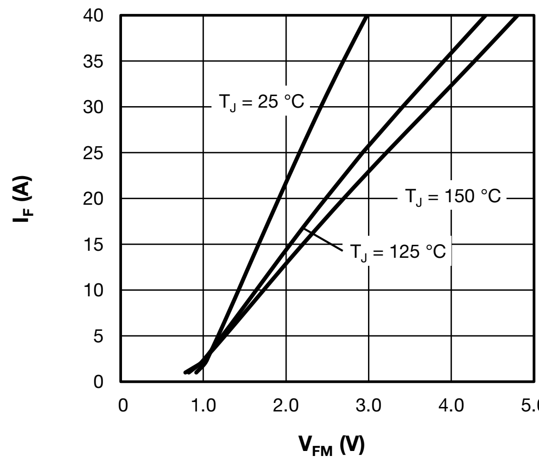


Fig. 30 - Typical DB1 - DB2 Diode Forward Characteristics

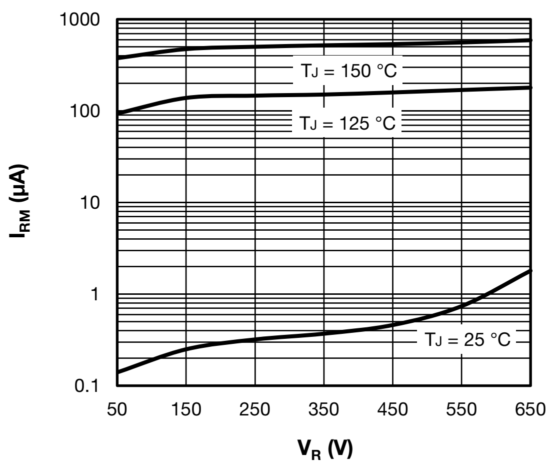


Fig. 31 - Typical DB1 - DB2 Reverse Leakage Current

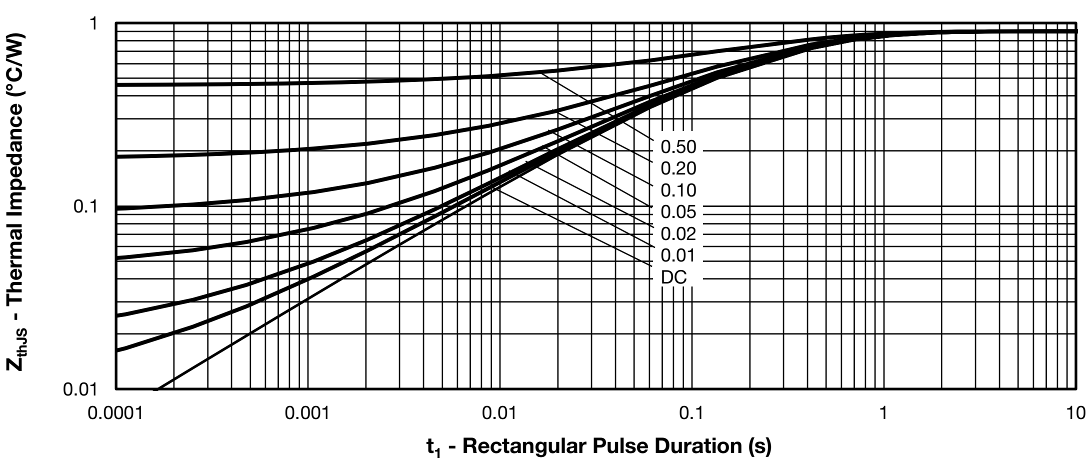


Fig. 32 - Maximum MOSFET Z_{thJS} Thermal Impedance Characteristics

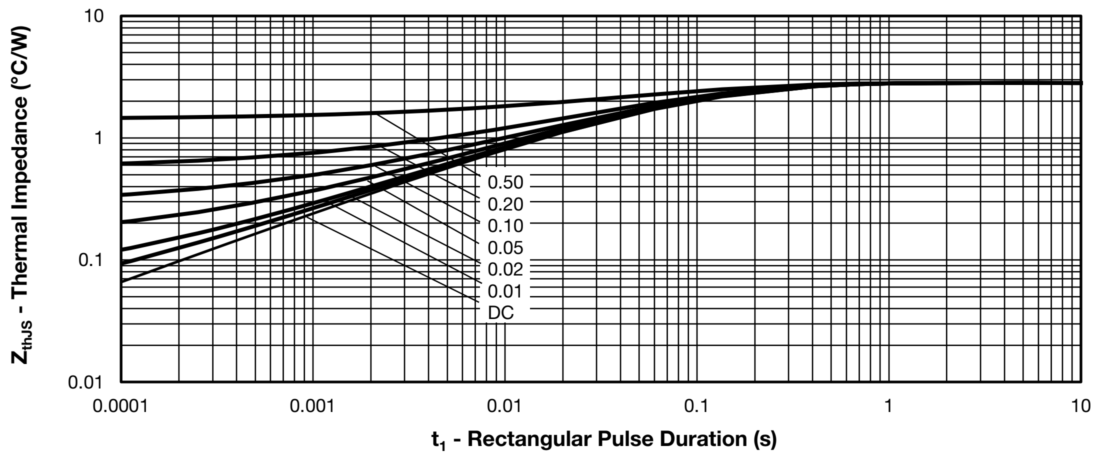
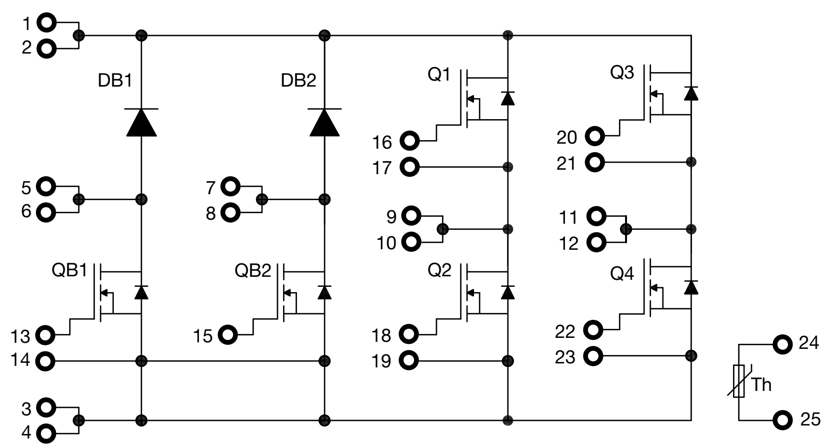


Fig. 33 - Maximum Diode Z_{thJS} Thermal Impedance Characteristic

ORDERING INFORMATION TABLE

Device code	VS-	EN	K	025	C	65	S
	1	2	3	4	5	6	7

1	-	Vishay Semiconductors product
2	-	Package indicator (EN = EMIPAK 1B)
3	-	Circuit configuration (K = MOSFET dual boost PFC and MOSFET full bridge inverter)
4	-	Current rating (025 = 25 A)
5	-	Switch die technology (C = PowerMOS)
6	-	Voltage rating (65 = 650 V)
7	-	Clamp diode technology (S = Silicon Carbide diode)

<table>
<tr><th colspan="3">CIRCUIT CONFIGURATION</th></tr>
<tr><th>CIRCUIT</th><th>CIRCUIT CONFIGURATION CODE</th><th>CIRCUIT DRAWING</th></tr>
<tr><td>MOSFET dual boost PFC and MOSFET full bridge inverter</td><td>K</td><td>


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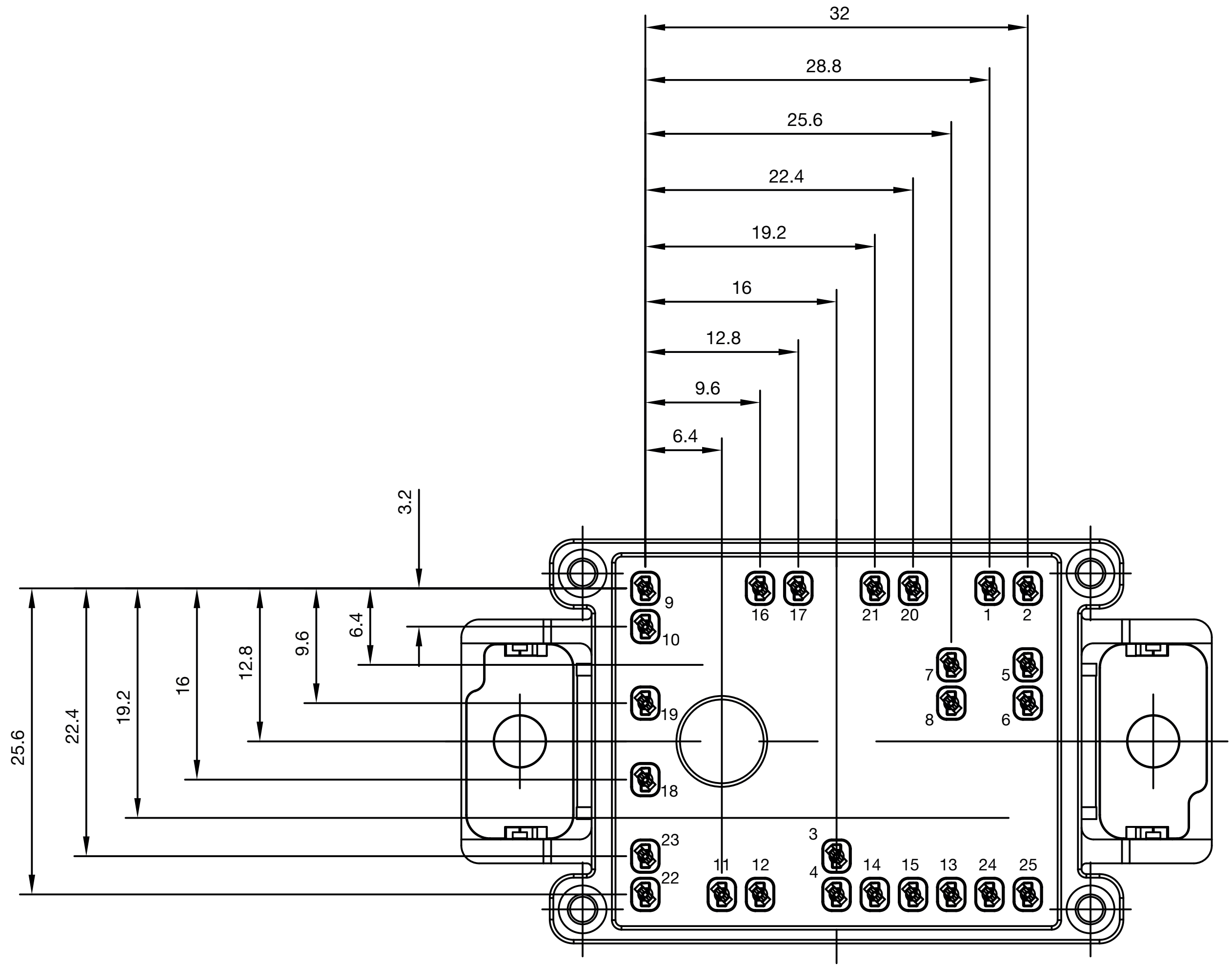
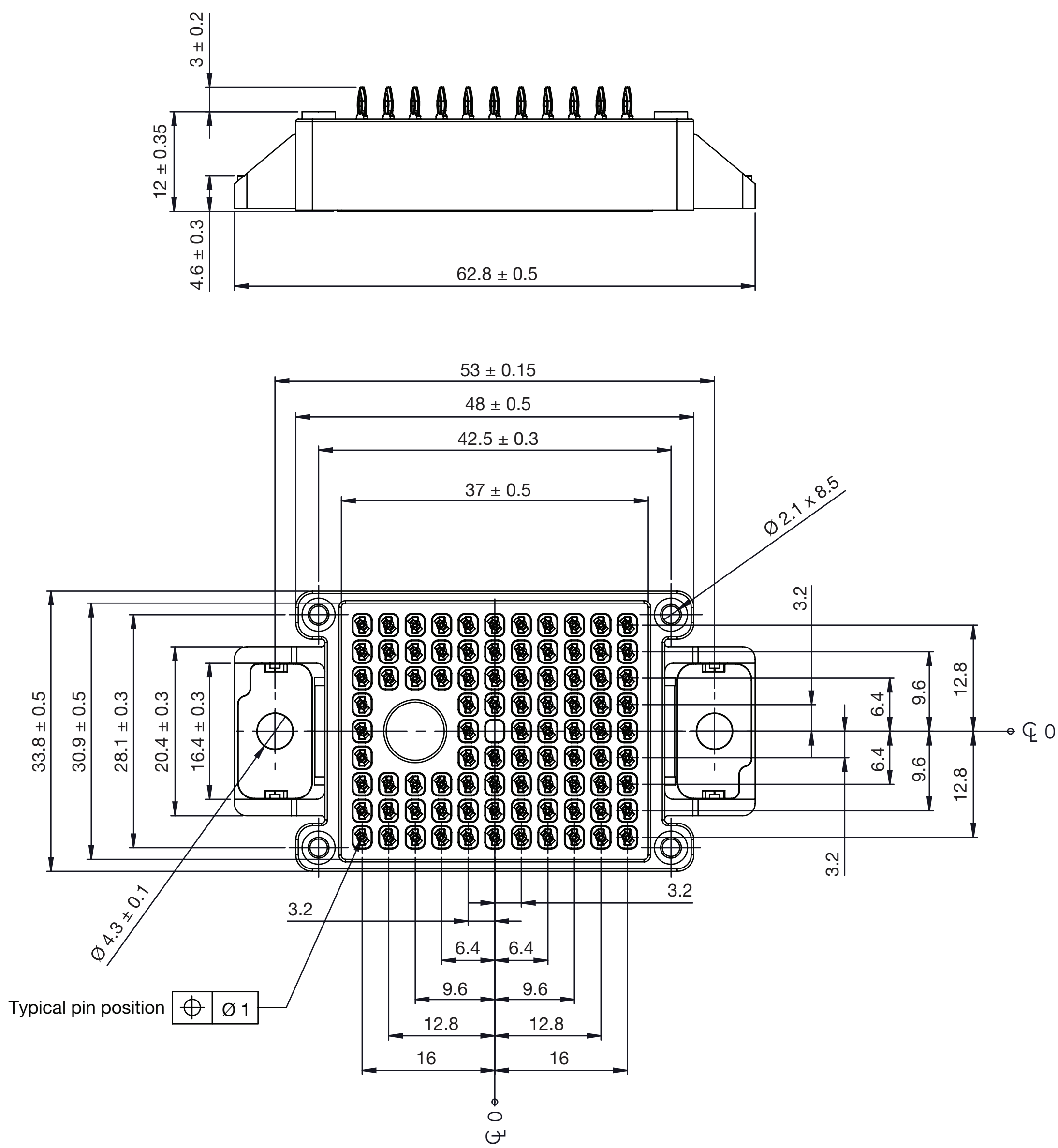
PACKAGE



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580

EMIPAK-1B PressFit

DIMENSIONS in millimeters



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