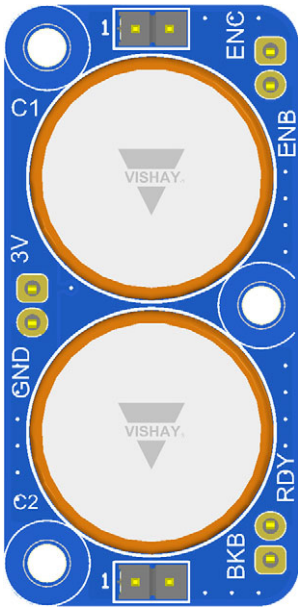
Reference Design
Circuit Providing Backup Power From an EDLC Super Capacitor



FEATURES

- Can supply high peak currents (1 A to 5 A peak inductor current limit)
- Super capacitor based backup circuit
- Low quiescent current

KEY COMPONENTS

- EDLC ENYCAP™ super capacitor
- IHLP0806 inductor
- T55 vPolyTan™ tantalum capacitors

APPLICATIONS

- Handheld equipment
- Portable devices with removable batteries
- Industrial sensor and actuators
- Aftermarket automotive tracking
- Energy storage for IoT devices
- Graceful shutdown of embedded systems

LINKS TO ADDITIONAL RESOURCES

- EDLCBU-3V3

DESCRIPTION

The EDLCBU-3V3 is a circuit providing backup power from an EDLC super capacitor to a 3.3 V circuit intended to bridge gaps in the power supply, such as while changing batteries, switching power sources, or allowing for a graceful shutdown after power loss.

Further, the circuit can be used to supply photovoltaic powered IoT nodes with energy during darkness or can provide the needed energy to tracking devices even after the main battery was disconnected.

To achieve these tasks, a buck-boost converter is used to interface between the EDLC's super capacitor energy storage and the 3.3 V rail of the application, charging the supercapacitor under normal operation and providing a stable voltage of 3 V during backup operation.

OVERALL SYSTEM BLOCK DIAGRAM

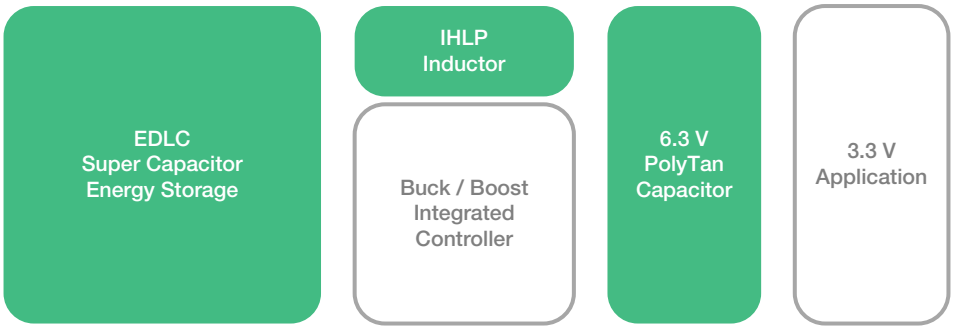


Fig. 1 - Overall System Block Diagram

APPLICATION DESCRIPTION

The EDLCBU-3V3 uses two (or more) parallel EDLC super capacitors to store energy in normal operation and to provide energy to the application during backup operation.

To achieve this task, the EDLC super capacitors and the 3.3 V rail of the protected circuit are connected via a buck-boost DC/DC converter based on the MAX38890 2.5 V to 5.5 V, 5 A reversible buck-boost regulator for backup applications and the IHLP0806ABEZR47M5A inductor.

As long as the system voltage VSYS is above 3.08 V the DC/DC converter charges the EDLC energy storage to a maximum voltage of 3 V using an average current of up to 2.5 A, reaching peak inductor currents of 5 A. If the system voltage VSYS drops below 3.08 V the DC/DC converter switches to backup mode and provides the energy stored in the EDLC to the system rail regulating the output to 3.0 V or the max. allowed current until the energy stored in the ELDC is expended.

The maximum EDLC charging and discharging current can be set using the trimmer R_{12} and determines the lowest voltage for the storage capacitor at which the DC/DC converter drops out.

The development kit offer access to all signal pins of the MAX38890 and can be mounted on standard bread boards. Further EDLCs can be added on J_4 and J_5, increasing the energy storage capability for prototyping purposes.

For an exact description of the DC/DC converter, its configuration options, and reset conditions, please consult the MAX38890 datasheet.

Under normal operating conditions the EDLC is charged up to 2.7 V and can be discharged down to 0.8 V. Therefore, the energy available to the system rail can be approximated by:

$$E = \frac{1}{2} \times C \times V^2 = C \times 0.5 \times (2.7^2 \times V^2 - 0.8^2 \times V^2) = C \times 3.325\ V^2$$

Should the DC/DC converter IC not allow the discharge down to 0.8 V (e.g., as can be the case when limiting the peak inductor current to low values), the accessible energy can be lower. In the best case the configuration is such that the IC discharges the capacitor down to 0.5 V, allowing for the of use more energy from the same capacitance value. The exact cut of voltage depends on the maximum allowed peak inductor current and load current. For more information, please consult the MAX38890 datasheet.

APPLICATION DESCRIPTION			
DEVELPMOMENT KIT VPN	**CAPACITOR VPN**	**CAPACITY**	**ENERY AVAILABLE**
3.3VEDLCMB050F (1)	-	2 x 25 F = 50 F	116.25 J
3.3VEDLCMB080F (1)		2 x 40 F = 80 F	266 J
3.3VEDLCMB100F (1)	MAL222091008E3	2x 50 F = 100 F	332.5 J
3.3VEDLCMB120F		2x 60 F = 120 F	399 J

Note

- Available on request

Higher capacitances can be prototyped by paralleling extra capacitors to the existing two capacitors using J_4 and J_5.

Time Available in Backup Mode

To calculate the time available in backup mode, it is best to use the worst case end of life capacitance of the chosen EDLC storage capacitor calculate the energy available to the DC/DC converter and then compare this to the energy consumption of the circuit to be operated in backup mode. While this neglects the efficiency of the DC/DC conversion step, it gives a good indication of the duration a certain application can be powered. Further, this allows arbitrary current waveforms to be considered, even rapidly changing current consumption flashing LEDs and MCUs, for example.

Current and Voltage Waveform Examples Using 2 x 40 F EDLCs

The following graph shows the system rail voltage VSYS and super capacitor voltage over time while in backup mode with a load of 4.7 Ω. The combined capacitance of 80 F is discharged over a 4.7 Ω load. The circuit holds the output voltage at 3 V, supplying 0.745 A to the load while the capacitor voltage drops from 2.7 V to around 0.7 V in about 140 s. In this condition the circuit is able to backup a 3 V / 745 mA load for over two minutes using two MAL222091001E3 capacitors in parallel.

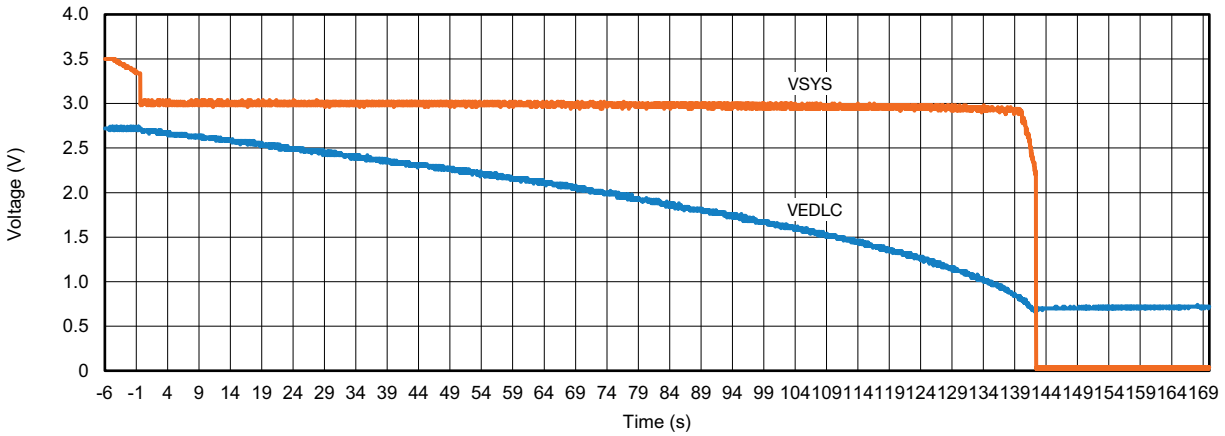


Fig. 2 - Backup Operation on 4.7 Ω Load

With a higher load impedance, the circuit discharges to lower voltages. With 6.5 Ω load and a peak inductor current setting of 5 A, the EDLC is discharged down to 0.55 V. The circuit supplies 0.5 A at 3.0 V for about 200 s before it drops out.

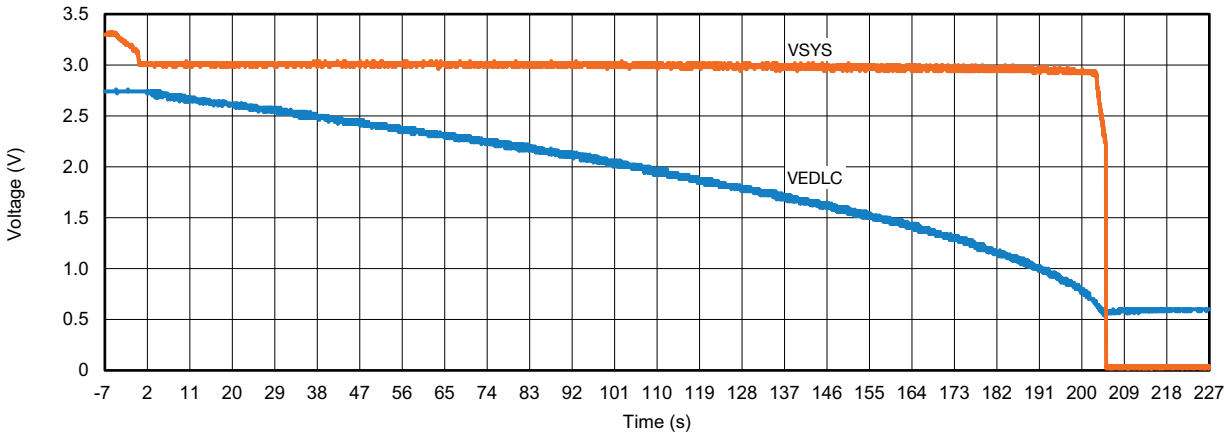


Fig. 3 - Backup Operation on 6.5 Ω Load

Set to minimum inductor current, charging of the 80 F of the EDLC capacitance requires approximately 440 s.

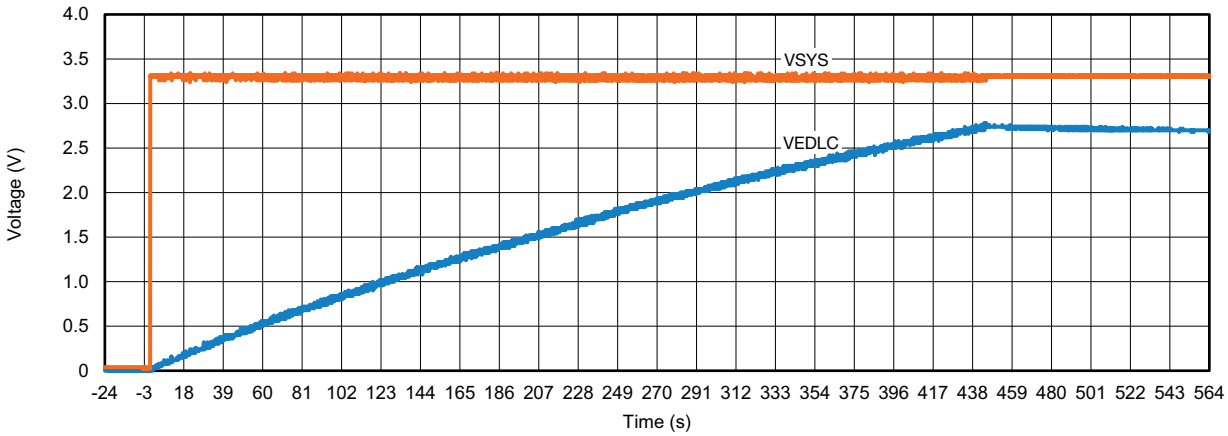


Fig. 4 - Charging at Minimum Peak Inductor Current

When set to maximum peak inductor current, the charging time decreases to about 90 s, as seen in the following graph. Alongside the charging curve, the graph shows the IC recharging the capacitor to maintain the capacitor voltage compensating resistance parallel to the capacitor such as voltage dividers, IC current draw, and leakage resistance.

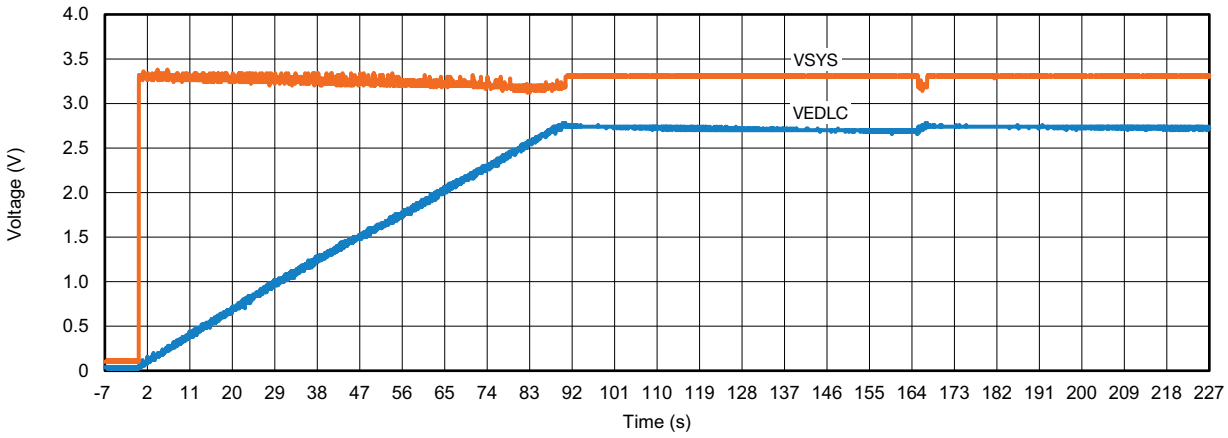


Fig. 5 - Charging at Maximum Peak Inductor Current

PIN CONFIGURATION

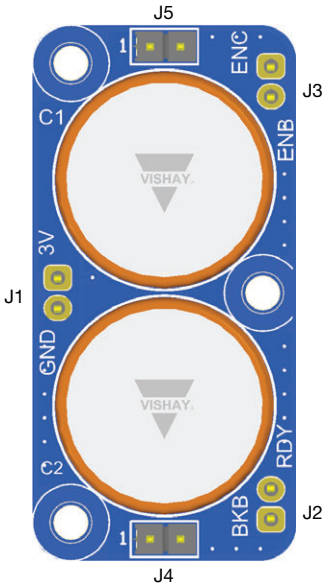


Fig. 6 - EDLCBU-3V3 Top

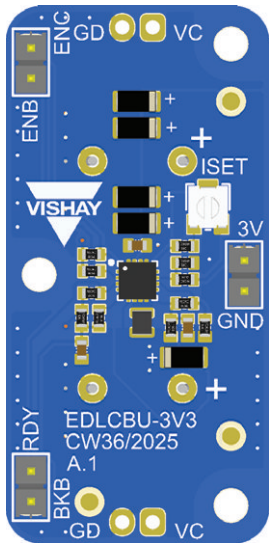


Fig. 7 - EDLCBU-3V3 Bottom

PIN DESCRIPTION		
PIN NUMBER	**NAME**	**DESCRIPTION**
J1/1	3 V	VSYS
J1/2	GND	GND
J2/1	BKB	Backup active
J2/2	RDY	Capacitors charged ready
J3/1	EN_B	Enable
J3/2	EN_C	Enable
J4/1	V_C	+ additional capacitor
J4/2	GND	GND additional capacitor
J5/1	V_C	+ additional capacitor
J5/2	GND	GND additional capacitor

Electrical Ratings

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise noted)				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
VSYS (backup operation)	2.5	3	-	V
VSYS (capacitor charging / ready state)	3.08	3.3	5.5	V
Average current	-	-	2.5	A
Peak inductor current	1	5	5	A
Quiescent current in ready state	-	4	-	µA

For absolute maximum ratings of the components, please consult their datasheets.

ADDITIONAL RESOURCES

220 EDLC ENYCAP™

MAX38890

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