High Voltage Ceramic Capacitors Radial-Leaded Singlelayer Disc

QUICK REFERENCE DATA	
DESCRIPTION	**VALUE**
Ceramic class	1
Ceramic dielectric	T3M
Temperature coefficient of capacitance	-4700 ppm/°C ± 1000 ppm/°C
Voltage ($U_{rated, DC}$)	15 000
Min. capacitance (pF)	100
Max. capacitance (pF)	1000
Capacitance tolerance	± 10 %
Max. dissipation factor (%)	1.0 at 1 kHz; 1.5 at 100 kHz
Min. insulation resistance (GΩ)	200 at 500 V_{DC}, 60 s
Operating temperature (°C)	-30 to +105
Mounting	Radial

RATED VOLTAGE

$U_{rated, AC} = U_{rated, DC}/2.8$ at 50 Hz / 60 Hz
$U_{rated, DC}$: 15 000 V; $U_{rated, AC}$: 5300 V

INSULATION RESISTANCE

Min. 200 000 MΩ at 500 V_{DC} / 60 s max.

TOLERANCE ON CAPACITANCE

± 10 %

DISSIPATION FACTOR

Max. 1.0 % at 1 kHz, 1.5 % at 100 kHz

OPERATING TEMPERATURE RANGE

-30 °C to +105 °C

FEATURES

- Ceramic singlelayer DC disc / AC disc capacitor
- High reliability
- High capacitance values up to 1 nF
- Low DC bias
- Low losses
- Radial leads
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb
e3
RoHS
COMPLIANT

APPLICATIONS

- High voltage power supplies for x-ray sources and pulsed lasers
- Baggage scanner
- Medical x-ray
- Industrial laser
- Airpurifier / ionizer

DESIGN

The capacitors consist of a ceramic disc of which both sides are silver-plated. Connection leads are made of tinned copper clad steel wire having diameters of 0.026" (0.65 mm) and 0.032" (0.80 mm).

The capacitors may be supplied with straight leads having lead spacing of 0.37" (9.5 mm) and 0.49" (12.5 mm).

Coating is made of flame retardant epoxy resin in accordance with “UL 94 V-0”.

CAPACITANCE RANGE

100 pF to 1000 pF

DIELECTRIC STRENGTH BETWEEN LEADS

1.5 x $U_{rated, DC}$ for maximum 60 s

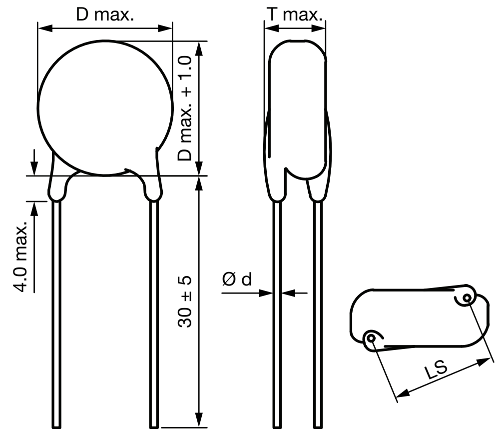
Notes

- Considered as destructive test in insulation liquid
- Avoid flashover between wires and currents higher than 50 mA

CERAMIC DIELECTRIC

T3M (N4700: -4700 ppm/°C ± 1000 ppm/°C)

DIMENSIONS in millimeters

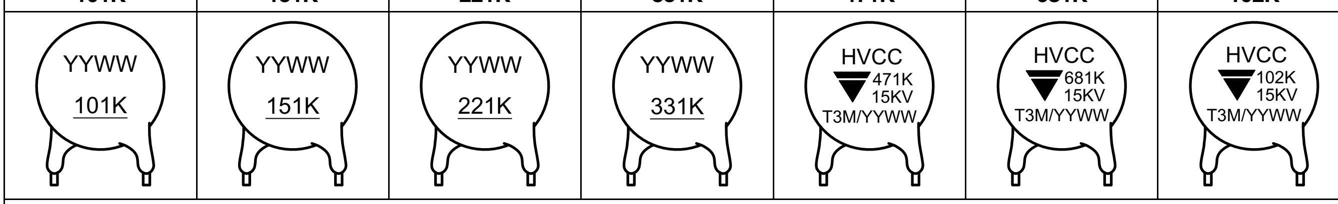


ORDERING INFORMATION

C (pF)	TOL. (%)	MAXIMUM BODY DIAMETER "D"	MAXIMUM BODY THICKNESS "T"	LEAD SPACE "LS" (± 1 mm)	WIRE DIAMETER "Ø d" (± 0.05 mm)	LEAD LENGTH (± 5 mm)	ORDERING CODE
		mm	mm	mm	mm	mm	
100	± 10	8.0	8.2	9.5 or 12.5	0.65 or 0.80	30	HVCC153T3M101K###
150	± 10	9.0	8.2				HVCC153T3M151K###
220	± 10	10.0	8.2				HVCC153T3M221K###
330	± 10	12.0	8.2				HVCC153T3M331K###
470	± 10	13.0	8.2				HVCC153T3M471K###
680	± 10	15.0	8.2				HVCC153T3M681K###
1000	± 10	18.0	8.2				HVCC153T3M102K###

MARKING

101K	151K	221K	331K	471K	681K	102K



YY: YEAR; WW: WEEK

ORDERING CODE

H	V	C	C	1	5	3	T	3	M	1	0	2	K	E	A	X
1				2			3			4			5	6		7

1	2	3	4	5	6	7
SERIES (**H**IGH **V**OLTAGE **C**ERAMIC **C**APACITOR)	RATED VOLTAGE	TEMPERATURE CHARACTERISTICS	CAPACITANCE VALUE	CAPACITANCE TOLERANCE	1st DIGIT: LEAD TYPE / LEAD SPACING / GAUGE 2nd DIGIT: LEAD LENGTH	PACKAGING

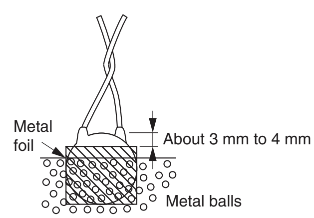
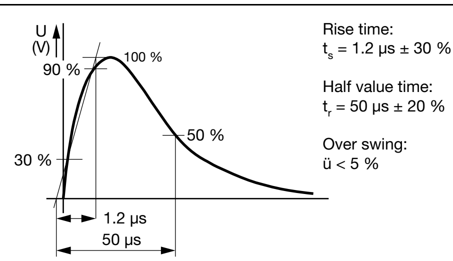
LEAD TYPE (position 6)

STANDARD TYPE						
CODE	**LEAD TYPE**	**LEAD SPACING (mm)**	**LEAD DIAMETER (mm)**	**# GAUGE**	**MATERIAL**	**LEAD LENGTH (mm)**
CA	Straight LL	9.5 ± 1.0	0.65	22	TCCSW	30 ± 5
EA	Straight LL	12.5 ± 1.0	0.80	20	TCCSW	30 ± 5

Notes

- 1th digit: lead type / lead spacing / gauge
  2nd digit: A = long leads
- LL = long leads
- TCCSW = **t**inned **c**opper **c**lad **s**teel **w**ire

PACKAGING (position 7)	
CODE	**VERSION**
X	Bulk

<table>
<tr><th colspan="5">PERFORMANCE</th></tr>
<tr><th rowspan="2">NO.</th><th rowspan="2" colspan="2">PARAMETER</th><th colspan="2">SPECIFICATION</th></tr>
<tr><th>TEST CONDITIONS</th><th>METHOD AND NOTES</th></tr>
<tr><td>1</td><td colspan="2">Appearance and marking</td><td>No visible damage.
The marking shall be legible</td><td>Visual inspection</td></tr>
<tr><td>2</td><td colspan="2">Dimensions</td><td>Dimensions are within specification</td><td>Measurement by caliper gauge</td></tr>
<tr><td>3</td><td colspan="2">Capacitance</td><td>Within tol. K = ± 10 %</td><td>Measure at 25 °C with 1 kHz and 5 V_{AC} (RMS) max., no aging</td></tr>
<tr><td>4</td><td colspan="2">Dissipation factor</td><td>DF = 1.0 % max. at 1 kHz
DF = 1.5 % max. at 100 kHz</td><td>Measure at 25 °C and 5 V_{AC} (RMS) max.</td></tr>
<tr><td>5</td><td colspan="2">Insulation resistance (between lead wires)</td><td>I_R = 200 GΩ min.</td><td>Measure at 500 V_{DC} ± 50 V_{DC} within 60 s of charging</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">Dielectric strength</td><td>Between lead wires</td><td>No failure at 1.5 x U_R, 60 s</td><td>Apply DC voltage between the lead wires in insulation liquid or gas (charge / discharge current ≤ 50 mA)</td></tr>
<tr><td>Body insulation</td><td>No failure at 5000 V_{DC}, 60 s</td><td>Connect lead wires together, dip capacitor head first into a bath with oil and metal balls (fig.), apply voltage between lead wires and metal balls. (charge / discharge current ≤ 50 mA)

</td></tr>
<tr><td>7</td><td colspan="2">Pulse test</td><td>No failure at 15 kV
n = 50 x single polarity</td><td>
</td></tr>
<tr><td rowspan="3">8</td><td rowspan="3">Solderability</td><td>Appearance</td><td>No marked defect</td><td rowspan="3">Solder temperature max 250 °C, dwell time max. 3 s
Distance of solder-epoxy min. 2 mm
Post-treat: capacitor shall be stored for 24 h ± 2 h at room condition.
(charge / discharge current ≤ 50 mA)</td></tr>
<tr><td>Capacitance change</td><td>Within ± 10 %</td></tr>
<tr><td>Dielectric strength (between lead wires)</td><td>No failure at 1.5 x U_R, 60 s</td></tr>
</table>

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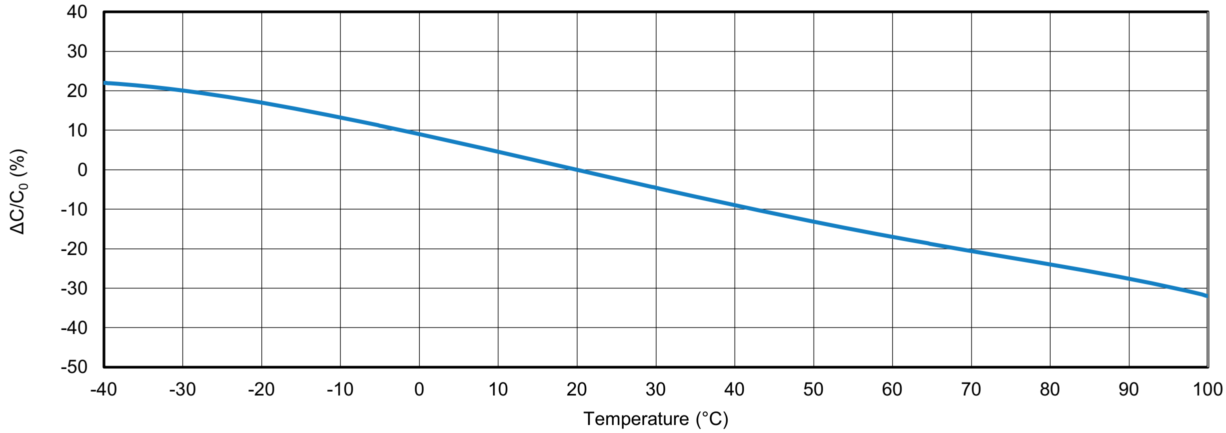
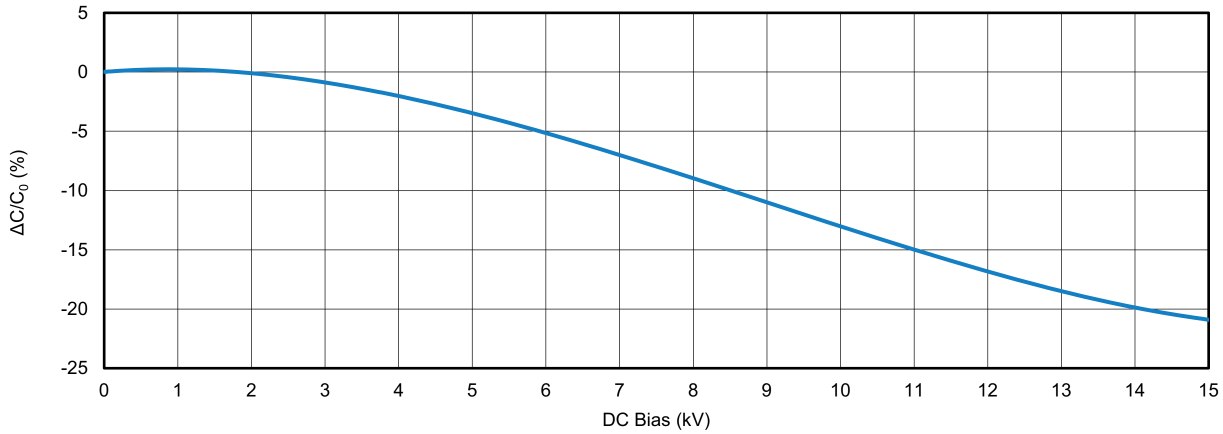
<tr><th>TEST CONDITIONS</th><th>METHOD AND NOTES</th></tr>
<tr><td>9</td><td colspan="2">Temperature characteristics / TCC</td><td>EIA code = T3M
(-4700 ppm/°C ± 1000 ppm/°C)</td><td>The capacitance measurement shall be made at step 1 to 3. Capacitance change from step 1 shall not exceed the limit specified.
<table><tr><td>Step</td><td>1</td><td>2</td><td>3</td></tr><tr><td>Temperature</td><td>25 °C</td><td>85 °C</td><td>25 °C</td></tr></table></td></tr>
<tr><td>10</td><td colspan="2">Temperature cycle</td><td>No crack in coating
No failure at 1.5 x U_R, 60 s</td><td>Unpowered, n = 50 cycles
-30 °C, 15 min / +105 °C, 15 min
Transition time: 1 min max.</td></tr>
<tr><td rowspan="5">11</td><td rowspan="5">Life</td><td>Appearance</td><td>No marked defect</td><td rowspan="5">Apply a DC voltage of 125 % of the rated voltage for 1000 (+24 / 0) h in silicon oil at 105 °C.
Post-treat: capacitor shall be stored for 24 h ± 2 h at room condition.
(charge / discharge current ≤ 50 mA)</td></tr>
<tr><td>Capacitance change</td><td>Within ± 10 %</td></tr>
<tr><td>DF</td><td>1.5 % max.</td></tr>
<tr><td>IR</td><td>100 GΩ min.</td></tr>
<tr><td>Dielectric strength (between lead wires)</td><td>No failure at 1.5 x U_R, 60 s</td></tr>
<tr><td rowspan="5">12</td><td rowspan="5">Steady state test (without load)</td><td>Appearance</td><td>No marked defect</td><td rowspan="5">Set the capacitor for 500 h +48 h / -0 h at 40 °C ± 2 °C / 93 % ± 3 %RH.
Post-treat: capacitor shall be stored for 1 h to 2 h at room condition.
(charge / discharge current ≤ 50 mA)</td></tr>
<tr><td>Capacitance change</td><td>Within ± 10 %</td></tr>
<tr><td>DF</td><td>1.5 % max.</td></tr>
<tr><td>IR</td><td>100 GΩ min.</td></tr>
<tr><td>Dielectric strength (Between lead wires)</td><td>No failure at 1.5 x U_R, 60 s</td></tr>
<tr><td>13</td><td colspan="2">Strength of lead wire / pulling</td><td>No lead wire broken</td><td>Fix the body of component, apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10 N, and keep it for 10 s ± 1 s</td></tr>
<tr><td>14</td><td colspan="2">Strength of lead wire / bending</td><td>No lead wire broken</td><td>Bending each lead wire to 90° from the lead egress with 2.5 N force, then back to original position, and bent again from the same direction. Totally 3 bends, 3 s each time.
1 bend: bending to 90° the return to normal position is one bend. Start from 1.6 mm to 3.2 mm from the part body</td></tr>
</table>

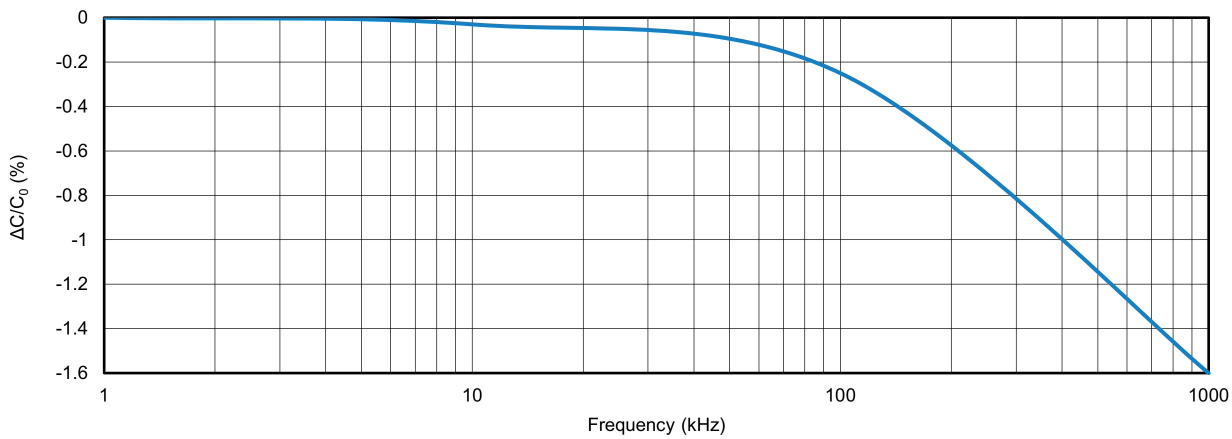
TYPICAL TCC T3M



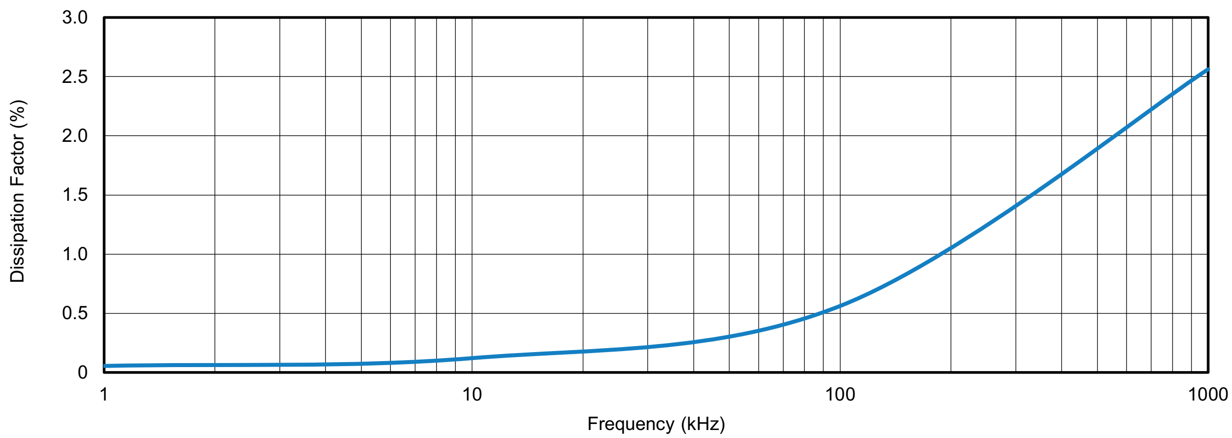
TYPICAL T3M - $\Delta C/C_0$ / % VS. $U_{rated,\ DC}$



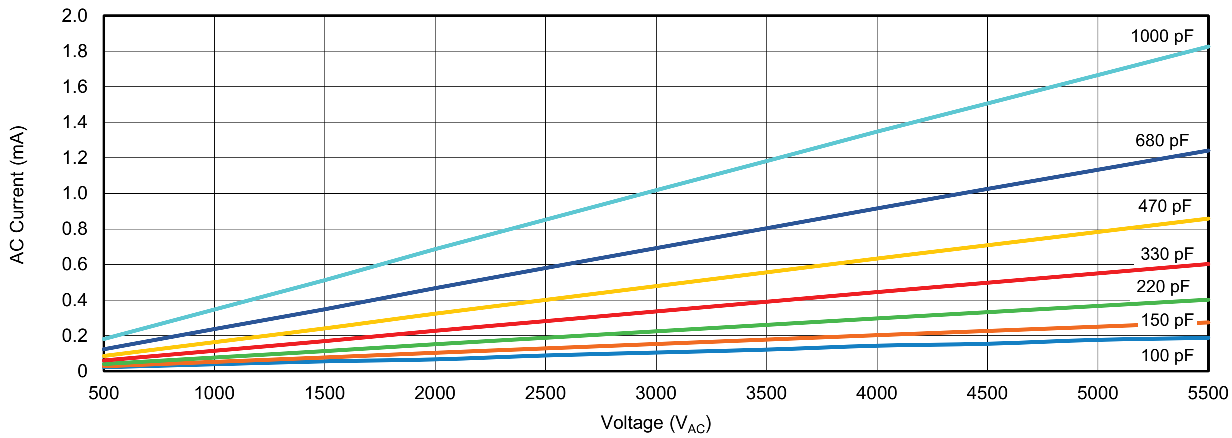
TYPICAL Y6P - $\Delta C/C_0$ / % VS. FREQUENCY



TYPICAL T3M DF VS. FREQUENCY



TYPICAL AC CURRENT VS. APPLIED VOLTAGE



1. QUALIFICATION

1.1 BASICS

Series is released according to type test with performance indication according to this datasheet. End of life tests are performed to confirm reliability beyond the performance indicators. We do not guarantee if any rated limits are exceeded.

Each production batch is released by lot tests as well as 100 % item tests to check on capacitance, dissipation factor, insulation resistance, and high voltage withstand ability. If you are interested in more details, please contact the factory slcap@vishay.com

1.2 LIMITS OF APPLICATION

Please take care whilst designing our parts into one of these applications, which require highest reliability and possible errors might harm life, body, or property of a third party.

- Transportation (aerospace, aircraft, train, ship, submarine, etc.)
- Medical equipment
- Critical control equipment (power plant, traffic signals, disaster prevention)
- Other application requiring similar reliability characteristics

2. STORAGE

2.1 ORIGINAL PACKAGING

Storing in the sealed original packages is preferred.

2.2 STORING CONDITIONS

Epoxy coating does not protect perfectly from all environmental conditions. Some materials can penetrate the epoxy and harm the performance of the parts. Therefore it is not recommended to use or store the parts in corrosive or humid atmosphere.

Optimal storing conditions should not exceed +10 °C to +35 °C and relative humidity up to 60 %.

3. ASSEMBLY

3.1 WIRE FORMING

If wire forming is needed, excessive mechanical force to the component body must be avoided as it might cause cracks in the ceramic element.

Do not crack coating extension of the epoxy layer, when applying force onto the wire.

3.2 SOLDERING

For best performance it is recommended to dry the components at 125 °C for 2 h before assembly.

Do not exceed resistance to soldering heat specification of the component. Subjecting this product to excessive heating could melt the internal junction solder and may result in thermal shocks that can crack the ceramic element.

Manual Soldering / Rework

Set the soldering iron (50 W max.) to less than 400 °C and solder the wires within 4 s onto the PCB. Exceeding that recommendations might reduce the electrical performance of the component.

Wave Soldering

Most common way to assemble these kind of components is carried out in 4 steps:

1. Increasing temperature to 120 °C within about 20 s
2. Preheating at 120 °C for about 60 s
3. Soldering at 260 °C in less than 10 s
4. Gradual air cooling in constant air flow

Reflow Soldering

It is not recommended to use reflow soldering with these components.

3.3 MOLDING AND COATING

Molding and / or applying another coating material might harm the performance of the components. Therefore it is recommended to test the electrical characteristics of the molded / coated part in advance.

Typical error is a reduced withstand voltage because of an inadequate solvent in the molding material, which penetrates the epoxy coating (please see recommendations for cleaning and drying in section 4.1 to 4.3). A similar result can be caused by an inadequate coating material, which might pull the original epoxy off the ceramic element.

4. CLEANING AND DRYING

4.1 CLEANING AGENTS

Cleaning agents might have an influence to the performance of the components after washing and after unsuitable drying. The following agents have been tested and classified:

Recommended

- DI water
- Isopropanol
- Ethanol
- Ehtyl alcohol
- ...

Not Recommended

- Acetone
- ...

4.2 ULTRASONIC

Settings for ultrasonic cleaning

Rinse bath capacity: output of 20 W per liter or less

Rinsing time: 5 min max.

Do not vibrate the PCB / PWB directly.

Excessive ultrasonic cleaning may lead to permanent destruction of the component.

4.3 DRYING

In case of cleaning the assembled PCB with cleaning agents a proper drying is recommended. It is recommended to properly insulate the assembled PCB (see section 5.2) after drying.

5. TESTING AND OPERATION

5.1 SHORT CIRCUIT

Avoid repetitive zero-ohm-short circuits because they might harm the components core construction, such as arcs between lead wires because of inadequate insulation material (e.g air).

5.2 INSULATION

During operation, components should be surrounded by adequate insulating material (silicone oil, epoxy or molding material). Voltage breakdowns or leakage current through this material (between lead wires or to ground) is not acceptable. It is recommended to properly clean and dry the assembled PCB (see section 4.1 to 4.3) before enclosing in insulating material.

5.3 APPLIED VOLTAGE

When using DC-rated components in AC applications (also ripple) the peak to peak voltage should not exceed the nominal DC-rating of the component.

6. CAUTION

6.1 OPERATING VOLTAGE AND FREQUENCY CHARACTERISTIC

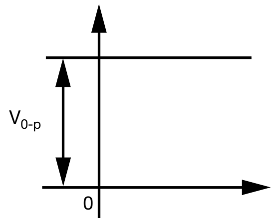
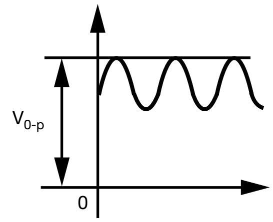
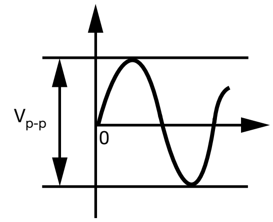
When sinusoidal or ripple voltage applied to DC ceramic disc capacitors, be sure to maintain the peak-to-peak value or the peak value of the sum of both AC + DC within the rated voltage.

When start or stop applying the voltage, resonance may generate irregular voltage.

When rectangular or pulse wave voltage is applied to DC ceramic disc capacitors, the self-heating generated by the capacitor is higher than the sinusoidal application with the same frequency. The allowable voltage rating for the rectangular or pulse wave corresponds approximately with the allowable voltage of a sinusoidal wave with the double fundamental frequency.

The allowable voltage varies, depending on the voltage and the waveform.

Diagrams of the limiting values are available for each capacitor series on request.

VOLTAGE	DC	DC + AC	AC
Waveform figure			

6.2 OPERATING TEMPERATURE AND SELF-GENERATED HEAT

The surface temperature of the capacitors must not exceed the upper limit of its rated operating temperature.

During operation in a high frequency circuit or a pulse signal circuit, the capacitor itself generate heat due to dielectric losses.

Applied voltage should be the load such as self-generated heat is within 20 °C on the condition of environmental temperature 25 °C.

Note, that excessive heat may lead to deterioration of the capacitor’s characteristics.

RELATED DOCUMENTS	
General information	www.vishay.com/doc?22001

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