Non-Linear Resistors | Application Note

Optimization of a Capacitor Precharging Circuit Featuring Vishay's PTCEL67 With Qorvo's QSPICE™ Simulator

By Alain Stas

INTRODUCTION

There are several issues that frequently arise in discussions of electronic circuit simulation. It is often argued that the software is too expensive; simulation times are too long; parasitic effects like temperature variations and product tolerances are not precisely accounted for; and the results simply do not represent a very complex reality. In this article, we will address these issues using the simulation of a precharge circuit for automotive chargers - featuring a network of Vishay's PTCEL67 inrush current limiters - as an example. For the simulation, we will rely on Qorvo's QSPICE™ software [1].

THE PRECHARGE CIRCUIT

Qorvo's QSPICE simulator is free to use without any restrictions, so right off the bat we've addressed the issue of cost in our simulation. With the software installed, next we need good models for Vishay's ceramic-based PTCEL67 inrush current limiter [2], which are available on Hackster.io [3]. Not only are the models available for download, but a full simulation of the charging of a capacitor by a rectified AC main network - through a network of PTCEL67 components - is possible.

Such a circuit is demonstrated in Fig. 1, which shows the rectification of a 50 Hz, 1000 V_{AC} main voltage with a diode bridge and a 2 mF capacitor. Surge current limiting and thermal protection is provided by a network of six PTCEL67R501TBE components, comprised of three parallel branches of two elements in series.

As an exercise, we can replace the PTCEL network with a fixed equivalent resistor of 333 Ω (three parallel branches of 2 x 500 Ω) and simulate the time it takes for the capacitor to reach 90 % of the final voltage, which turns out to be exactly 4.755 s. This value gives us a reference point for our later simulations. Also, we can easily verify that with an AC main, the capacitor charging time constant (63.2 %) is higher than the DC mains RC constant (here = 333 x 2 x 10^{-6} = 0.67 s). With an AC main, the time constant for 63 % is in fact equal to 2.08 x RC = 1.387 s.

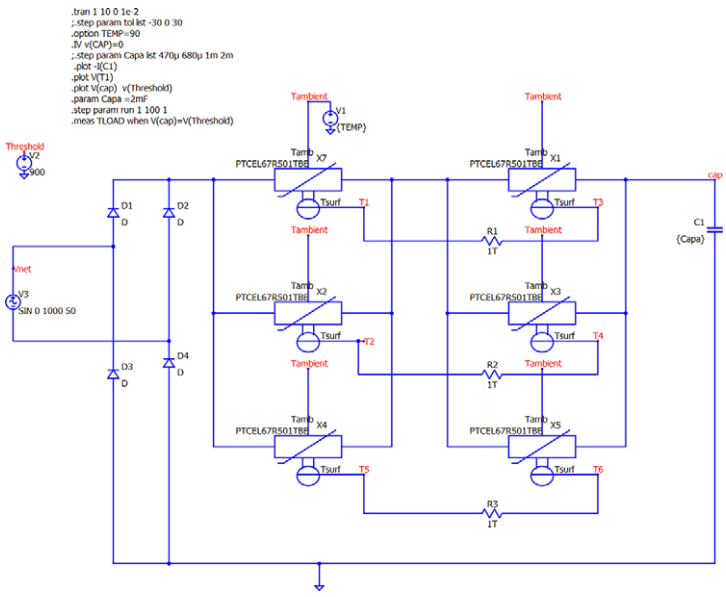

Fig. 1 - A precharge circuit of a capacitor with a 1000 V_{AC} mains

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TEMPERATURE AND TOLERANCE

The PTCEL67R501TBE model used for this simulation takes into account the eventual ambient temperature variation via the T_{amb} node. It also shows the self-heating above this temperature via the T_{surf} node. The last T_{surf} pin can be used to interconnect the PTCEL devices in the event the user decides to thermally link them. In the schematic, resistances R_1, R_2, and R_3 do not refer to electrical resistances, but thermal resistances (expressed in °C/kW as opposed to Ω). This is an electronic representation of the thermal conduction performed, for example, by a thermoconductive silicon paste deposited on the serial PTCEL components, which then have to be pressed against each other on the board. An example will be presented later in this article. In the Fig. 1 schematic, these resistances are of about 1T, and thus in such a case the serial PTCELs do not contact each other.

Finally, the electrical R_{25} tolerance of the PTCEL67R501TB0 (500 Ω, ± 30 %) is named TOL and is evaluated in a random way by means of the product attribute: TOL = 30 - 60 x random( ), where random( ) changes from 0 to 1.

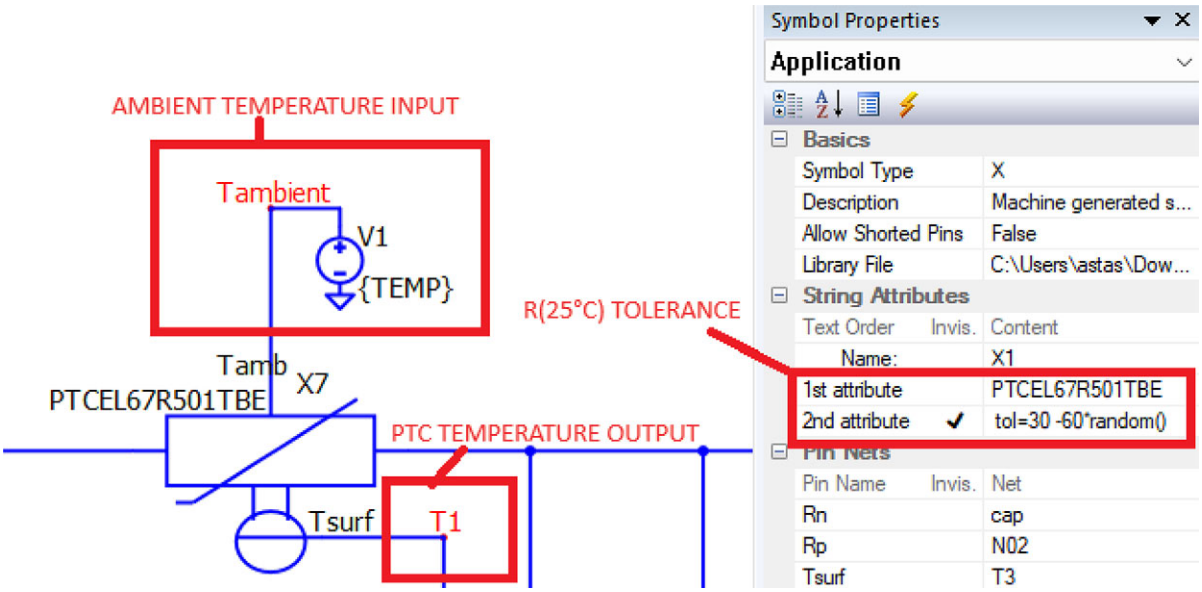

Fig. 2 - Tolerance and temperature properties of the PTCEL model

The issue of parasitic effects has now been fully addressed and it is time to run the simulation.

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THE SIMULATION

The capacitor must be charged at a minimum of 900 V before a 4 s delay. As we have already established, with a fixed resistor, the time would be 4.755 s. But as the resistance of the PTCEL decreases when voltage is applied, and as its temperature increases prior to the switch (Fig. 3), we can still achieve the desired result. We will plot the voltage rising on the capacitor (Fig. 4), the temperature variation of two PTCEL67 devices in series in one parallel branch (Fig. 5), and the inrush current into the circuit (Fig. 6).

A .meas SPICE directive is used to compute the time needed for the capacitor voltage to reach 900 V from 0 V. 100 simulations are made, with the TOL changing randomly for each PTCEL device independently of each other. The results are then plotted in the histogram in Fig. 7.

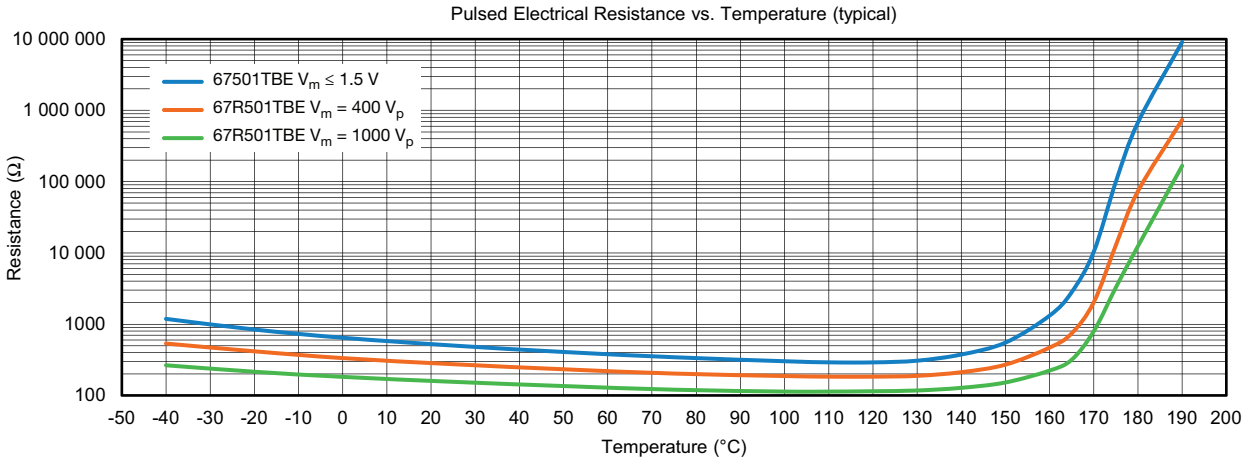

Fig. 3 - PTCEL resistance variation as a function of temperature (in pulsed voltage)

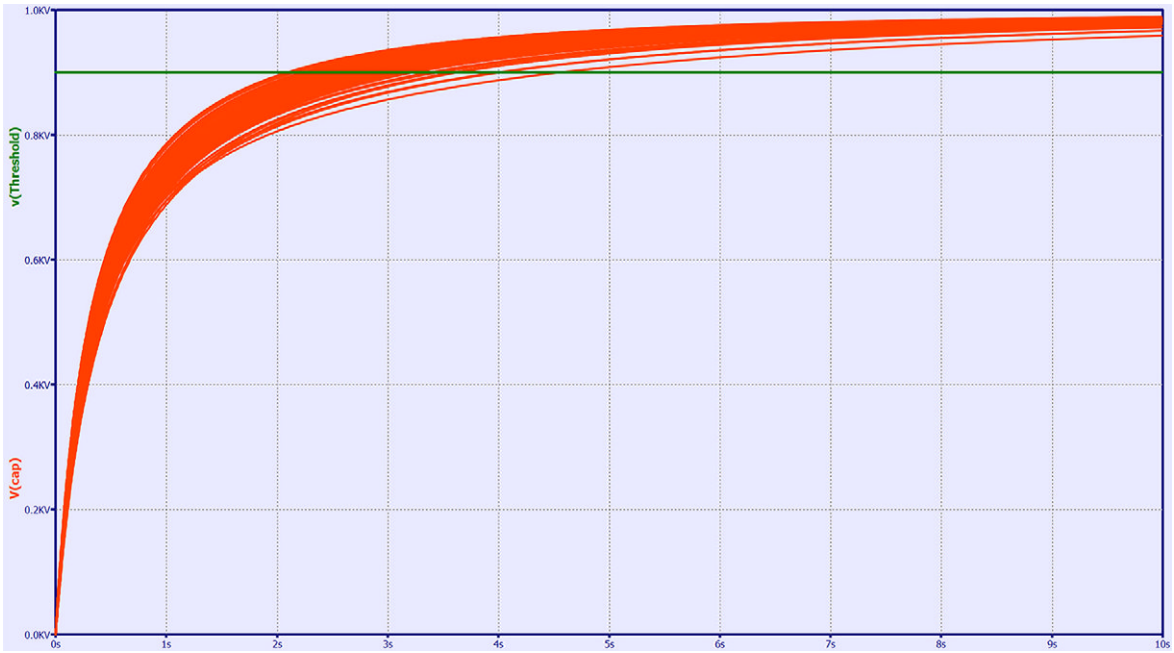

Fig. 4 - Capacitor voltage drop from Fig. 1

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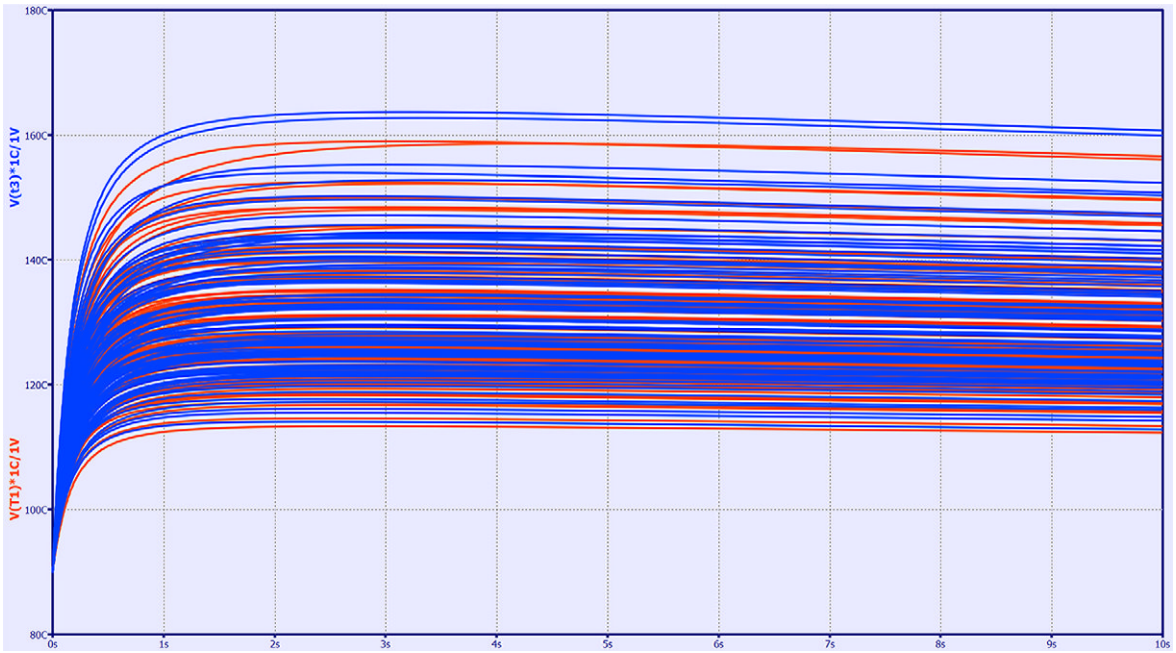

Fig. 5 - The temperature change of two PTCEL67 devices placed in series in one branch

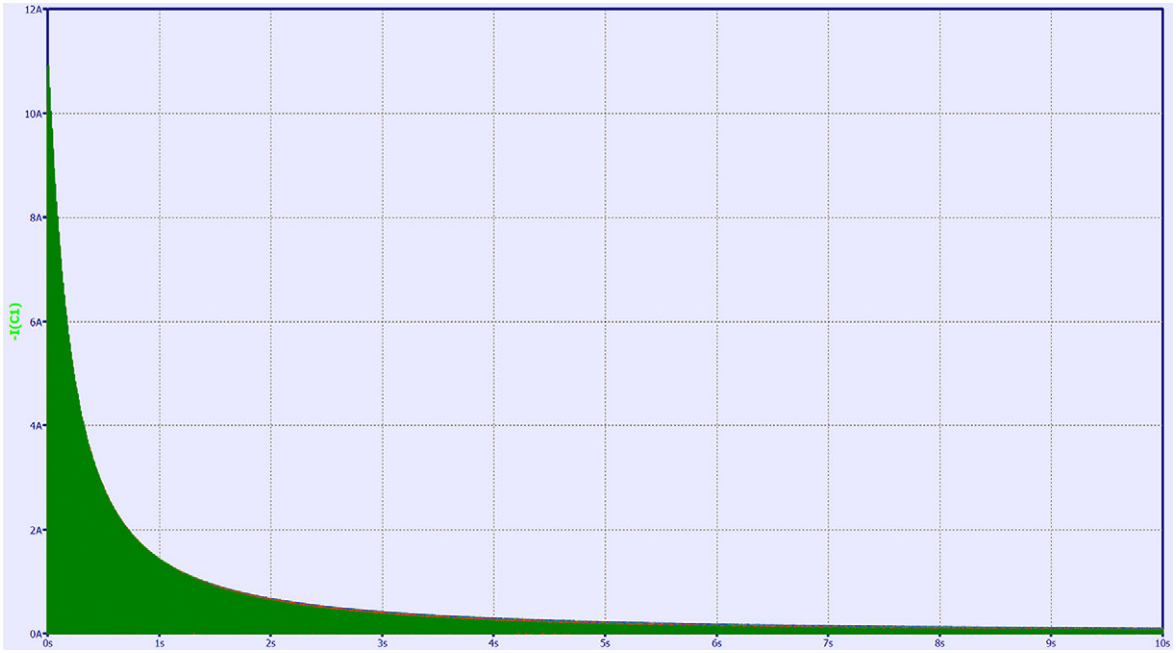

Fig. 6 - Capacitor current variation in time

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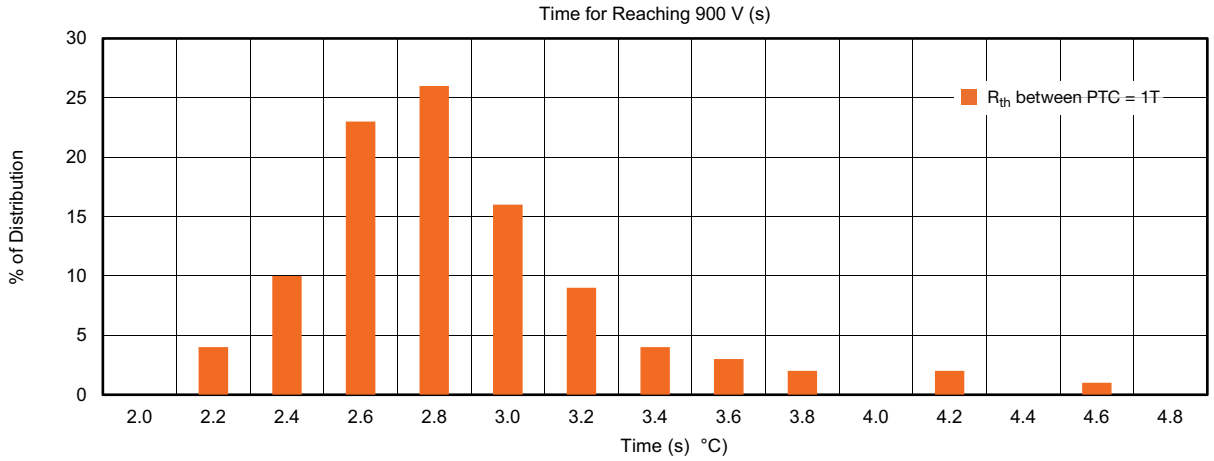

Fig. 7 - Histogram of the time distribution (time for the voltage capacitor to reach 900 V)

THE RESULTS

The histogram in Fig. 7 shows that a small proportion of the measurements is above 4 s. This happens because of the ± 30 % tolerance on the PTCEL's R_{25} characteristic. As a result, some pieces are switching faster, which increases the global network resistance and thus the charging time.

In order to correct this effect, we can increase the thermal efficiency of the PTCEL67 network by thermally connecting the two PTCEL67 devices in each parallel branch. Then we'll drastically decrease the R_1, R_2, and R_3 values to 2.5 °C/W and repeat the same Monte Carlo simulation with this change only.

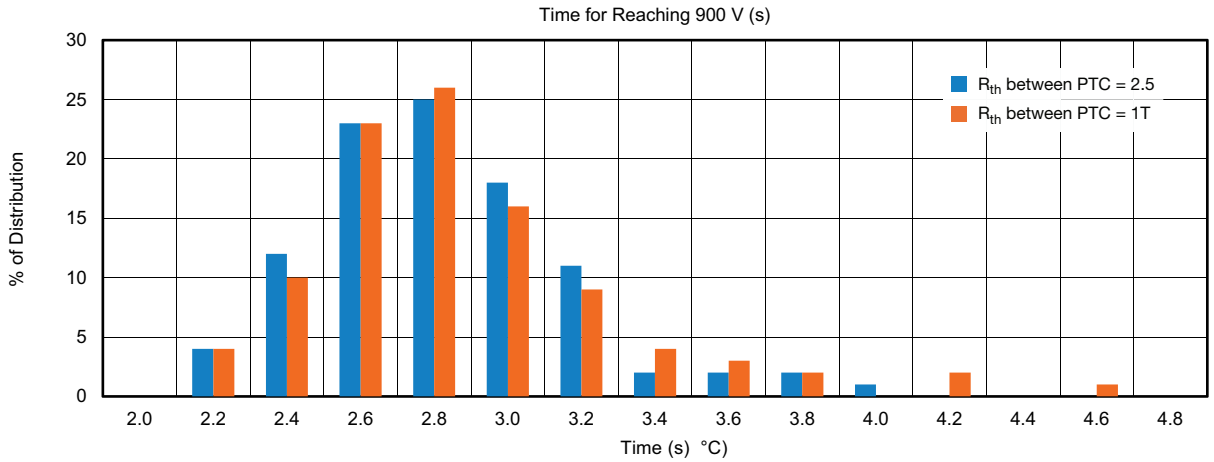

Fig. 8 - Histogram of the time distribution (time for the voltage capacitor to reach 900 V)

We can see in Fig. 8 that the thermal connections between the PTCELs decrease the spread so that the time to reach 900 V falls just under 4 s. This thermal contact uniformizes the temperatures of the PTCELs in each parallel branch, suppressing the distribution tail. Of course, we cannot exclude a marginal overpassing of this 4 s time. More simulations would be needed to assess the real maximum.

But when it comes to the issue of simulation time, the screen capture in Fig. 9 shows that each of the hundred simulations was performed in less than 2 s. These results are incredibly fast, and I would therefore encourage QSPICE™ users to increase the number of runs.

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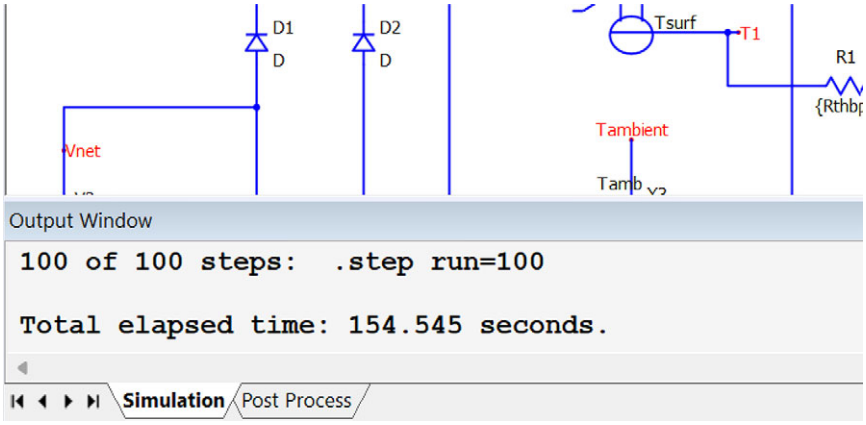

Fig. 9 - Screen capture of the simulation time for the circuit in Fig. 1

FROM A MONOPHASE TO A TRI-PHASE CIRCUIT

In order to represent a real grid more closely, we can then extend our circuit to a tri-phase circuit: we draw then the circuit of Fig. 10, and we can simulate similar conditions with the same guidelines exposed before, and achieve similar results (Fig. 11).

The circuit of Fig.10 can be fully download from Hackster.io.

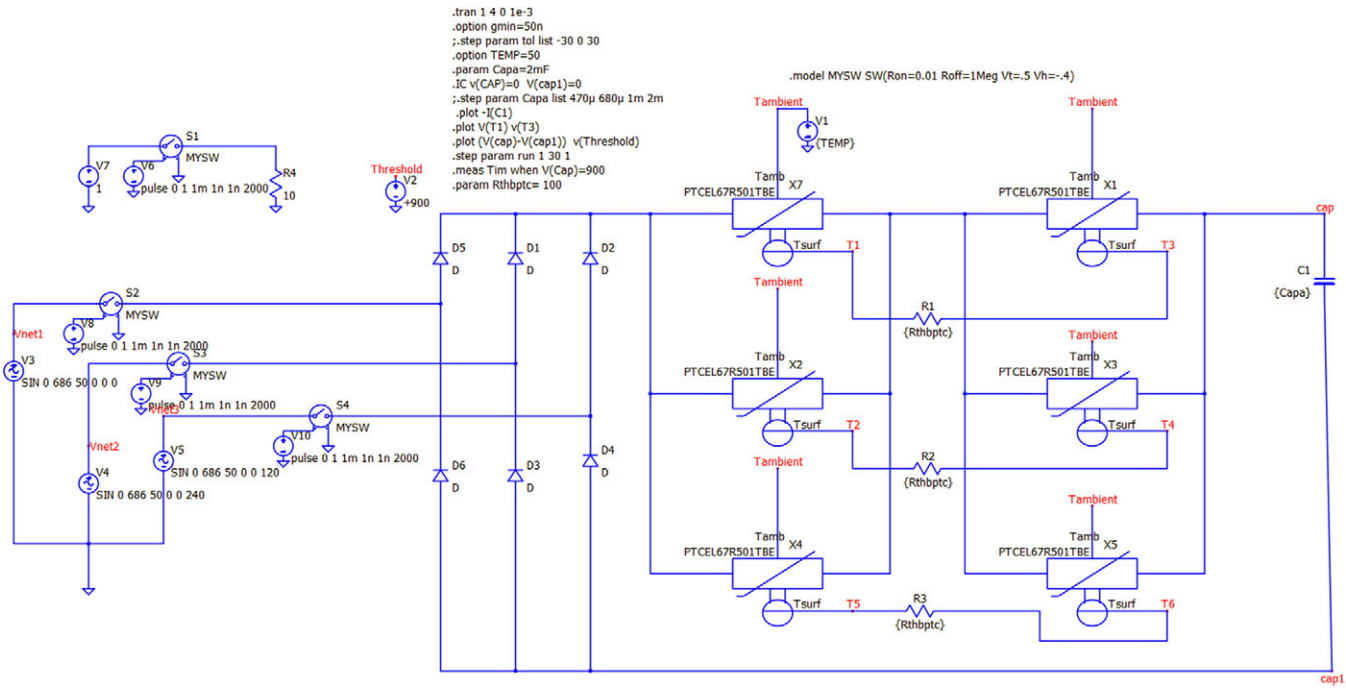

Fig. 10

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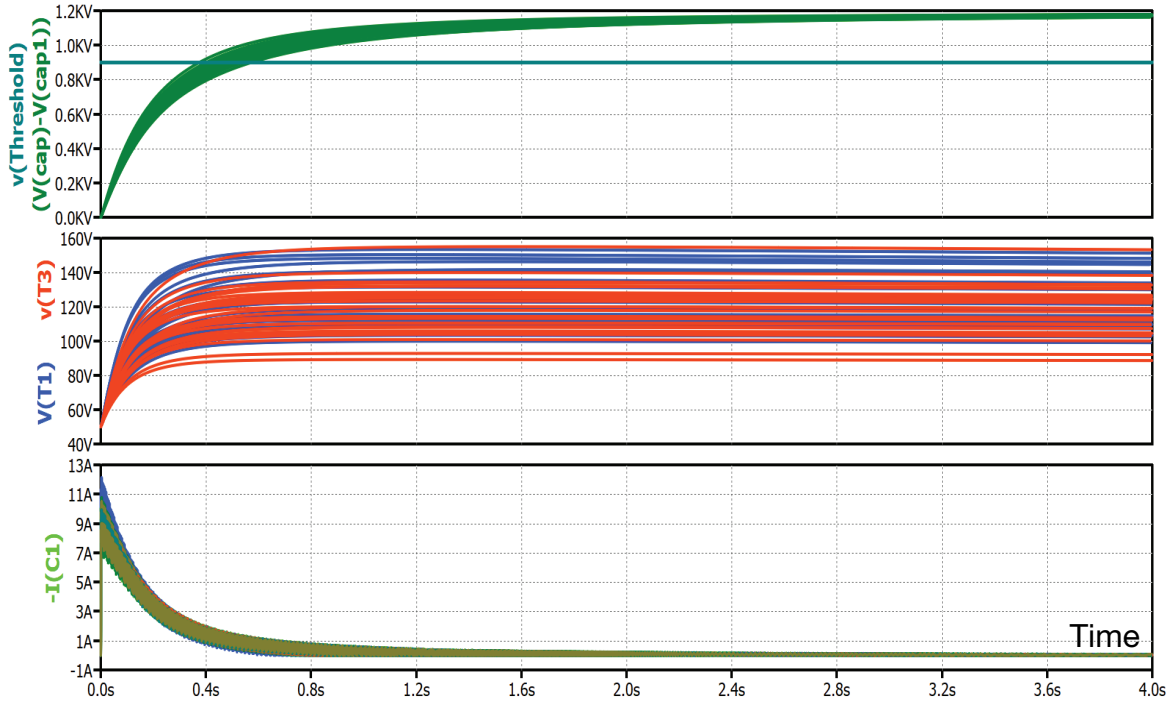

Fig. 11

SIMULATION VS. REALITY: YOU MAKE THE CALL

Now that no-nonsense results have been reached using free software - taking temperature and tolerance effect into account - within a reasonable time, there's one issue left to address: whether or not these results are representative of the real complex world. Ultimately, I leave it up to you, the reader, to decide, as you deal with the complex problems associated with precharge circuits every day.

I recommend practicing the simulation first with your own circuit - which may be much more complex than the one studied here - while still using Vishay SPICE models and QSPICE software from Qorvo. Then verify if your practical results match the simulation results provided here. Finally, make your own determination about the ability of Qorvo's QSPICE software, with Vishay SPICE models from Hackster.io, to predict reality. Given the care which was taken in the building of the SPICE models, and the power of QSPICE to achieve accurate results, I have very little doubt that your simulation and reality will align.

Feedback about your conclusions and help requests are welcome anytime at edesign.ntc@vishay.com.

REFERENCES

[1] QSPICE™ Simulator - Qorvo

[2] PTCEL High Energy - PTC Thermistors, Inrush Current Limiter High Energy

[3] EV Battery Pre-Charge Simulated in Qspice With PTC - Hackster.io