



From Specification to QSPICE®-ification: a Complete Modelling Framework for Vishay PPTC Devices

By Alain Stas

1. INTRODUCTION - GENERAL CHARACTERISTICS AND POSSIBLE SPICE-IFICATION OF POLYMER PTC DEVICES

Among the new products being introduced by Vishay in 2026 are several series of SMD polymeric positive temperature coefficient (PPTC) devices, covering package sizes from 0603 to 2920. These protection components are widely used in applications where a resettable fuse is preferred over a standard fuse, including consumer, telecommunications, industrial, and medical systems.

However, despite their widespread use, there has been little enthusiasm for developing detailed SPICE models for these devices. Apart from a few theoretical attempts (like https://hanbinhu.github.io/data/report/2014_PPTC_TE_Connectivity.pdf), plug and play models are difficult to find. Among the top 15 major players, only Bourns provides them ([Bourns - Design Files](#)).

PPTC devices are passive protection components used across a wide range of electronic systems, and many of their typical operating conditions can be effectively reproduced through SPICE-based simulation. Examples include overcurrent or short to ground events on a USB 5 V supply line, short to ground faults on a Li-ion battery, or motor stall protection at different ambient temperatures. The value of such simulations to engineers is clear, as they directly illustrate the consequences of complex overcurrent conditions or potential failure scenarios. Alas, PPTC models are seldom available.

Why is this the case? Why do manufacturers prefer to provide static characteristics in datasheets rather than dynamic electronic models capable of delivering predictive results for these types of applications?

I received an answer to this question from an experienced electronic engineer to whom I had shown a snippet of a SPICE model I had developed for a new Vishay PPTC.

His questions went directly to the key concerns designers must consider. Would the model include the large tolerances inherent in these components? Would ambient temperatures influence the results? Would it account for device aging after the first trip event? What happens if a simulation exceeds the maximum rated voltage during operation? And how would trip time curves versus fault current be incorporated?

To some, this would sound like a dire warning - similar to the one Bob Pease gives when asked about SPICE software. He replied that "his favorite programming language was solder." ([Bob Pease says: "My favorite programming language is solder" | Atmel | Bits & Pieces](#))

Indeed, all these concerns are valid. If models are to be used effectively, all these points must be addressed. My conclusion from this advice, however, was that we should move forward and model these crucial characteristics as fast and realistically as possible, embracing the challenge. The next step is to apply these models to as many applications as possible to demonstrate their value.

2. PPTC SPICE MODEL GENESIS AND THERMAL FUNDAMENTALS

From a functional perspective, a PPTC consists, to a first approximation, of a thermal mass with a baseline electrical resistance at ambient temperature. When heated by a fault current (I_{fault}) to the temperature T_{trip} (trip temperature), it undergoes a rapid positive resistance change after a time called t_{trip} , sharply reducing the current and stabilizing at a high temperature.

The heat balance of the PPTC system can be described by the following equation:

$$C_{\text{th}} \frac{dT}{dt} = D(T_{\text{amb}} - T) + R(T)I^2 \quad (1)$$

In equation (1), C_{th} represents the thermal capacitance, dT/dt is the rate of temperature change, and D is the thermal conductivity constant. The terms T_{amb} and T denote the ambient and system temperatures, respectively, while $R(T)$ is the electrical resistance and I indicates the input (fault) current. This formulation is commonly used to model transient thermal

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behavior in electronic systems. Before tripping, the resistance can be approximated as a linear function of temperature, characterized by a temperature α (tempco), expressed in %/K up to the trip point.

$$R(T) = R_{25}(1 + \alpha(T - T_{25})) \quad (2)$$

From equations (1) and (2), we derive and simplify:

$$dT = \left(\frac{DT_{amb} - R_{25}\alpha T_{25}(I^2 + R_{25}I^2)}{C_{th}} - \frac{(D - \alpha R_{25}I^2)}{C_{th}} T \right) dt = (A - BT)dt \quad (3)$$

In fact, here $T_{amb} = T_{25} = 25^\circ\text{C}$.

By integrating equation (3) from $t = 0$ to t_{trip} and from $T = 25^\circ\text{C}$ to $T = T_{trip}$, we get:

$$\int_{T_{amb}}^{T_s} \frac{dT}{(A - BT)T} = t_{trip} \quad (4)$$

$$t_{trip} = \frac{1}{B} \ln \left(\frac{A - BT_{amb}}{A - BT_{trip}} \right) \quad (5)$$

Plotting equation (5) for the defined parameter values of the Vishay product PPTC0603E3010V15, we can compare it to values of the datasheet (www.vishay.com/doc?29254).

D	0.004602	W/K
T_{amb}	25	$^\circ\text{C}$
R_{25}	2.843	Ω
alpha	0.007985	%/K
C_{th}	0.002	J/K
T_{trip}	125	$^\circ\text{C}$

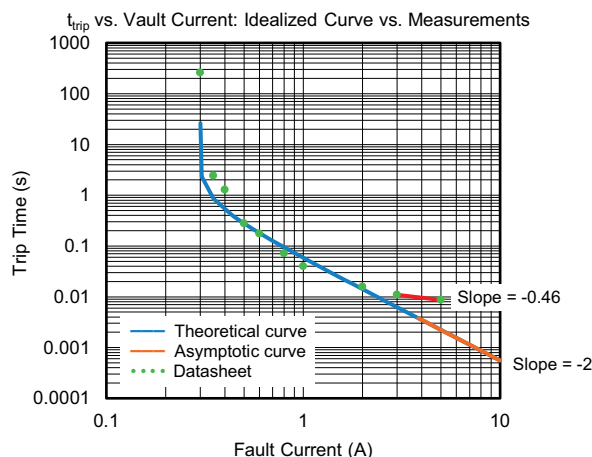


Fig. 1 - I_{trip} vs. fault current computed theoretical curve compared to datasheet PPTC0603E3010V15

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Our simplified single thermal-block model shows clear limitations at both low and high fault currents. At high current levels, the ideal slope of $\ln$ (trip time) versus $\ln$ (fault current) should be -2, since the trip time is inversely proportional to the dissipated power, which itself scales with the square of the current. In practice, however, the observed slope is much flatter (around -0.46), indicating that additional physical mechanisms distort the thermal response at high currents. These effects reduce the model's accuracy and must be included to obtain realistic simulations. At low fault currents, the theoretical curve rises more sharply than the measured one.

The discrepancy is mainly due to the fact that a PPTC cannot be modeled as a single thermal mass with heat dissipated through a single thermal resistance. Additional factors also contribute, including instantaneous aging effects, heat dissipated into the solder tracks rather than the device itself, and delays in heat propagation with the polymer and carbon network.

3. FULL PRACTICAL REALISTIC PPTC SPICE MODELS

Under low current conditions, the PPTC thermal behavior is better represented by a three-stage thermal Cauer network (Fig. 2), implemented directly implemented in QSPICE® using the QORVO® [QSPICE® simulation tool](#). The T_{PPTC} node represents the temperature of the internal active polymer PTC material, while the $T_{electrode}$ node corresponds to the temperature at the component electrodes. T_{PCB} represents the temperature at the PCB solder joint, and T_{amb} denotes the far-field ambient temperature. The three R_{thi} / C_{thi} pairs model the thermal resistance and thermal capacitances between, or associated with, these four nodes.

The resistance R_{PPTC} is represented using a (here simplified) V_{table} . The TOL parameter represents the tolerance defined by the fundamental device characteristic: R_1 min. before handling, R_1 max. after soldering and tripping.

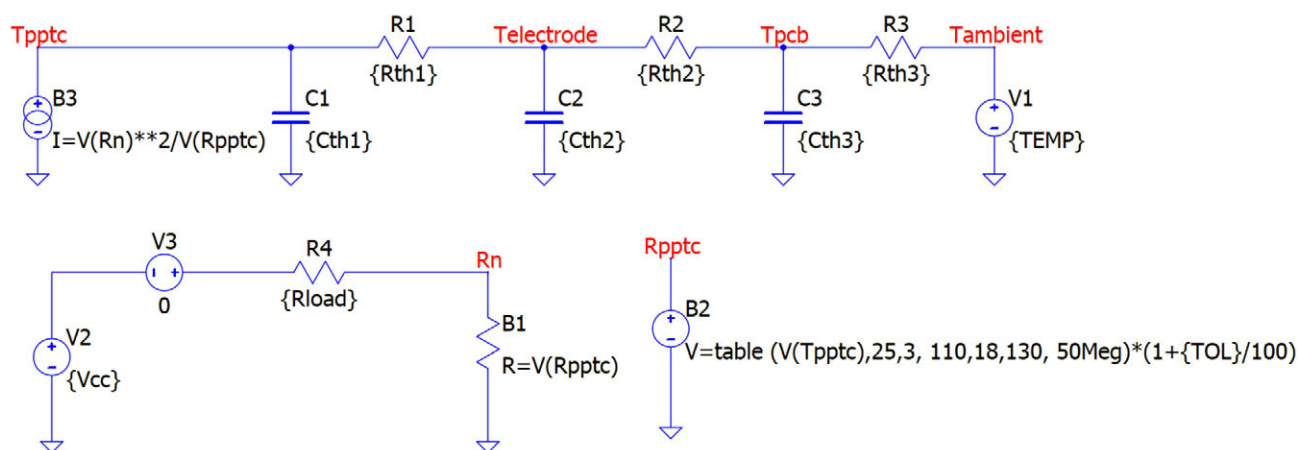


Fig. 2 - Example of a 3 ladder thermal Cauer model for a PPTC placed in an application circuit

The SPICE software used for this modelling is QSPICE®, which, among its other advantages, allows up to six parameters to be swept simultaneously, enabling thousands of simulations and measurements to be performed in a very short time.

Once the three R_{thi} / C_{thi} pairs have been adjusted to fit the trip time vs. fault current characteristics of the PPTC0603E3010V15, and the high current flattening of the trip time curve has been mathematically addressed, we can observe how closely the simulation reproduces the measured results (Fig. 3).

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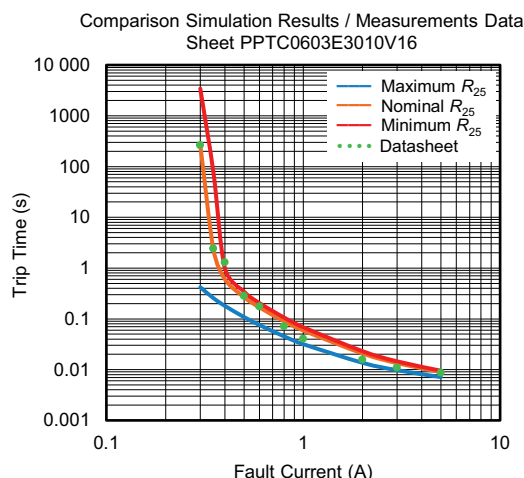


Fig. 3 - Simulated trip time vs. fault current of 3 ladder Cauer model compared to datasheet

A significant portion of the remaining deviation between the measurements and the simulation results is likely due to measurement conditions and limited reproducibility. It should be noted that resistance drift can occur during the measurement itself. The simulation results show that all measurements fall within the predicted minimum and maximum values, representing a clear improvement over the single thermal-block. Further improvements may be possible, but they would likely come at the cost of increased model complexity.

It now remains to demonstrate the capability of this QSPICE model to:

- Reproduce the positive resistance aging that occurs after a trip event, which typically remains for several hours
- Implement a “smoke” analysis feature. In this case, the PPTC is forced into will a near short-circuit condition when the applied voltage exceeds 25 % of its rated value. This represents a failure condition that must be avoided in real-world applications for safety reasons. Simulating a short circuit provides a useful warning that the circuit parameters are incorrect
- Account for the far-field ambient temperature, showing the natural derating or increased sensitivity. For example, in Fig. 2 the parameter TEMP, representing ambient temperature, varies from 25 °C to -20 °C or 50 °C.

This behavior is illustrated in the next simulation (Fig. 4) using the upgraded model. At different ambient temperatures, two successive 12 V pulses are applied to an 0805 PPTC rated at 15 V, followed by, two pulses of 22 V, exceeding the rated voltage by more than 25 %. The resulting waveforms are shown in Fig. 5.

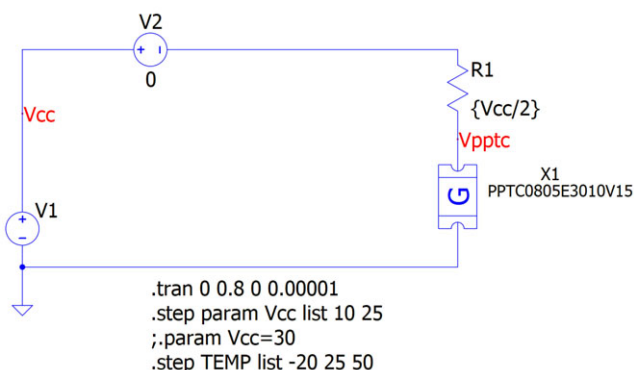


Fig. 4 - A PPTC0805E3010V15 in an application circuit tested in surge for different ambient temperatures

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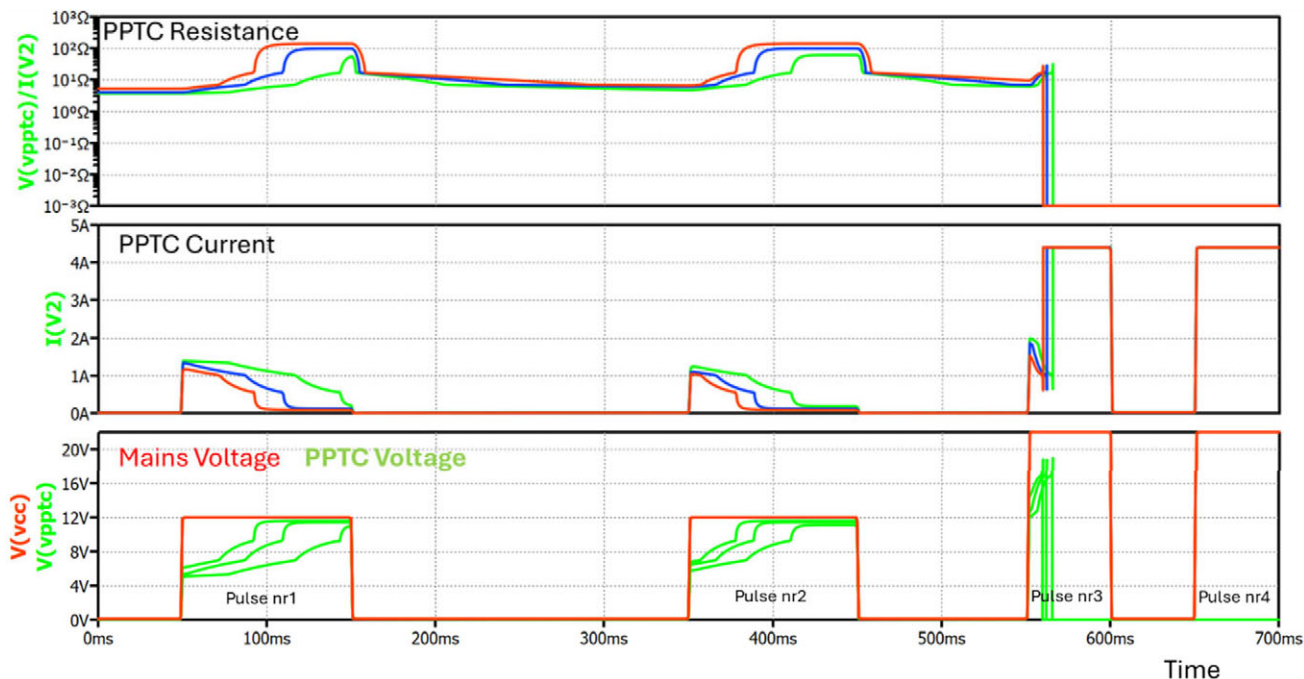


Fig. 5 - Simulation results of circuit of Fig. 4

- The influence of ambient temperature on the trip time is clearly observed during the first two pulses: the trip time decreases for the second pulse at each temperature, indicating that the initial PPTC resistance has increased following the first trip.
- During the third pulse, the component enters a short-circuit condition when the applied voltage exceeds the specified limit.
- During the fourth pulse, this short-circuit condition is shown to be permanent.

Due to the dependance on far-field ambient temperature, a derating rule for the hold current is specified in the datasheet, as shown for the PPTC1210 in Fig. 6.

Thermal Derating

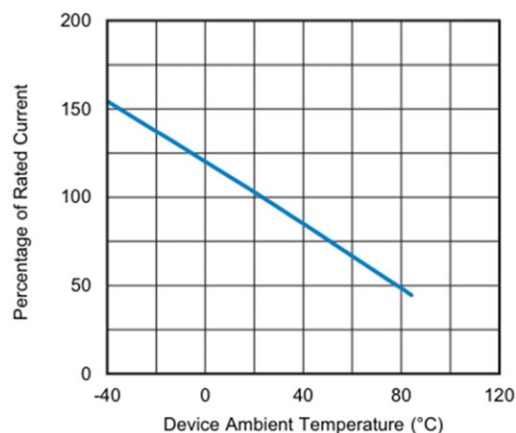


Fig. 6 - Datasheet thermal derating curve for PPTC

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The technical details underlying this graph are best illustrated by the following simulation of the circuit shown in Fig. 7. A PPTC1210E3075V24 is subjected to a 25 V supply (below the maximum rated voltage of 24 V + 20 %) through a load resistance that is adjusted while sweeping the ambient temperature in order to maintain nearly the same trip time (results shown in Fig. 8).

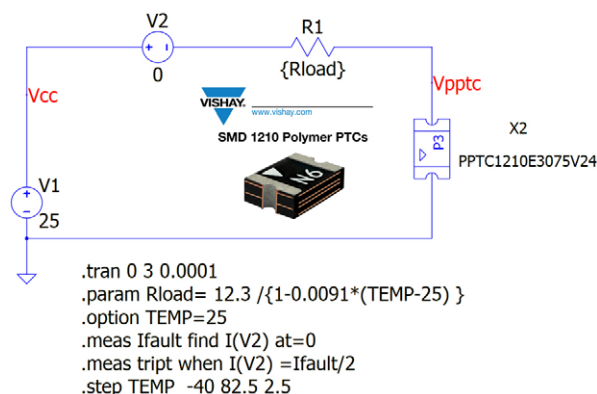


Fig. 7 - PPTC tested in over-current with load resistances changing with temperature

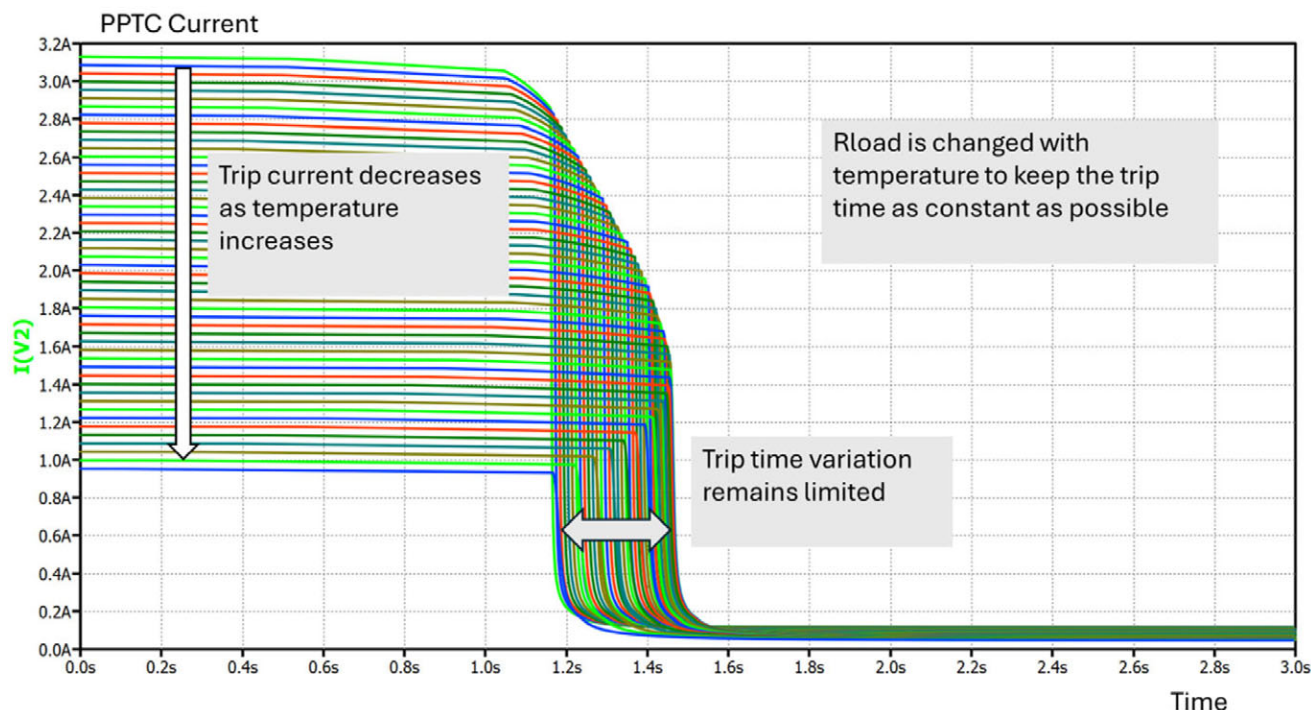


Fig. 8 - Simulation results of circuit of Fig. 7

From these results, we extract the variation of the fault current as a function of the ambient temperature, reproducing the datasheet derating curve shown in Fig. 9. For a similar trip time, the current derating must be linear and can be accurately reproduced by simulation.



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% variation Trip Current vs value at 25°C

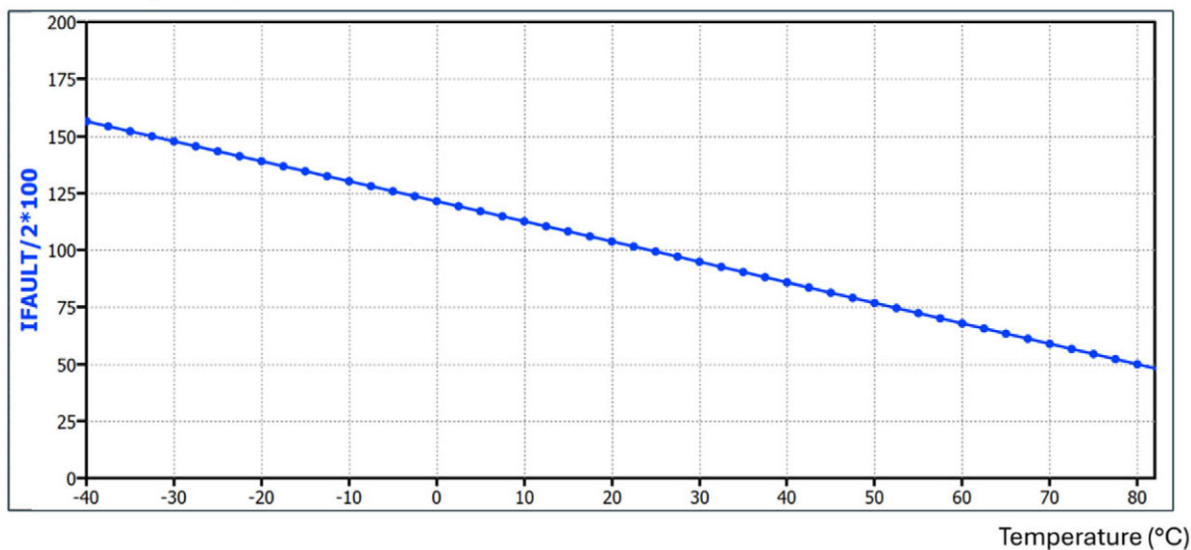


Fig. 9 - Simulated thermal derating curve

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4. SIMULATION OF FULL APPLICATIONS BASED ON THE PPTC SPICE MODELS 4.15 V USB PROTECTION

4.1 Overcurrent Protection of a 5 V USB Power Supply

Now that we have PPTC models, we can return to the simulation of the various applications mentioned in the introduction. Let us first consider the overcurrent protection of a 5 V USB power supply. A generic circuit for this application, including the PPTC, is shown in Fig. 10 and the simulation results are presented in Fig. 11.

USB 5 V supply Protection with PPTC : Hot Plug/ Short Fault/
Worst Case Analysis R(25°C) /Sweep Ambient Temperature

- * Simulation of three parallel USB loads, each protected by a PPTC resettable fuse.
- * The source is connected through a realistic plug-in profile including ESR, cable inductance, and contact resistance. Each load has a bulk capacitor with ESR and a nominal operating resistance. At 100 ms, a low-ohmic short is applied to each branch to emulate a downstream device failure. The PPTCs respond by heating and transitioning to their tripped state, limiting current and protecting the upstream supply.
- * A temperature sweep (-20°C to +50°C) captures the effect of ambient conditions on trip time, peak current, and post-trip resistance.

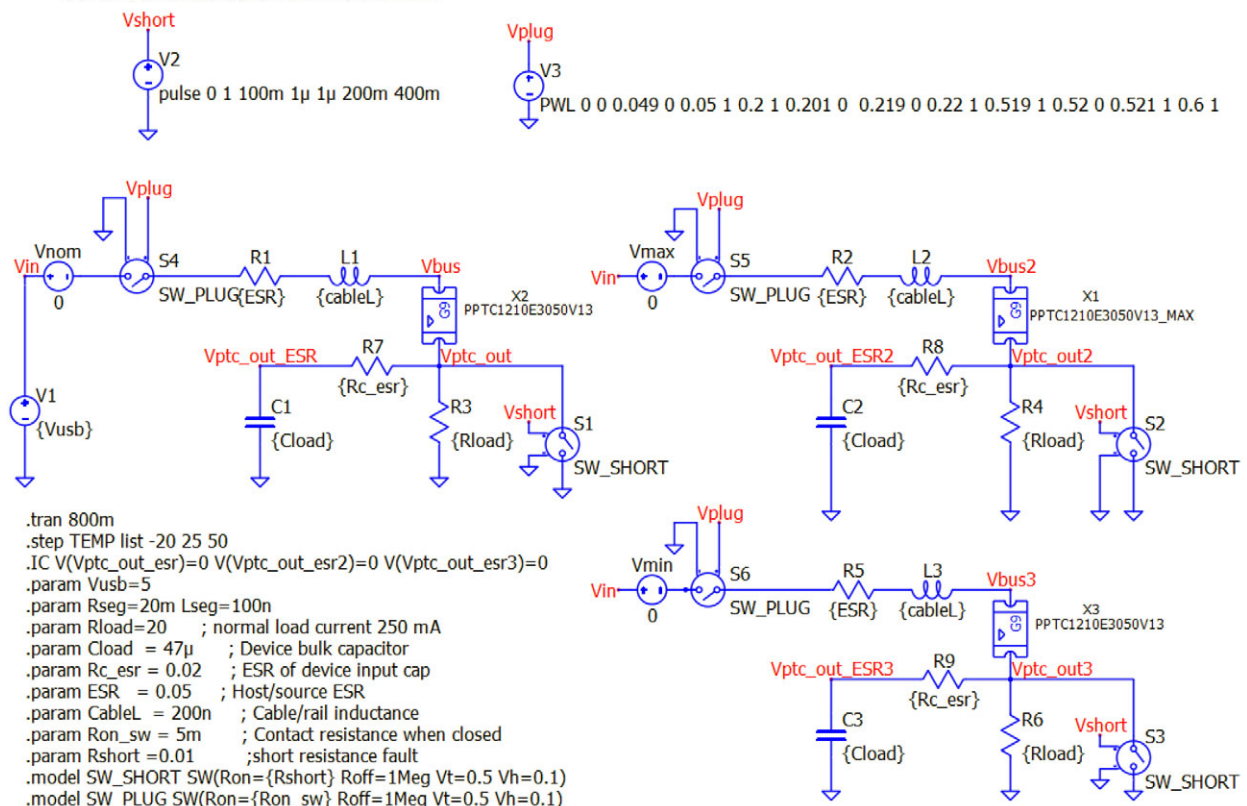


Fig. 10 - Complete application circuit of USB 5 V supply protected by PPTC

A PPTC1210E3050V13 was selected in to ensure a hold current of 0.5 A and a maximum rated voltage of 15 V, well above the USB supply voltage ($V_{USB} = 5$ V).

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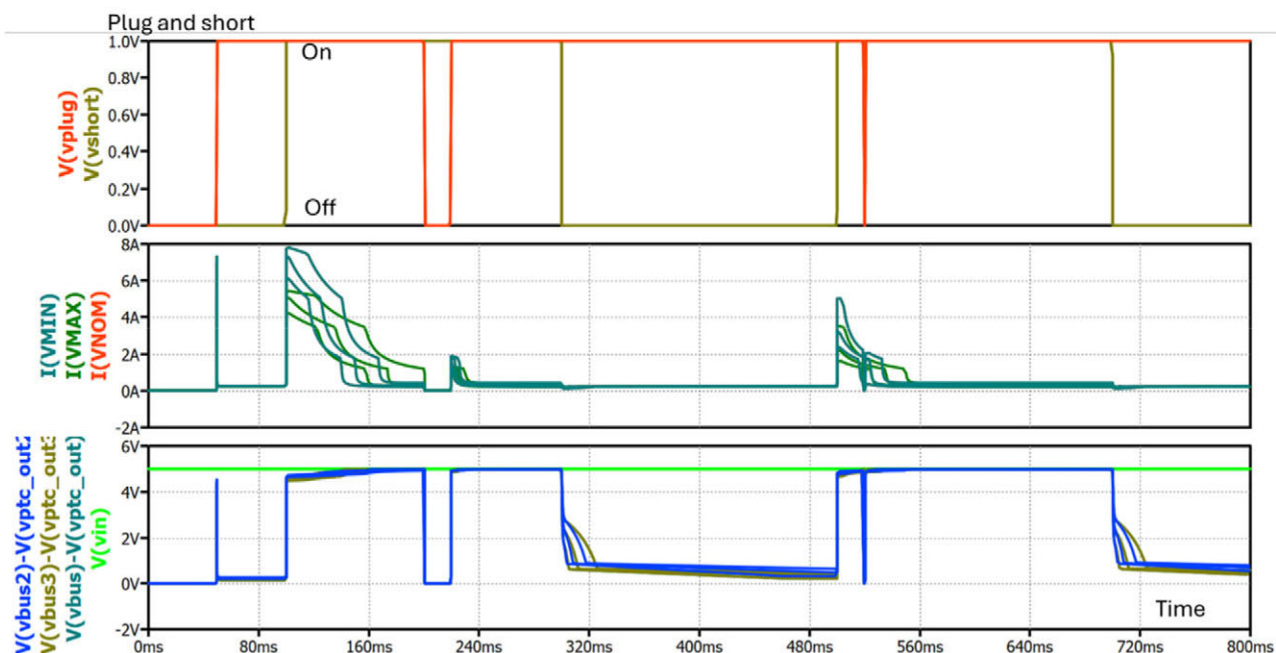


Fig. 11 - Simulation results of circuit of Fig. 10

The upper pane shows the plug and short-circuit disturbances applied in the simulation. At 100 ms, a load short circuit is introduced, causing the PPTC to trip either partially or fully (middle pane), depending on the maximum or minimum R_{25} values and the ambient temperature. A second short circuit results in a complete trip.

The lower pane shows the corresponding voltage variations across the PPTC.

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4.2 Protection of Motor Stalls

A second application example is the protection of small electric motors against stall conditions, illustrated in Fig. 12. A stalled motor draws a very high current, which rapidly heats the windings and can quickly lead to thermal damage unless proper protection is provided.

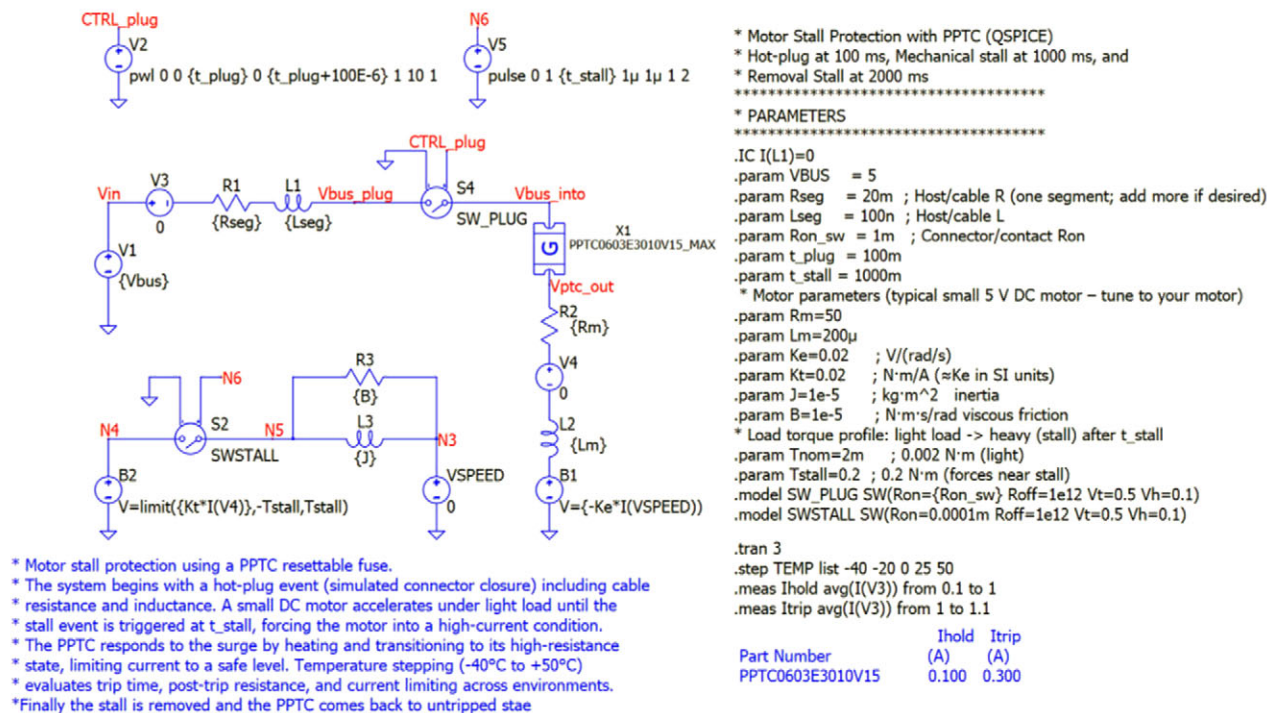


Fig. 12 - Complete circuit of an electric motor protected against stalls

The resulting waveforms are shown in Fig. 13.

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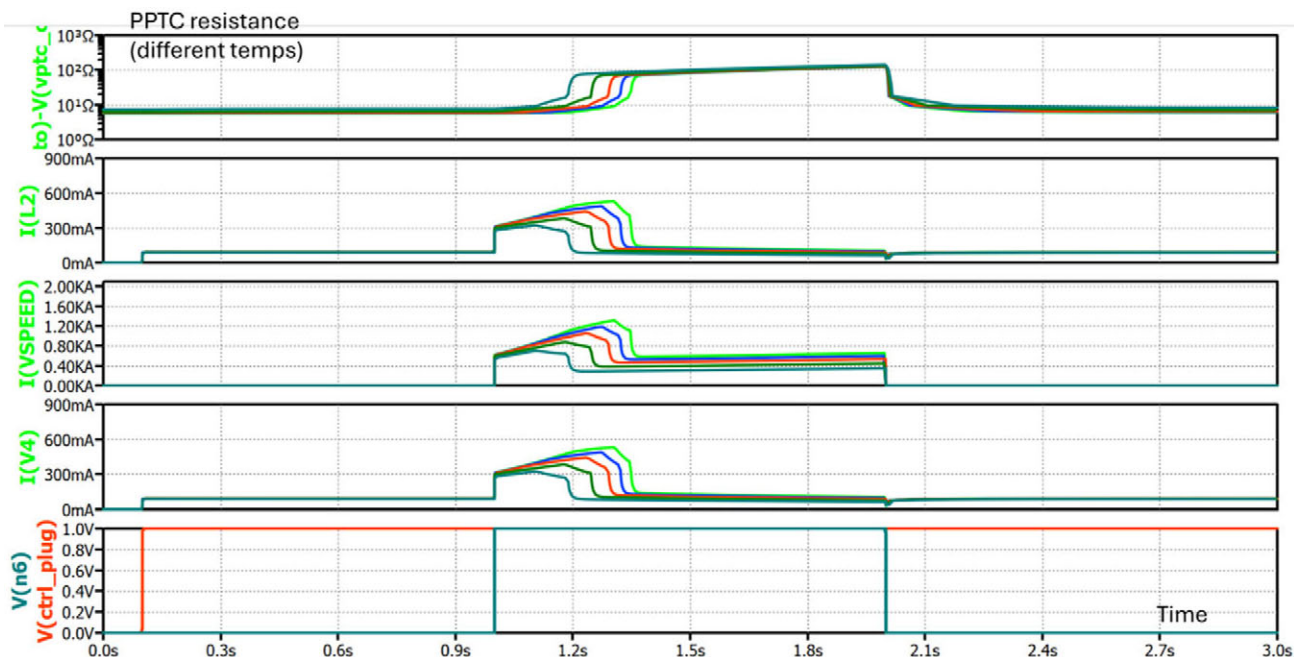


Fig. 13 - Simulation results of circuit of Fig. 12

The text included in the simulation (Fig. 12) is self-explanatory. This second example provides another practical demonstration of the usefulness of SPICE modeling. At time = 1 s, the motor stalls and the current I(L2) flowing through the motor increases at different levels depending on the ambient temperature while the PPTC heats up, after which the device trips.

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4.3. Li-ion Battery Short Circuit Protection

The simulation circuit and results are presented in Fig. 14 and Fig. 15.

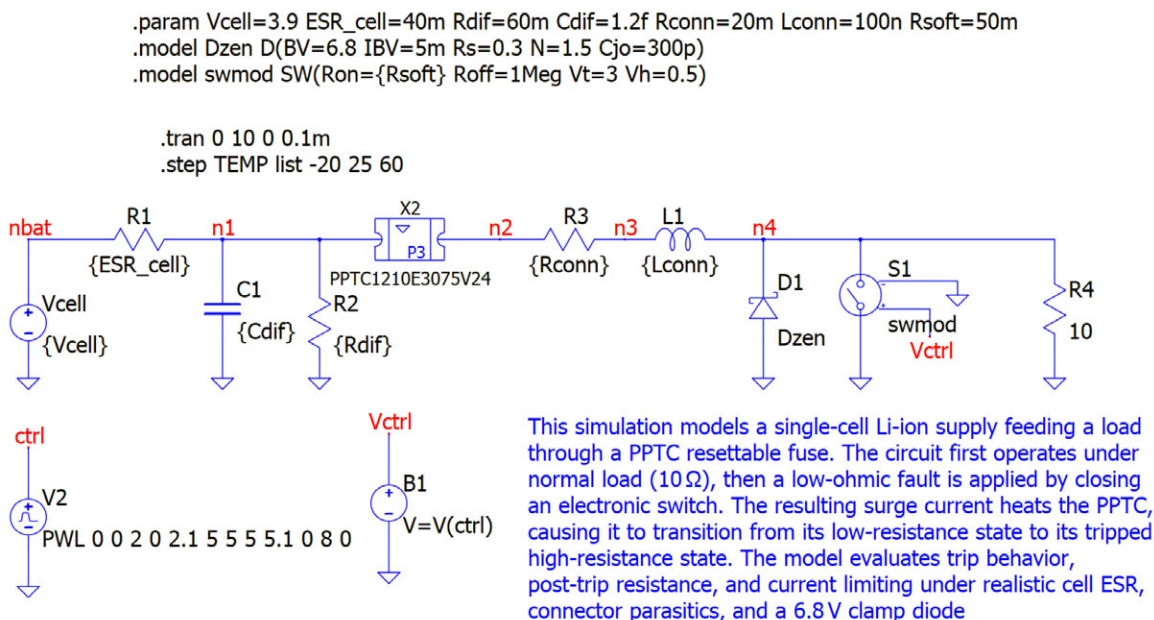


Fig. 14 - Simulated circuit of a Li-ion battery with load short-circuit

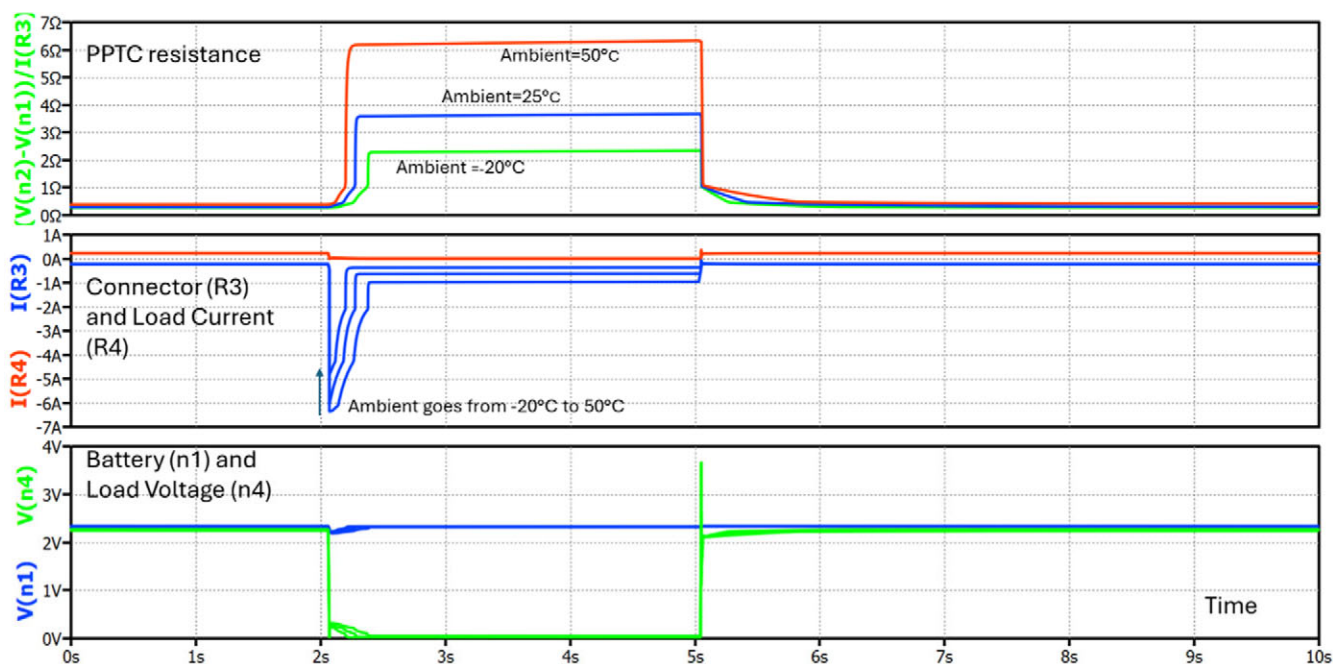


Fig. 15 - Simulation results of circuit of Fig. 14



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The load short circuit is introduced just after 2 s (lower pane), and we see the surge current through the circuit (mid pane), inducing a resistance rise of the PPTC (upper pane). A low ambient temperature induces a slower PPTC reaction by a factor above 2 and increases the surge current from 4.5 A to 6.5 A.

FINAL CONCLUSIONS

QSPICE® modelling of Vishay PPTC devices - built by fitting model parameters directly to datasheet characteristics - successfully meets the essential requirements for designing reliable and safe over current-protection circuits. The models accurately account for resistance tolerance, aging effects, ambient temperature dependence, and over-voltage-induced shorting behavior. Because aging is primarily a long term and largely irreversible phenomenon, no reversibility mechanism has been included in the simulations, which remains consistent with the physical behavior of real PPTCs.

Each PPTC model is provided in three instances (minimum, nominal, and maximum R_{25} values), allowing designers to evaluate circuit robustness across tolerance spreads. As demonstrated in section 4, these models can be seamlessly used in full application simulations, offering an effective complement to traditional PPTC tutorials and datasheet analyses.

A consistent evaluation workflow is recommended:

- Build a realistic SPICE representation of the target circuit.
- Determine the required hold current.
- Introduce real world parasitics such as hot-plug events and short-circuit faults.
- Select the PPTC with the appropriate voltage rating and hold-current specification.
- Validate performance in transient simulation through temperature sweeps and R_{25} tolerance variations.

Following this process enables designers to fully understand the operating conditions of their application and to develop engineering intuition that cannot be gained from datasheet inspection alone. Finally, before releasing any design into the field, it remains wise to follow Bob Pease's timeless advice: "*verify the simulation results with hands on laboratory testing - preferably with a soldering iron in hand*". The different libraries, plus the simulations described in this article are downloadable online at www.vishay.com/doc?29265 or available by mailing: nlr@vishay.com.