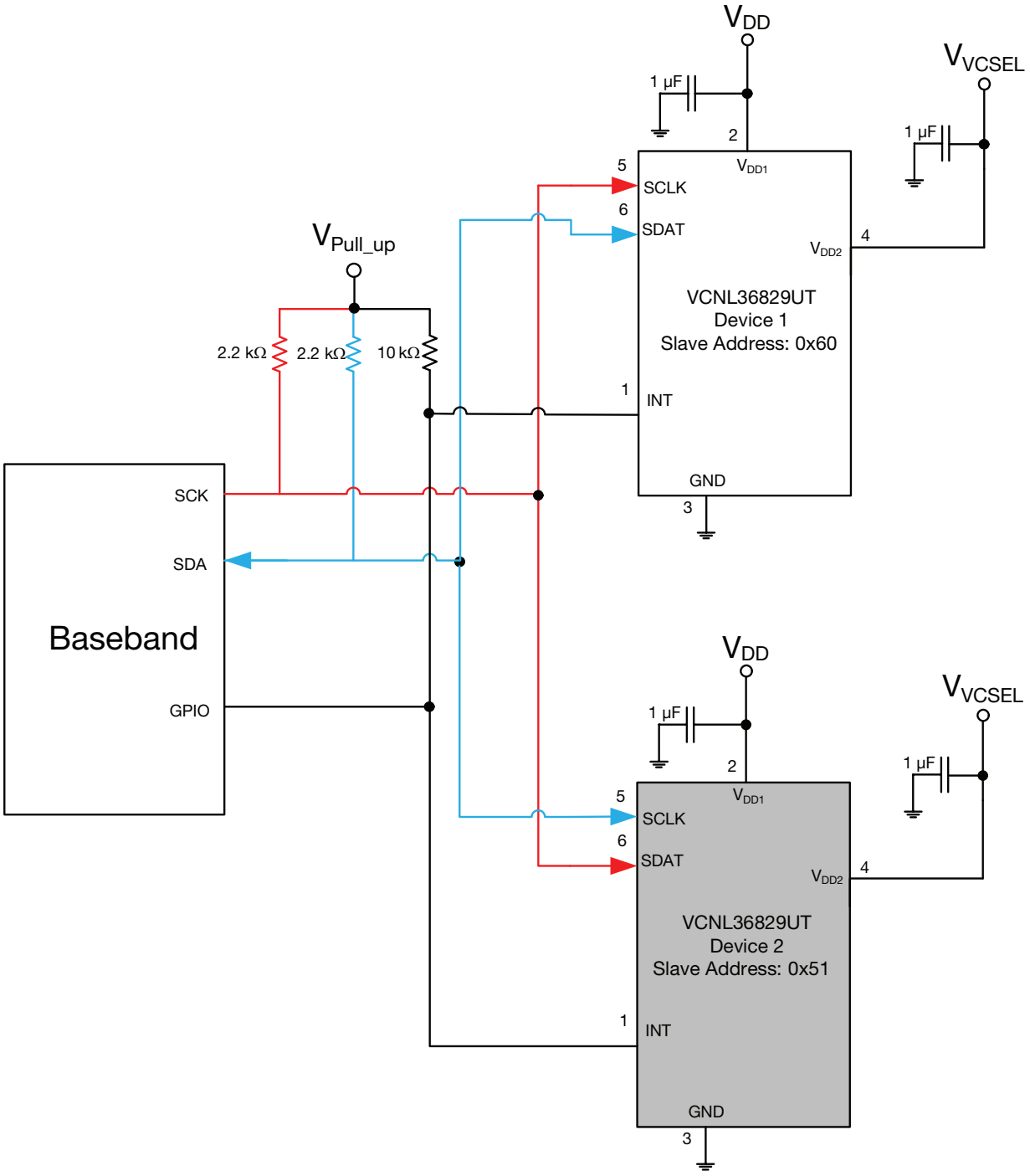
DID YOU KNOW?

DUAL SLAVE ADDRESS FUNCTION: SWAP

To enhance flexibility, dual slave address functionality allows users to conveniently switch between addresses. For example, the VCNL36829UT utilizes this dual slave address capability. By default, the VCNL36829UT uses a 7-bit slave address of 0x60 (HEX). If the SCLK and SDAT lines are interchanged, the slave address changes to 0x51 (HEX) under 7-bit addressing, as shown in the following circuit



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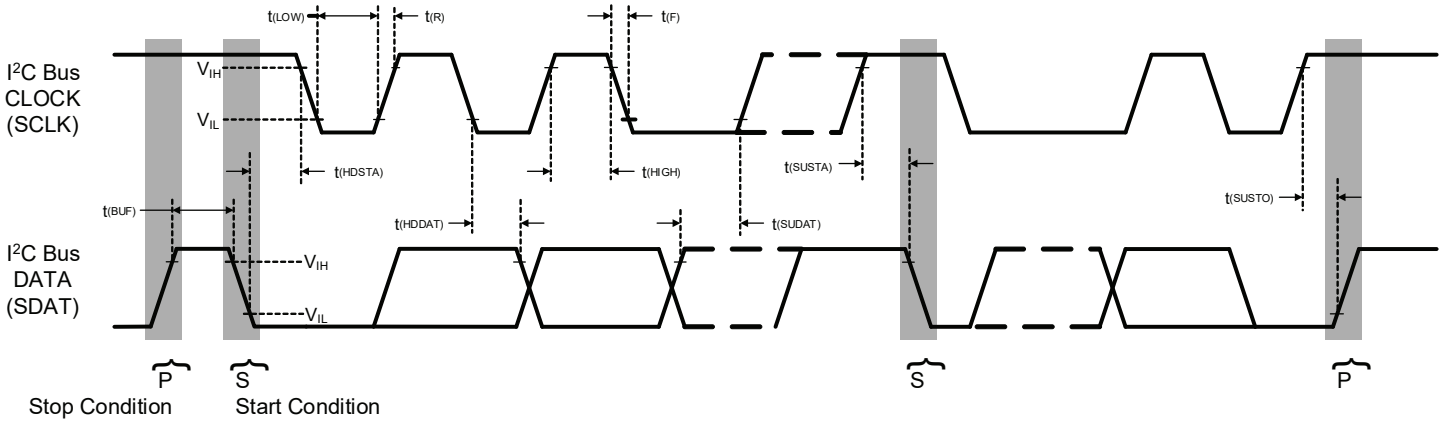
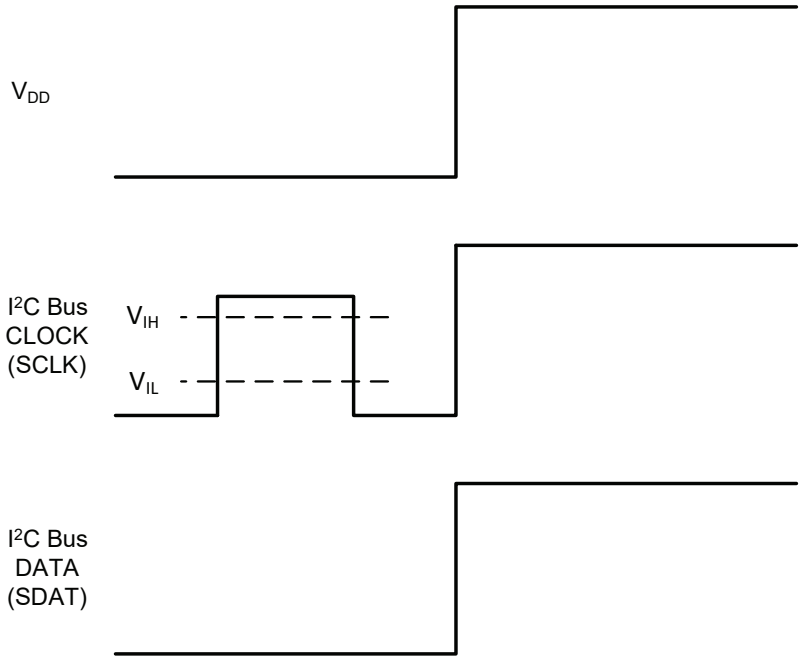
DUAL SLAVE ADDRESS FUNCTION: SWAP

The slave address is determined during the initial power-up phase of the I²C bus. The determination condition is as follows: when V_{DD} initializes with a high voltage, it will start to check the voltage levels of both the SCLK and SDAT. Once the SCLK is at a high voltage (V_{IH}) and the SDAT transitions from high (V_{IH}) to low (V_{IL}), it will trigger the slave address recognition and the slave address will be determined. In the default configuration, the master's SCLK is connected to the slave's SCLK, and the master's SDAT is connected to the slave's SDAT. If the SCLK is held at a high voltage while the SDAT undergoes a voltage change and below V_{IL}, the slave address will be identified as 0x60. Alternatively, if the SCLK and SDAT are interchanged - connecting the master's SCLK to the slave's SDAT and the master's SDAT to the slave's SCLK - the slave address will then be identified as 0x51.



Awareness — Taking a sensor with a slave address of 0x60 as an example, the signals V_{DD}, SCLK, and SDAT play a role. In this scenario, noise interference on the SCLK line results in a small spurious signal on SCLK. Unfortunately, this spurious signal momentarily exceeds the V_{IH} threshold and then drops below the V_{IL} threshold, thereby triggering the slave address recognition mechanism. At that moment, the SDAT remains at a high level, causing the device to incorrectly be identified as having a slave address of 0x51 instead of 0x60. Consequently, issuing commands to either the 0x60 or 0x51 slave addresses will not result in any response or action from the device.



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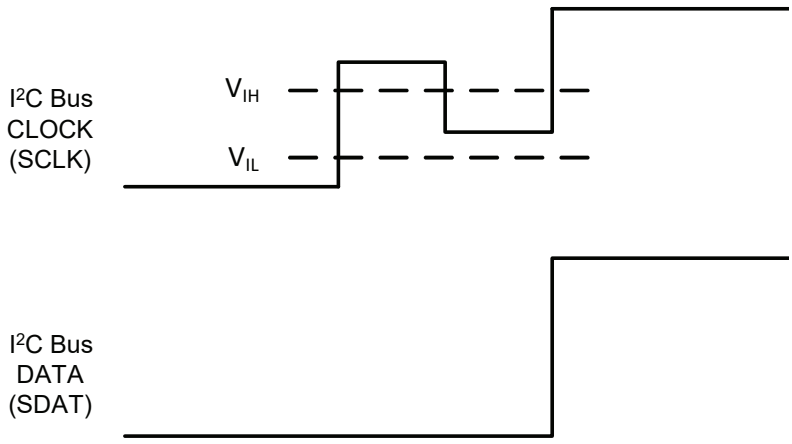
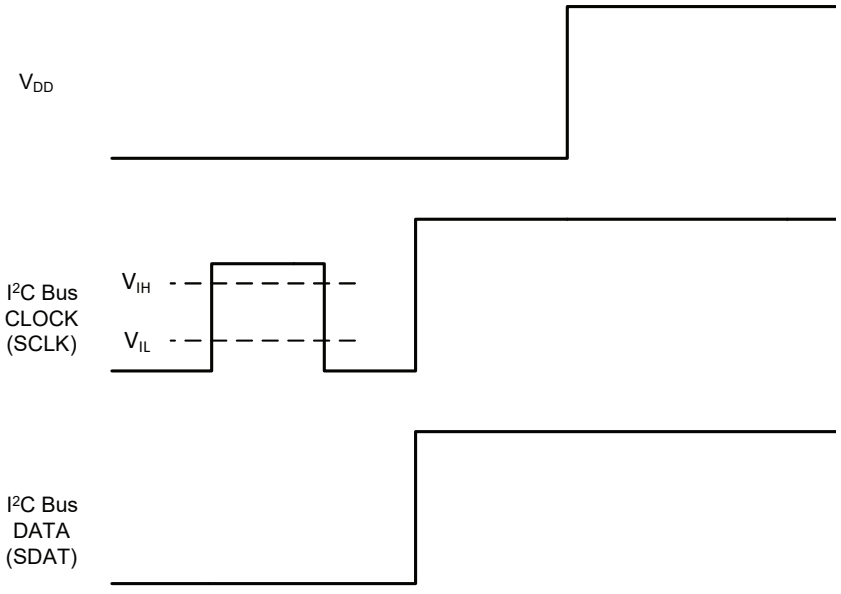
DUAL SLAVE ADDRESS FUNCTION: SWAP

To prevent misinterpretation and avoid errors in slave address identification that could lead to failure in normal read or command operations, the following recommendations are provided:

1. **Signal stabilization:** ensure stable signals and minimize noise on the I²C bus to reduce the likelihood of erroneous triggers.
2. **Threshold management:** even in the presence of minor noise, avoid conditions where noise exceeds the V_{IH} threshold and subsequently drops below the V_{IL} threshold. If noise remains below V_{IH}, stays consistently above V_{IH}, or does not drop below V_{IL} after exceeding V_{IH}, the slave address confirmation process will not be triggered, preventing slave address misidentification.



3. **Ramp up timing:** since the slave address is determined immediately after the sensor V_{DD} is powered on, it is recommended to fully ramp up the SCLK and SDAT lines before ramping up the sensor's V_{DD}. This ensures that any noise present during the transition to V_{IH} does not affect the slave address recognition process.
4. **Re-trigger V^{DD}:** if a misidentification occurs, disconnect and reconnect the sensor's V_{DD} to force the senor to reinitialize the slave address recognition process.



By following these guidelines, potential errors in slave address recognition can be effectively mitigated, ensuring reliable communication over the I²C bus.