



The DNA of tech.™

## SiZF640DT Symmetric Dual N-Channel 40 V MOSFET

# Save Space While Simplifying PCB Layouts and Minimizing Parasitic Inductance

### ADVANTAGE

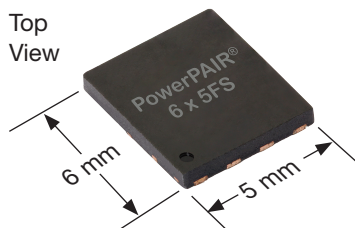


In space-constrained applications, the SiZF640DT reduces PCB requirements by 50 % compared to discrete devices.

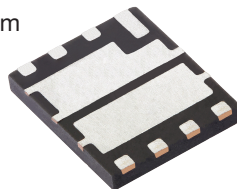
### KEY PRODUCT FEATURES

- ✓ PowerPAIR® 6 × 5FS symmetric dual integrated package
- ✓ High side and low side MOSFETs form optimized combination for 50 % duty cycles
- ✓ Pin assignment matches layout concept
- ✓ Gate return for short loop and minimized parasitic inductance
- ✓ Maximum  $V_{IN}$  and GND pad for enhanced thermal dissipation
- ✓ 100 %  $R_g$  and UIS tested

Top View



Bottom View



### MARKETS AND APPLICATIONS



#### INDUSTRIAL

- Half-bridge synchronous rectification in brushless DC motor drives, welding equipment, converters, robotics, power tools, and garden equipment



#### COMPUTER

- Half-bridge synchronous rectification in servers, embedded applications, edge computing, portable computers, tablets, and super computers; type C chargers



#### CONSUMER

- Half-bridge synchronous rectification in cleaning robots



#### CONNECTIVITY

- Half-bridge synchronous rectification in telecom mobile infrastructure, including radio base stations and PSUs

### RESOURCES



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[Pad Pattern](#)



[Package Information](#)

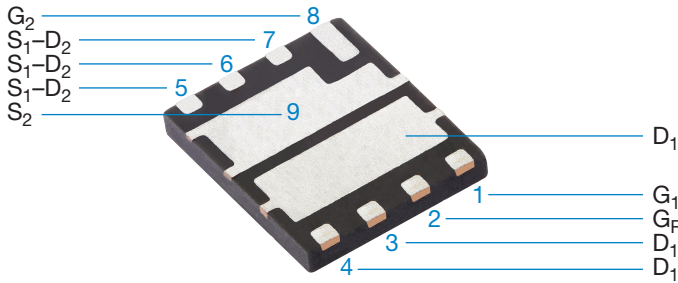


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## POWERPAIR® 6 × 5FS PIN ASSIGNMENTS

Pin assignments for the PowerPAIR 6 × 5FS are designed to facilitate layouts and to minimize parasitic inductance by making the equivalent loop area covered by traces as small as possible.

Bottom View

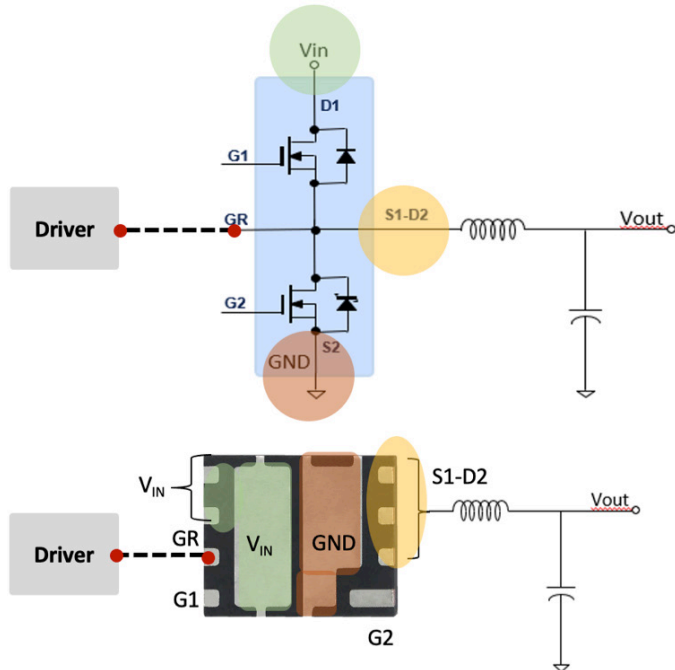


## SPECIFICATION TABLE

Part number	SiZF640DT
Package	PowerPAIR® 6 × 5FS
Configuration	Symmetric Dual N
$V_{DS}$ (V)	40
$V_{GS}$ (V)	+20 / -16
$R_{DS(ON)}$ typ. @ 10 V (mΩ)	1.0
$R_{DS(ON)}$ max. @ 10 V (mΩ)	1.37
$R_{DS(ON)}$ typ. @ 4.5 V (mΩ)	1.6
$R_{DS(ON)}$ max. @ 4.5 V (mΩ)	2.4
$Q_g$ @ 10 V (nC)	69
$Q_g$ @ 4.5 V (nC)	30
$Q_{gs}$ (nC)	21
$Q_{gd}$ (nC)	1.5
$R_g$ typ. (Ω)	1.7

## BUCK CONVERTER BLOCK DIAGRAM

- Optimal  $V_{IN}$  and GND pad
- Ultra short loop for switching
- Gate return simplifies layout



## MOTOR DRIVE BLOCK DIAGRAM

- Optimal  $V_{IN}$  and GND pad
- Ultra short loop for switching

