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Microwave Thin Film Resistors

Application Note

High Frequency Behavior of CHA Series Resistors Following AEC-Q200 Qualification Tests

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SUMMARY

This application note describes ways to measure S-parameters and deduce impedance values of chip resistors at frequencies up to 70 GHz.

A good board design, alongside precise measurements, allows for a comparison of the impedance over frequency before and after AEC-Q200 tests, and shows the high stability of CHA series thin film chip resistors.

Precise measurements at high frequencies require suitable characterization boards and assembly and analyzing methods. Supplying these while demonstrating the impedance stability of Vishay resistors - particularly in demanding automotive environments, where electronic components must endure harsh conditions and continue to operate flawlessly - is the primary objective of this application note.

CHA SERIES RESISTORS

Vishay's unique CHA series of microwave AEC-Q200 qualified resistors, available with gold (P) and tin / silver (F) terminations, offers best in class performance for IoT, mmWave, 5G, radar, and other high frequency applications. These miniaturized components are designed in such a way that their internal reactance is very small. When correctly mounted and used, they function as almost pure resistors over a very large range of frequencies up to 70 GHz. CHA series devices are available with ohmic values between 10 Ω and 500 Ω .

This application note focuses on 50 Ω and 100 Ω resistors in the 02016 package, which are often used in high frequency applications, such as Wilkinson dividers, splitters, and attenuators.

For additional details, please refer to the CHA series datasheet: www.vishay.com/ppg?53086.

HIGH FREQUENCY RESISTOR SUMMARY

Parasitic elements inherent to resistors by construction are generated by the resistor-circuit interface (described in <u>www.vishay.com/doc?53077</u>).

The S-parameters shown in Fig. 1 are defined according to a scattering matrix where incidents (a1, a2) and reverse waves (b1, b2) are defined as the square root of the power.



Where:

- $S_{11} = b_1 / a_1$ with $a_2 = 0$
- $S_{21} = b_2 / a_1$ with $a_2 = 0$

Designers can use the S-parameters (<u>www.vishay.com/doc?53061</u>) or impedance characterization to perform hyper-frequency z simulations and compare system results. Component usage requires propagation into a PCB where the component is mounted as a quadripolar element. The mounting influence and design topology made with PCB technology permit high frequency Z characterization using calibration, as required in hyper-frequency applications.

• $S_{22} = b_2 / a_2$ with $a_1 = 0$

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When the component is mounted on the board, the whole component, including parasitic elements, is modeled thanks to a π structure (see Fig. 2).



Fig. 2 - Electrical Model Equivalent for HF Applications of a CH / CHA Component

Where:

- R is the nominal resistance value
- L is the inductance linked to the resistor
- C is the capacitance linked to the resistor
- L_c is the parasitic inductance due to the resistor mounting
- C_g is the parasitic capacitance due to the resistor mounting
- Z_o is the characteristic impedance of the line



Fig. 3 - CHA Quadripolar PI Structure

The π structure illustrated in Fig. 3 is used as a two-port representation of the DUT. We derive impedance from the transmission admittance conversion (as well as ABCD parameters), which forms the measured S-parameters after calibration:

$$Z = B = \frac{-1}{Y_{21}} = Z_0 \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2 \times S_{21}}$$

Therefore, even if it is not possible to measure the impedance Z directly, key component parameters, such as impedance and the influence of AEC-Q tests on impedance, can still be obtained.

As in the CH / CHA series datasheets, throughout this document we will use the normalized value |Z|/R, where R is the ohmic value of the resistor under test to visualize, and compare the behavior of our CH / CHA component.

Using this approach, Fig. 4 compares the normalized impedance over frequency of an ideal and real 50 Ω resistor.





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HIGH FREQUENCY PCB DESIGN

HF applications require high quality materials. Care should be taken to choose low loss substrates with an adequate dielectric constant that can maintain its isolation properties to frequencies of 40 GHz and higher.

We have designed a 3D-encrypted CHA component (substrate, ohmic value, termination, etc.). Using this 3D-encrypted model, a top-down methodology permits the best compromise on the PCB to be made (topology, characteristic impedance, connector layout, etc.) to enhance the CHA behavior after calibration and during the measurements.

Finally, best choice (Fig. 5) is a specific PCB series with a coplanar waveguide with ground (CPWG) topology for both thru reflect line (TRL) and device under test (DUT) boards.

The 3D HFSS encrypted components are available to customers.



Fig. 5 - CHA Mounted on DUT Characterization Board

To study the impact of AEC-Q200 tests on the DUT, we use HF connectors to allow easier mounting / unmounting of sampling quantities during calibration and measurements. Using a TRL calibration instead of resistance-based calibration, the calibration cancels the effects of the VNA / cables / connectors / DUT over reference plan (Fig. 6).



Fig. 6 - TRL Calibration Board

Via technology is used to avoid the substrate wave mode and increase the cut-off frequency in the pre-preg layer, maintaining a good impedance characteristic at 50 Ω in the 1 GHz to 70 GHz band. To be representative of customer applications and multi-layer stacking, especially for AEC-Q200 tests, we use a 1 mm multi-layer PCB, as is standard in the industry. This avoids mechanical issues and permits easy electronic component assembly.

A compromise between optimizing the impedance characteristic over frequency and minimizing discontinuities by the matching of the resistor footprint to the connector via tapered lines was found. This design is depicted in Fig. 7.



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This was enabled by using a CPWG, as depicted in Fig. 8, allowing for characterization up to 70 GHz with reference plans focused on the resistive layer.



Fig. 8 - Reference Plans for CHA Characterization (red for DUT, blue for component)

RECOMMENDATIONS FOR IMPROVED ASSEMBLY OF SURFACE-MOUNT TECHNOLOGY

Due to the (very) small size of the 02016 package (approx. 0.4 mm x 0.5 mm), the main assembly failure mode is excessive tilting (Fig. 9).



Fig. 9 - Excessive Tilting vs. Good Assembly

To limit tilting during assembly and soldering, we recommend:

- Using the land pattern dimensions suggested in the CH / CHA datasheet (Fig. 10)
- Depositing the right amount of solder paste by reducing the stencil thickness from 0.1 mm down to 0.08 mm, or by reducing the aperture size, as illustrated in Fig. 11
- Using the solder paste based on IPC-J-STD-005 (type 4 or higher), e.g. SAC 305 solder paste made of 96.5 % tin, 3 % silver, and 0.5 % copper for lead (Pb)-free soldering
- Using the J-STD-020 thermal profile, or profile no. 3, from our application note "Guidelines for Vishay Sfernice Resistive and Inductive Components" (chapter 3.2), as presented in Fig. 12. (www.vishay.com/doc?52029) for soldering



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Fig. 11 - Stencil Aperture and Stencil vs. Land Pattern Illustration

RECOMMENDED REFLOW PROFILES									
PROFILE	T _p lead (Pb)-free	tp	T _L lead (Pb)-free	T _{S min.} lead (Pb)-free	T _{S max.} lead (Pb)-free	t _s lead (Pb)-free	tL		
3	260 °C	10 s	219 °C	150 °C	200 °C	60 s to 150 s	60 s		



Fig. 12 - Reflow Profile Recommendation

By implementing these recommendations, the excessive tilting of the CHA 02016 case size can be reduced to a minimum.

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AEC-Q200 COMPLIANT AND HYPER-FREQUENCY CHARACTERIZATION PROTOCOL

Automotive applications require electronic components that must operate reliably even when the environment is harsh. The Automotive Electronics Council (AEC) established the AEC-Q200 standards for passive components. The CHA 02016 is qualified to these standards and demonstrates exceptional performance.

TABLE 1 - AEC-Q200 TEST PROCEDURES AND REQUIREMENTS									
AEC-Q200 CLAUSE	TEST	PROCEDURE	GLOBAL PERFORMANCES	TYPICAL PERFORMANCES (25 Ω TO 250 Ω)					
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 125 °C, unpowered	\pm 2 % \pm 0.05 Ω	\pm 0.2 % \pm 0.05 Ω					
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	\pm 1.8 % \pm 0.05 Ω	\pm 1.5 % \pm 0.05 Ω					
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power	± 2 % ± 0.05 Ω	$\pm 0.75 \% \pm 0.05 \Omega$					
8	Operational life	MIL-STD-202 method 108 condition D steady state T = 125 °C at rated power 90' on / 30' off / 1000 h	\pm 2.5 % \pm 0.05 Ω	± 1 % ± 0.05 Ω					
13	Mechanical shock	MIL-STD-202 method 213 condition C 100 g/6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	$\pm 0.05 \% \pm 0.05 \Omega$	$\pm 0.015~\% \pm 0.05~\Omega$					
14	Vibration	MIL-STD-202 method 204 5 <i>g</i> for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	\pm 0.1 % \pm 0.05 Ω	$\pm 0.05 \% \pm 0.05 \Omega$					
15	Resistance to soldering heat	MIL-STD-202 method 210 condition D Flux used: alpha 611 Solder temp.: 260 °C ± 5 °C Total immersion during 10 s	$\pm 2.5 \% \pm 0.05 \Omega$	$\pm 0.5~\% \pm 0.05~\Omega$					
17	ESD	AEC-Q200-002	Classification 1C 1000 V_{DC} to 2000 V_{DC}						
18	Solderability	J-STD-002 - Preconditioning 4 h dry heat aging and 235 °C SnPb 5 s - 215 °C SnPb 5 s - 260 °C SnAgCu 10 s	Good tinning (≥ 95 % covered) No visible damage						
20	Flammability	UL 94	Class V-0 No burning						
21	Board flex	AEC-Q200-005	$\pm~0.1~\%~\pm~0.05~\Omega$	$\pm~0.05~\%~\pm~0.05~\Omega$					
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C						

We applied all the AEC-Q200 tests to the component. In addition, we measured the high frequency stability before and after these selected tests:

- High temperature exposure: 1000 h at 125 °C unpowered
- Temperature cycling: 1000 cycles (-55 °C to +125 °C)
- Biased humidity: 1000 h at 85 °C / 85 % hum. and 10 % of operating power
- Operational life: 1000 h at rated power and Ta = 125 °C

Z S-parameter measurements and quadripolar impedance computation characterizations are made in real time thanks to the Ζ admittance conversion and computation capabilities of VNA, as presented in the "HF resistor summary" section above. The 0 frequency characterization is summarized in Fig. 13 and Fig. 14.

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Fig. 13 - Serialization of Measurements, Comparison Between Final vs. Initial Measurements



Fig. 14 - Comparison Between Final Measurements vs. Datasheet

HIGH FREQUENCY CHARACTERIZATION AND RESULTS

By using the test boards described in the previous sections, high accuracy values for the normalized impedance over frequency of the CHA series resistors were taken before and after being subjected to various AEC-Q200 test procedures. Fig. 15 shows the changes induced by exposure to the biased humidity test; Fig. 16 depicts changes originating from operational life testing; Fig. 17 shows the normalized impedance after high temperature exposure compared to datasheet values; and Fig. 18 shows normalized impedance after temperature cycling alongside the datasheet value.



Fig. 15 - Frequency Response of a 100 Ω CHA02016 Before (-I) and After (-F) a AEC-Q200 Biased Humidity Test

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Fig. 16 - Frequency Response of a 100 Ω CHA02016 Before (-I) and After (-F) a AEC-Q200 Load Life Test



Fig. 17 - Frequency Response of a 50 Ω CHA02016 After AEC-Q200 Temperature Cycling vs. Datasheet Values



Fig. 18 - Frequency Response of a 50 Ω CHA02016 After AEC-Q200 High Temperature Exposure vs. Datasheet Values

CONCLUSION

Our new AEC-Q200 qualified mmWave CHA02016 resistors provide stable high frequency performance up to 70 GHz, or and maintain that stability even after the most stressful AEC-Q200 tests simulating harsh automotive environmental conditions.

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