

AEC-Q200 Qualified High Frequency 70 GHz Thin Film Termination Resistor



FEATURES

- Up to 70 GHz at 1.2 VSWR (1 % loss)
- HFSS encrypted model available
- AEC-Q200 qualified
- Thin film microwave resistors
- 50 Ω and 100 Ω available
- [Modelithics®](#) library available
- Optimized land patterns
- Small internal reactance (LC down to 1×10^{-24})
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(5-2008)

LINKS TO ADDITIONAL RESOURCES



3D Models



S-Parameters



Simulation Tools

The CHTA02016 miniaturized 50 Ω and 100 Ω components are engineered with extremely low internal reactance, making them ideal for termination mounting and enabling excellent VSWR performance. When properly mounted and operated, they behave as near ideal termination resistors across an exceptionally wide frequency range, extending from DC up to 70 GHz for the 50 Ω CHTA02016 variant.

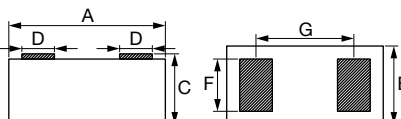
STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER P_n ⁽¹⁾ W	LIMITING ELEMENT VOLTAGE V	TOLERANCE $\pm$ %	TEMPERATURE COEFFICIENT $\pm$ ppm/ $^{\circ}$ C
CHTA02016	02016	50 and 100	0.100	30	1, 2, 5	100 (50 upon request)

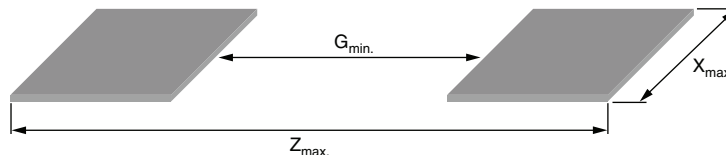
Note

⁽¹⁾ PCB mounting with +70 $^{\circ}$ C ambient temperature

DIMENSIONS in millimeters (inches)



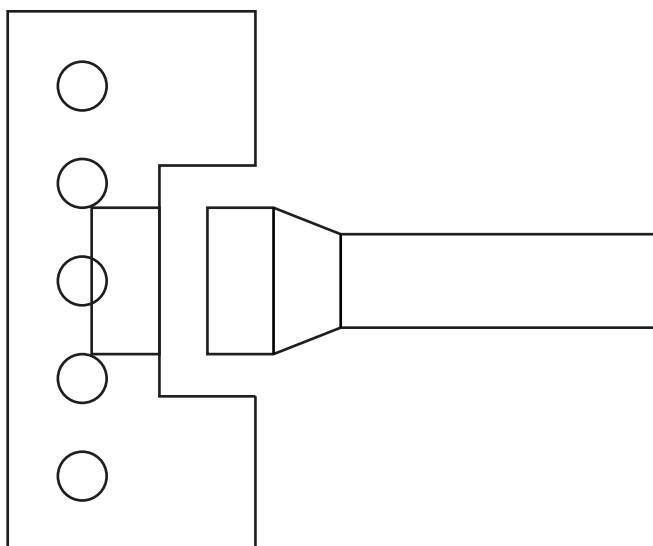
CASE SIZE MODEL / TERMINATION	DIMENSIONS					
	A $\pm$ 0.10 ($\pm$ 0.004)	B $\pm$ 0.10 ($\pm$ 0.004)	C $\pm$ 0.127 ($\pm$ 0.005)	D E when applicable		F $\pm$ 0.050 ($\pm$ 0.002)
				MIN.	MAX.	G $\pm$ 0.050 ($\pm$ 0.002)
CHTA02016 F	0.480 (0.020)	0.390 (0.016)	0.420 (0.016)	0.110 (0.004)	0.150 (0.006)	0.260 (0.010)

LAND PATTERN FOR F “FLIP CHIP” TERMINATIONS in millimeters (inches)


CHIP SIZE	$Z_{max.}$	$X_{max.}$	$G_{min.}$
02016	0.53 (0.021)	0.44 (0.017)	0.15 (0.006)

Notes

- Suggested land pattern: according to IPC-7351
- Land pattern dimensions are given for quadripole applications and DC applications
- Dimension and tolerance of land pattern shall be defined by PCB designer; PCB can be designed according to IPC-7351A “Generic Requirements for Surface Mount Design and Land Pattern Standard”

SUGGESTED LAND PATTERN FOR TERMINATION APPLICATIONS


Vishay Sfernice designed for 50 Ω applications using 0.127 mm (0.005") thick Ro3003G2 with MS topology. This land pattern was designed to provide the best behavior for impedance stabilization and losses reduction (VSWR) according to one 50 Ω resistor. Other configurations are possible when source impedances are matched to 50 Ω (GPCW, MS, multi-via etc).

PERFORMANCE

TEST PROCEDURES AND REQUIREMENTS				
AEC-Q200 CLAUSE	TEST	PROCEDURE	GLOBAL PERFORMANCES	TYPICAL PERFORMANCES (25 Ω TO 250 Ω)
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 155 °C, unpowered	$\pm 2 \% \pm 0.05 \Omega$	$\pm 0.2 \% \pm 0.05 \Omega$
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	$\pm 1.8 \% \pm 0.05 \Omega$	$\pm 1.5 \% \pm 0.05 \Omega$
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power	$\pm 2 \% \pm 0.05 \Omega$	$\pm 0.75 \% \pm 0.05 \Omega$
8	Operational life	MIL-STD-202 method 108 condition D steady state T = 125 °C at rated power 90' ON / 30' OFF / 1000 h	$\pm 2.5 \% \pm 0.05 \Omega$	
13	Mechanical shock	MIL-STD-202 method 213 condition C 100 g/6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	$\pm 0.05 \% \pm 0.05 \Omega$	
14	Vibration	MIL-STD-202 method 204 5 g for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	$\pm 0.1 \% \pm 0.05 \Omega$	
15	Resistance to soldering heat	MIL-STD-202 method 210 condition D Flux used: alpha 611 Solder temp.: 260 °C $\pm$ 5 °C Total immersion during 10 s	$\pm 2.5 \% \pm 0.05 \Omega$	
17	ESD	AEC-Q200-002	Classification 1C 1000 V _{DC} to 2000 V _{DC}	
18	Solderability	J-STD-002 - Preconditioning 4 h dry heat aging and 235 °C SnPb 5 s - 215 °C SnPb 5 s - 260 °C SnAgCu 10 s	Good tinning ($\geq 95 \%$ covered) No visible damage	
20	Flammability	UL 94	Class V-0 No burning	
21	Board flex	AEC-Q200-005	$\pm 0.1 \% \pm 0.05 \Omega$	$\pm 0.05 \% \pm 0.05 \Omega$
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C	

Note

- Performance according to Rev. E of AEC-Q200

PREFERRED MODELS AND VALUES

Recommended values:

50 Ω / 100 Ω

Minimum order quantity for waffle pack:

484

Minimum order quantity for tape and reel:

1000

Other values can be ordered upon request, but higher MOQ will apply: 1000 pieces for CHTA02016.

Recommended termination:

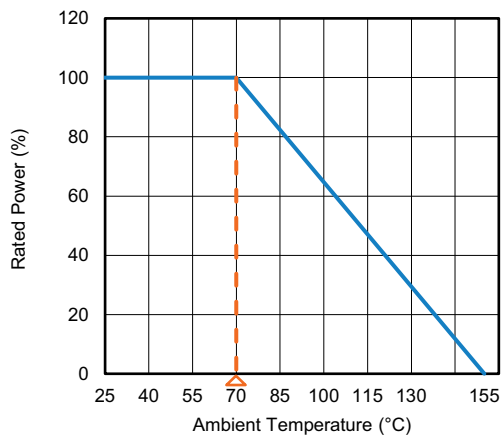
F

Recommended tolerance:

2 %

TEST BOARDS

TRL (Thru Reflect Line) and DUT (Device Under Test) evaluation boards (50 Ω or 100 Ω) are available on request.

**THERMAL SPECIFICATIONS****POWER DERATING CURVE****BACKSIDE CHIP TEMPERATURE +25 °C**

CHIP SIZE	POWER ⁽¹⁾ (W)
02016	0.100

Note

⁽¹⁾ Estimations with components thermal resistance knowledge

PACKAGING

Standard packaging is plastic tape and reel for all sizes.

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE		TAPE WIDTH
		TAPE AND REEL		
		MIN.	MAX.	
02016	1000 tape and reel	1000	10 000	8 mm

Note

- See "Codification of Packaging" table for additional details

Flip chip:

Tin / silver terminations: (F termination option): Active face down in tape and reel.

Notes

- CHTA02016 with active face down in tape and reel have back-side blue marked to indicate right orientation
- Please refer to Vishay Sfernice Application Note [Guidelines for Vishay Sfernice Resistive and Inductive Components](#) for soldering recommendation (document number 52029, section "3. Guidelines for Surface Mounting Components (SMD)", profile number 3 applies

PACKAGING RULES**Tape and Reel**

See Part Numbering information to get the quantity desired by tape.

Regarding the CHTA02016 size only, up to 5 empty cavities can be found every 1000 parts in the reel. Nevertheless, the number of requested parts will be respected.

GLOBAL PART NUMBER INFORMATION

Part Number Example: CHTA02016-100RFFTF (AEC-Q200 qualified termination CHTA series, 100 Ω, 1 % tolerance, 5000 pieces reels)

C	H	T	A	0	2	0	1	6	-	1	0	0	R	F	F	T	F
GLOBAL MODEL				SIZE		OHMIC VALUE		TOLERANCE		TERMINATION		PACKAGING					
CHTA				02016		50R 100R		F = 1 % G = 2 % J = 5 %		F (flip chip): SnAg over nickel barrier		For more information see "Codification of Packaging" table					

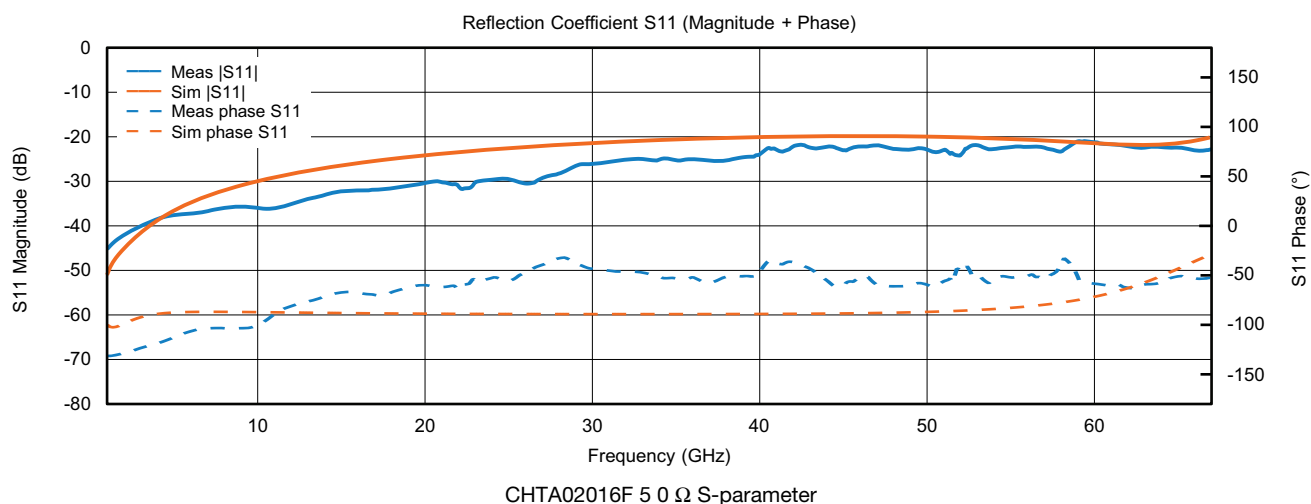


CODIFICATION OF PACKAGING	
SAMPLES-CUT TAPE	
CT	20 min., 20 mult.; 20 pcs max.
PLASTIC TAPE	
TD	1000 min., 1000 mult.; delivered in reels of 1000 pcs
TF	5000 min., 5000 mult.; delivered in reels of 5000 pcs
TG	10 000 min., 10 000 mult.; delivered in reels of 10 000 pcs

S-PARAMETER

Based on previous land pattern recommendations for 50 Ω 02016 size case.

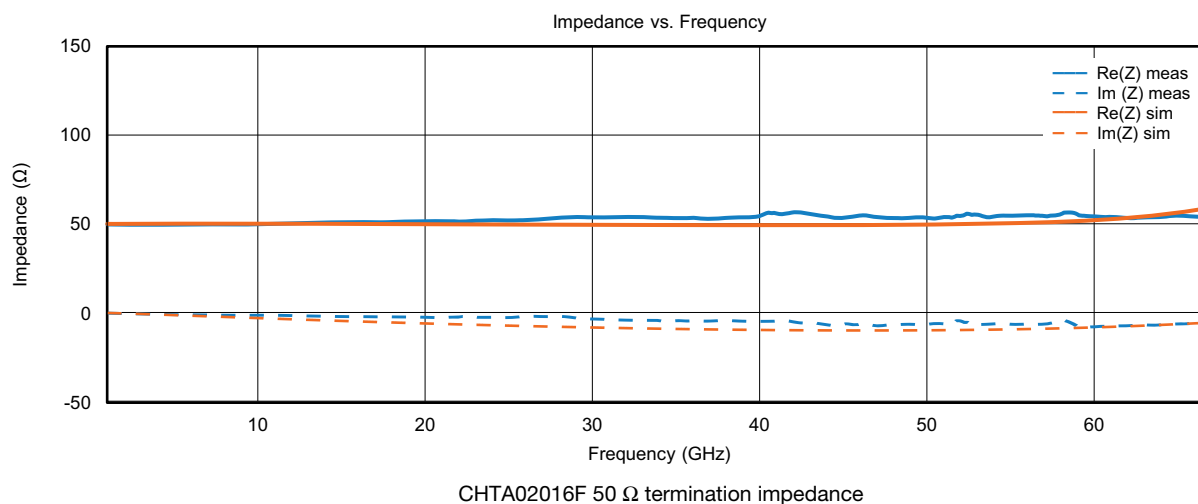
Showing magnitude (solid) and phase (dash).



IMPEDANCE CURVES

Based on previous land pattern recommendations for 50 Ω 02016 size case.

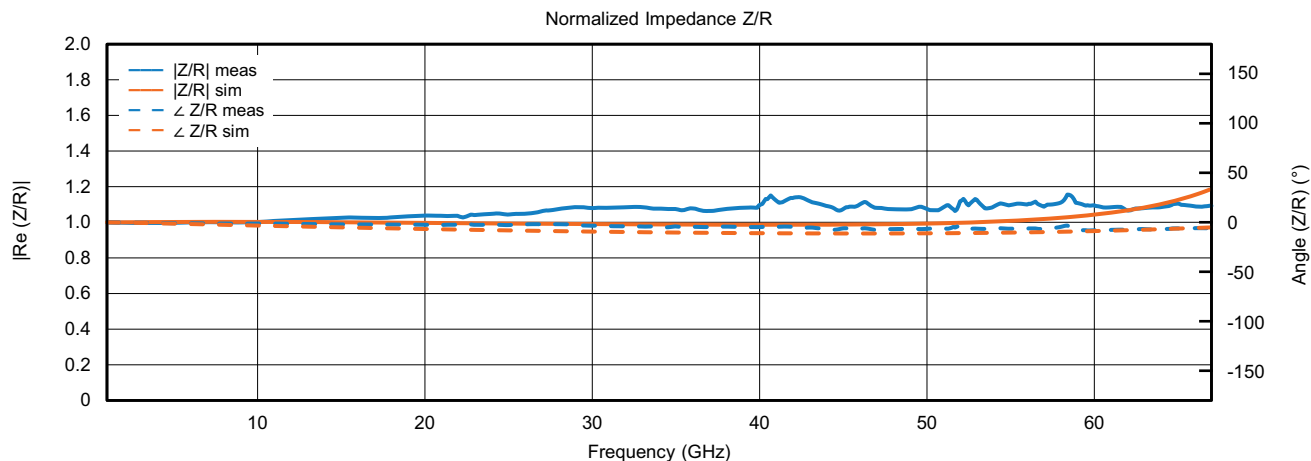
Showing the real part (solid) and imaginary part (dash) of impedance.



NORMALIZED IMPEDANCE

Regarding previous land pattern recommendations for 50 Ω 02016 size case.

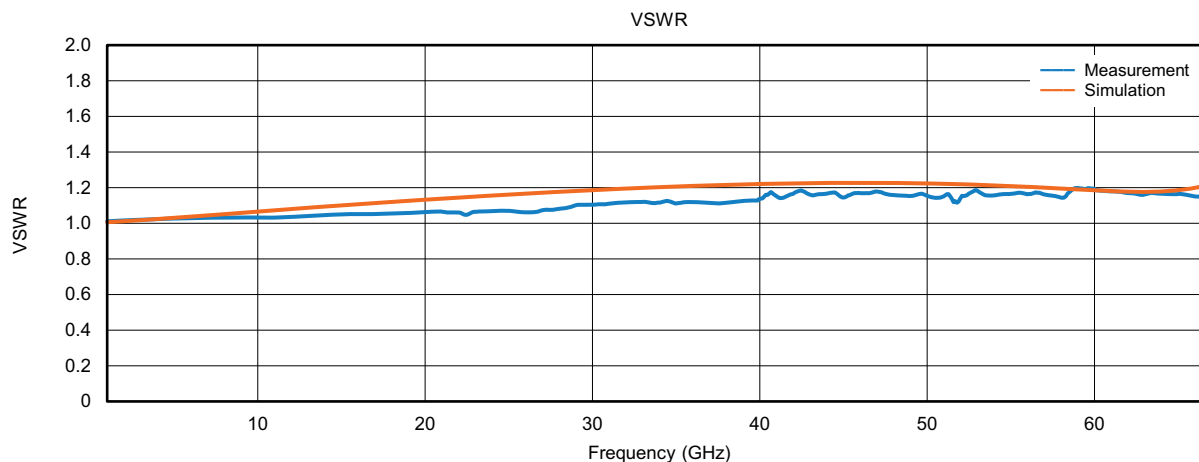
Showing real part of normalized impedance (solid) and angle (dash).



CHTA02016F 50 Ω termination normalized impedance

VSWR

Regarding previous land pattern recommendations for both 50 Ω and 100 Ω 02016 size cases.

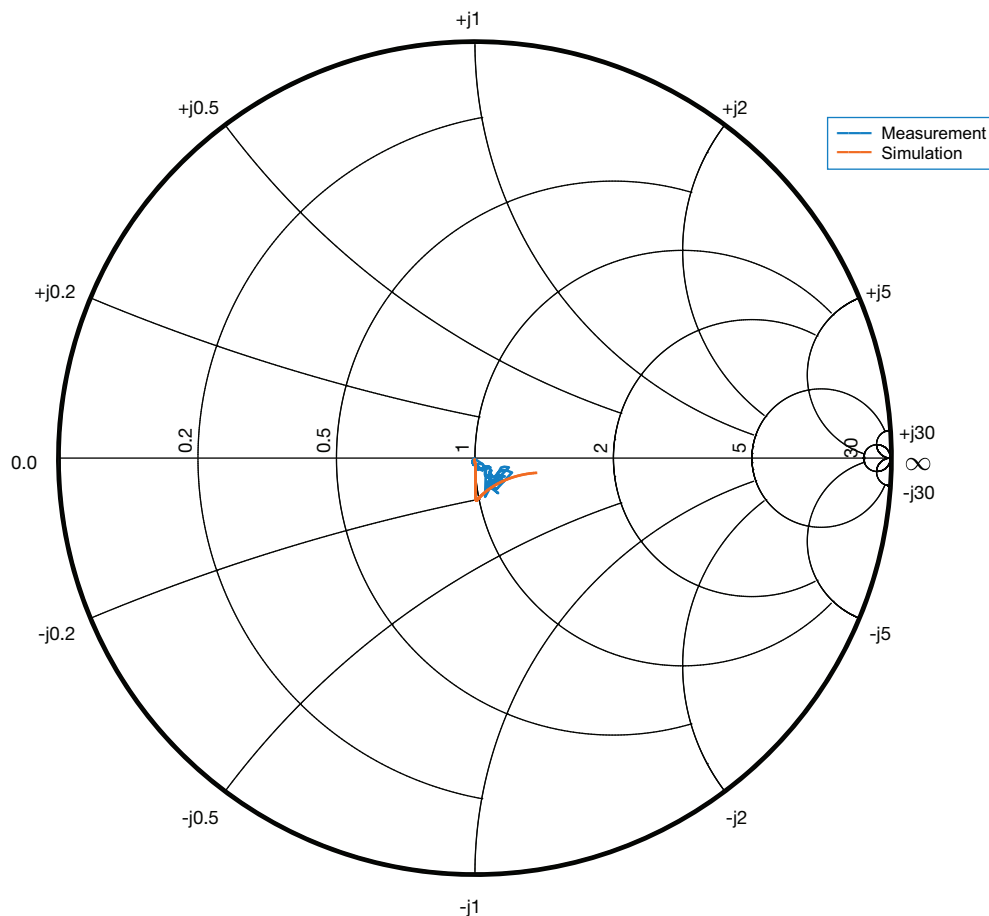


CHTA02016F 50 Ω VSWR performance

SMITH DIAGRAM

Regarding previous land pattern recommendations for 50 Ω 02016 size case.

Shows real part of normalized impedance (solid) and angle (dash), in simulation (blue) and measurements (black) cases.



CHTA02016F 50 Ω Smith chart diagram



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